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A Low Noise, Voltage Control Ring Oscillator Based on Pass Transistor Delay Cell

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ABSTRACT: Voltage control ring oscillators are the heart of communication system. They are widely used in PLL for frequency synthesize. This paper presents the design of low noise voltage control ring oscillator in 0.18µm CMOS technology for the application ofFM radio telecommunication (88MHz-108MHz).The proposed design consists of five delay cell stages. The output Frequency tuning range is 71MHz-112MHz and Control voltage varies from 0V to 0.8V. The proposed voltage control ring oscillator (VCRO) achieves a phase noise of -117.92dBc/Hz at a 1 MHz offset frequency. We have used the inverter based pass transistor delay cell technique to improve linear characteristics and to decrease thepower dissipation of the designed circuit. We have also used NMOS as active resister load to improve the phase noise. The supply voltage (Vdd) used is 0.8V and the maximum power consumption is 317.2 µW.

KEYWORDS: Oscillator, Power Consumption, Phase noise, Frequency tuning, Delay cell, VCO.

I. INTRODUCTION

Every communication system transmits and receives data from the other transceiver system. For this the system has to work on certain frequency. Fig. 1 is the block diagram of PLL. Phase locked loops (PLL) are used to generate and synthesize that required frequency for the communication system [1]. Voltage control oscillator generates the required frequency for the PLL block and thus VCOs are the main frequency generating units for PLL.Phase detector detects the phase of input signal and compares it with the output phase of the VCO. Hence changes the output of the loop filter .Voltage control oscillator generates the output frequency according to the voltage generated by theloop filter unit. PLL is generally used as a clock recovery circuit. There are mainly two types of oscillators. Inductor capacitor based VCOs and Ring VCOs. Ring VCO consumes smaller layout area and lower power dissipation. Ring oscillators are having less design complexity and they provide wide tuning range [9]. These days' ring VCOs are also implemented on two topologies these are single ended ring VCO and Differential ended ring VCO. Differential ring oscillator typically requires more power consumption and chip area size compared to single ended ring VCOs [2].

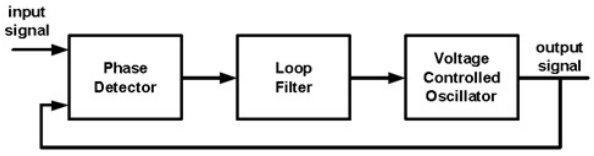

Fig. 1 PLL General Block diagram

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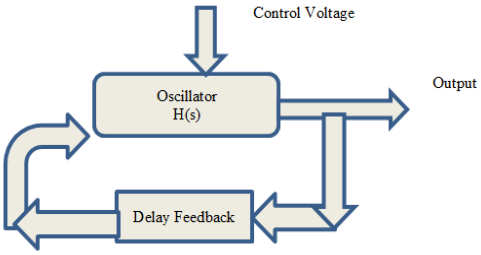

Fig. 2 Delayed feedback oscillation

However a modern communication system widely uses system on chip. That is because of its compactness and lower power dissipation and thus in order to take these advantages it is difficult to design inductor and capacitor based VCOs on the semiconductor chip.Taking about ring VCOs these are quite good because they are not having any on chip inductor or capacitor. Thus we have designed single ended inverter based ring oscillator. Periodic output signal can be generated by the oscillator with respect to control voltage. A simple oscillatory system can be seen in Fig 2. It shows the oscillatory feedback system. For sustain oscillation the oscillatory system must follow the Barkhausen's stability criteria and should became sustain periodic signal[2]. According to Barkhausen's criteria two condition must be simultaneously satisfy for sustain oscillation that are the loop gain must be unity and total phase shift around the loop must be equal to zero or 360˚.

II. RELATED WORK

In [2] the proposed VCO is based on single ended delay cell topology. It is an inverter based VCO which uses single ended type of delay cells. This is four stage VCO which operates from 12.6MHz to 48MHz. It gives full swing, wide tuning range and can operate at both high and low frequency mode. Reference [2]uses 1 V as power supply and its topology reduces the static power dissipation. Higher amplifier trans-conductancecan be achieved through its current reuse technique. The maximum power dissipation shown by this design is 1.2mW. The referenced circuit also uses band select circuit to work on higher and lower frequency. When band selective input is 0V it works at lower frequency from12MHz to 22MHz but when band selective input is 1V it works on higher frequency mode from 22MHz to 48MHz. In [3] current starve based VCO is shown with the input biased stage. It has 5 number of inverter based delay stages which centred at 1300MHz oscillation frequency. Reference [4] uses the differential type of delay cells to improve the phase noise performance. The reference paper derives the Frequency equation including gate resistance. It has also shown the relation between number of cells and relative oscillation frequency. Reference [11] includes the study of phase noise in oscillator. This paper shows the phase noise dominates the amplitude noise and thus discussed the phase noise in detail. A comparative study of phase noise on various types of oscillators is shown in [10]. Taiwan semiconductor manufacturing company (TSMC) fabricated the three oscillator circuits. These are simple five stage ring oscillator, current starve nine stage ring oscillator and LC cross coupled oscillator. The various results among frequency, phase noise, power dissipation and offset frequency is shown.

For the application of ultrasound transmitter a wide tuning range VCO is presented in [9]. It is voltage controlled oscillator based on inverter delay cells which uses the current starve topology. Each stage of oscillator is studied and equivalent frequency and delay equations are calculated. It uses the higher power supply that is 5V. The power supply is quite high but it is necessary because of the need of circuit to work on higher frequency. Due to these parameters the power dissipation of the reference [9] paper is high. Circuit oscillates in the range 240-407MHz.In [8] a wide tuning range 69GHz VCO is designed in colpitt structure. The power dissipation by the circuit is 27.52mW. Although it is a high frequency tuning range VCO but its phase noise is too poor. The measured phase noise is -76.23dBc/Hz at 1MHz offset. Phase noise in ring oscillators and expression of phase noise is discussed in [7].In [7] link between phase noise and jitter is discussed.

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III. PROPOSED VCO

The five stages proposed ring oscillator consists of five delay cell cascaded and output is then feedback to the input of first stage. Control voltage from 0V to 1V is provided by dc voltage source. Control voltage is directly feed to the pass transistor NMOS M4 (see in Fig. 4). Vin and Vout are the two single ends of the unit delay cell and thus all the five stages are connected as shown in Fig. 3. The proposed pass transistor VCO block diagram is shown in Fig. 4. This VCO is fully design in cadence UMC .18µm CMOS technology. The supplied Vdd is 0.8V and the Vss is -0.8V.

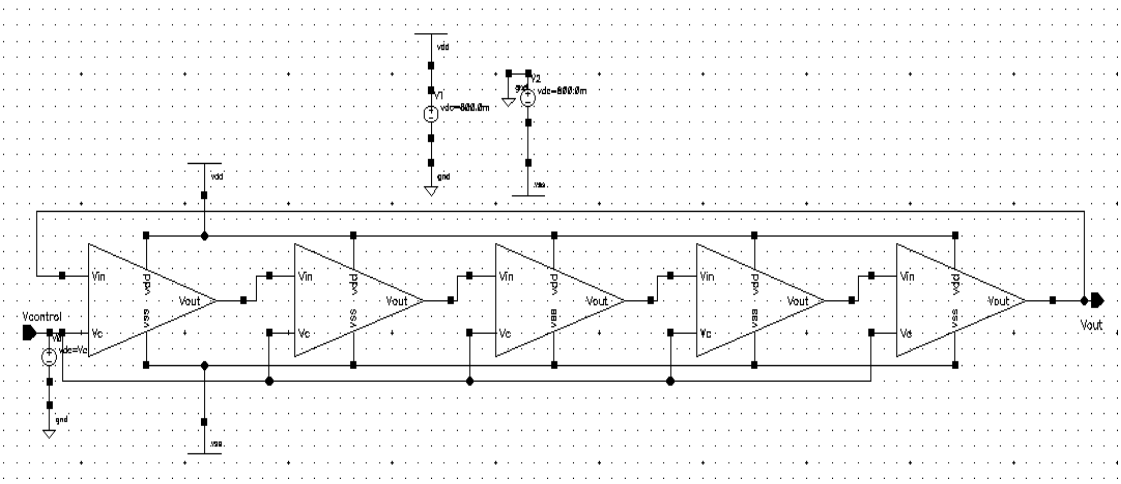

Fig. 3 Proposed Five stage single ended ring oscillator block diagram

Figure 4 shows the schematic diagram of the five stage VCRO. The circuit is designed such that the rise and fall time is equal and gives the better transient performance. The oscillation frequency can be calculated by calculating each delay cell's delay time (t).

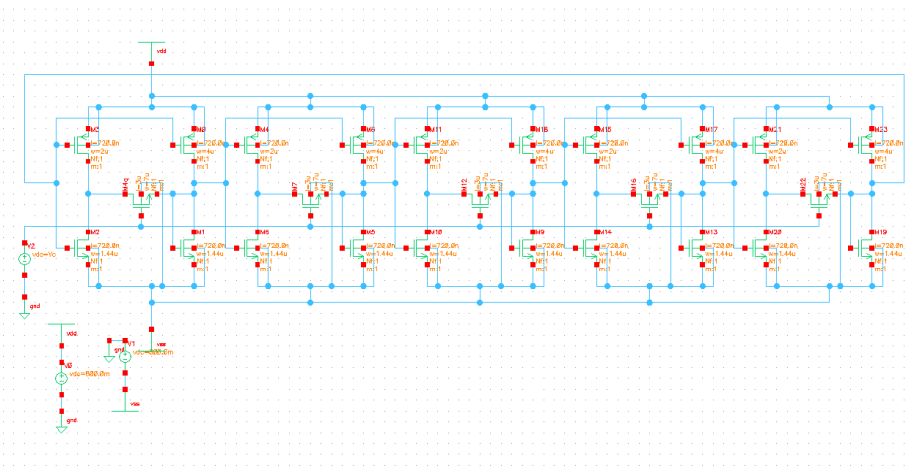

Fig. 4 proposed five stage single ended ring oscillator circuit diagram

Oscillation frequency can be given by f = 1/ 2Nt [3][4]. Here N is the number of delay stages and t is the delay time of each delay cell. Cadence CMOS UMC .18µm technology is used to simulate the VCO. The delay cell consists of five CMOS. The inverter is followed by a NMOS (pass transistor) to control the frequency. The output frequency is directly proportional to the change in control voltage. The two other NMOS and PMOS connected are to reduce the phase noise and to increase the oscillation frequency. The oscillation frequency is increased due to current reuse.

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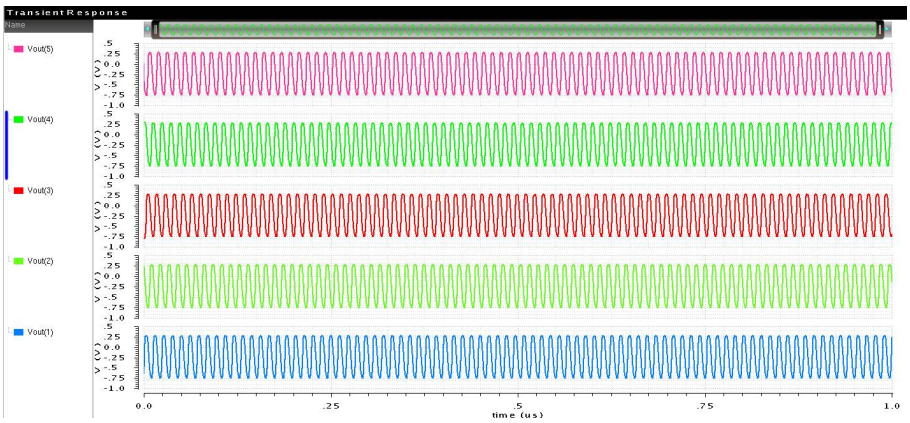

Fig. 5 Transient output of each delay cell

The transient outputs of the proposed VCO are shown in figure 5 and figure 6. Fig. 5 shows the transient waveform of each five delay cell output. Each output of the delay cell is delayed by certain value and thus the final time delay of the overall circuit is Td = N×t .Where N is the number of delay cells and t is the time delay of each stage. Figure 6 shows the transient output of the final (fifth delay stage output) delay stage.

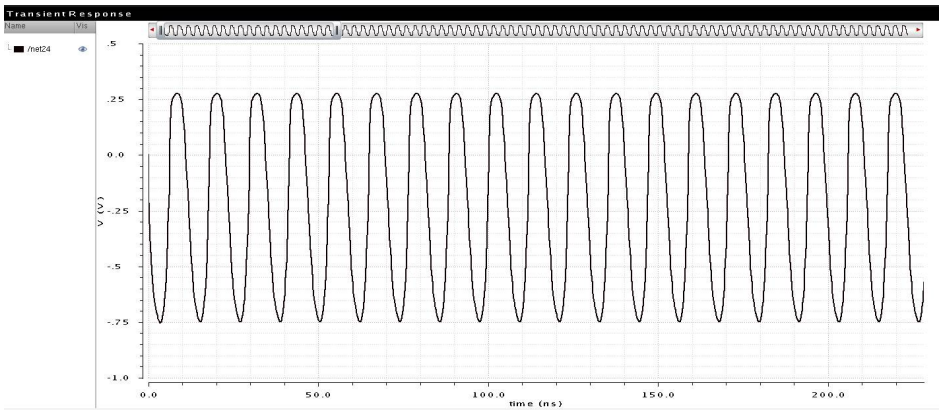

Fig. 6 Transient output of VCRO

IV. SIMULATION RESULTS

The simulation resultsobtained by us areDC, Transient, PSS and phase noise analysis. We have designed the unit cell with inverter single ended delay cell followed by an active resister to increase the oscillation frequency and to reduce the phase noise. Proposed circuit dissipates less power than the referenced circuit [2]. This delay cell is basically designed for the FM radio transmission range frequency oscillation which is from 88MHz to 104MHz. For the application of this frequency range we have designed the proposed circuit in 71MHz –112MHz. In other words the five stage oscillator will have the frequency range from 71MHz to 112MHz. Simulations such as periodic steady state analysis (PSS) are done on spectreRF. The proposed circuit is linear along the required frequency range.Ring oscillator must satisfy some of the specifications such as a better phase noise with a linear Vc (control voltage) verses frequency characteristics. It can be seen that the proposed five stage VCO gives full swing. Figure 7 shows phase noise of the designed circuit. At various control voltage the frequency and its corresponding phase noise varies.

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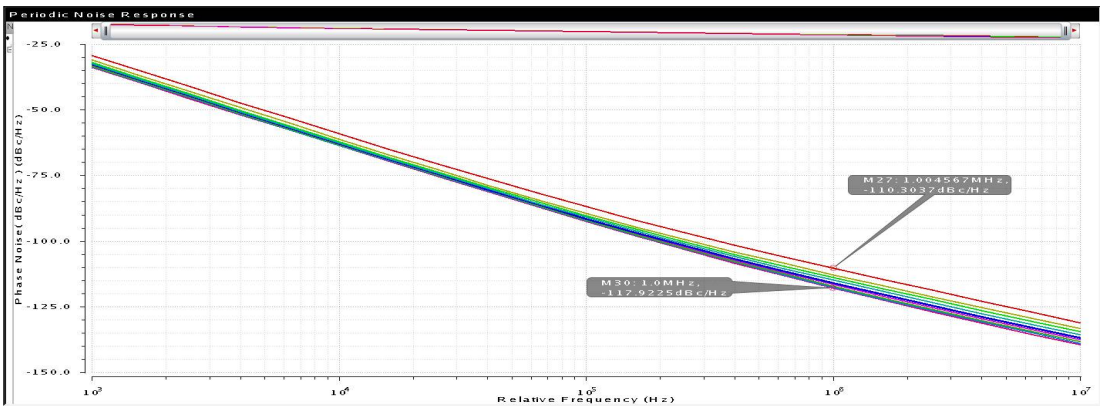

Fig. 7Phase noise at various Vc (Control voltage)

The phase noise at 1MHz offset is calculated by is -117.92dBc/Hz. The phase noise variations according to the control voltage can be seen in figure 7. Figure 8 shows the Frequency voltage characteristic of the designed VCRO. It can be seen that the Frequency voltage curve is linear and can be used for various applications. The control voltage varies from 0V to 800mV and at this control voltage band the frequency tuning range varies from 71MHz-112MHz.

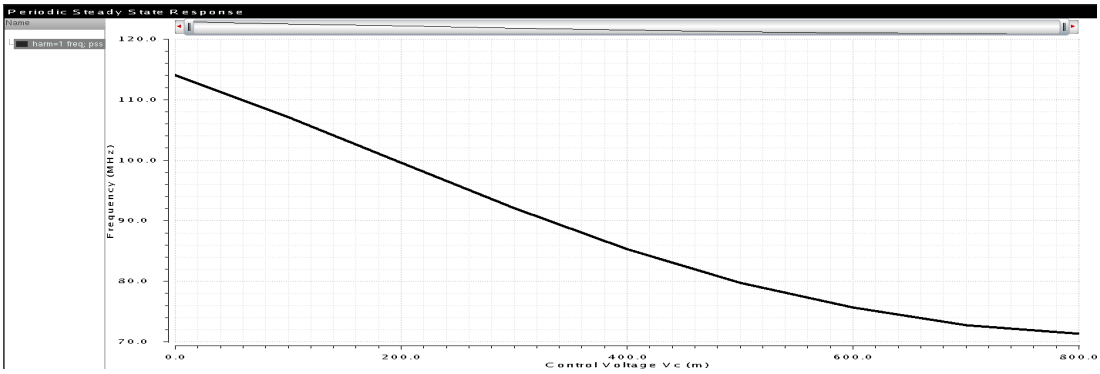

Fig. 8Frequency verses control voltage curve

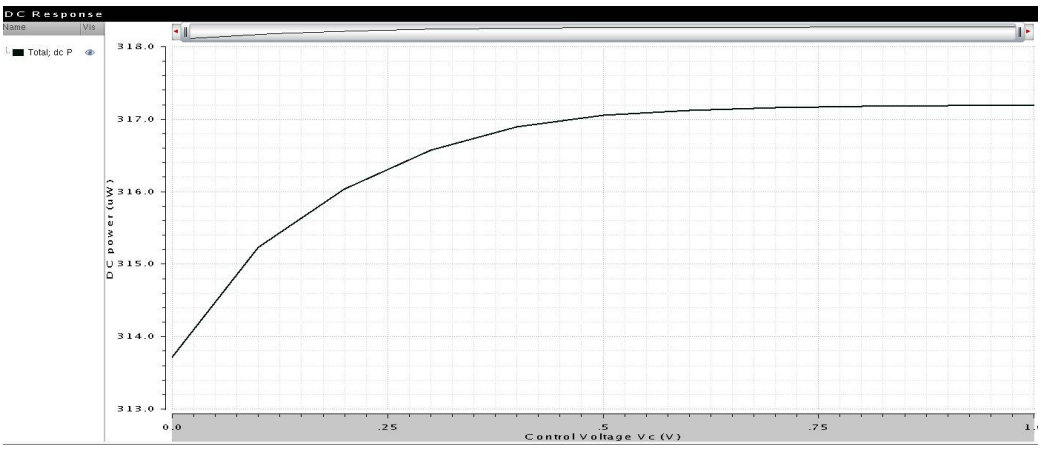

Fig. 9Power dissipation curve

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Power dissipation at various control voltage is shown in figure 9. At control voltage equal to 0V the power dissipation is around 313µW and at highest control voltage that is at .8V the power dissipation becomes saturate at 317.2µW. It can be seen from the result that the proposed design is a low power voltage control ring oscillator design. Table 1 shows comparison of proposed VCO parameters to the referenced parameters. The designed VCO is quite good in frequency, power dissipation and phase noise parameters. It can be seen in the Table 1.

Parameters	This work	Low Voltage VCO [2]	Low phase noise Oscillator [5]	Current control Oscillator [8]
Oscillation Frequency	71MHz-112MHz	12.6~48(MHz)	1~25 (MHz)	1~25 (MHz)
Supply Voltage	0.8 V	1.2 V	2 V	2V
Technology	0.18 µm CMOS	0.18 µm CMOS	0.35 µm CMOS	0.35 µm CMOS
Power Consumption	317.2 µW	1.2 mW	-	-
Architecture	Single Ended	Single Ended	Differential (3 stage)	Differential (3 stage)
Phase noise	-117.92 dBc/Hz	-109.38 dBc/Hz	-	-
Output phase	5	4	6	6
Control Mechanism	Voltage control	Voltage control	Voltage control	Current control
Control voltage	0V-0.8V	0V-1.2V	0V-2V	0V-2V

Table 1comparison table of various parameters

It is seen that there is trade-off between frequency and phase noise. If the number of delay stages is increased the phase noise is reduced. But at every increase in the delay cell the frequency became extremely decreases. If we want to work with specific kind of frequency then we have to compromise with the phase noise and wise versa. Taking about power dissipation, it is also increases as the stage are increasing. Therefore there should be as minimum stages as possible.

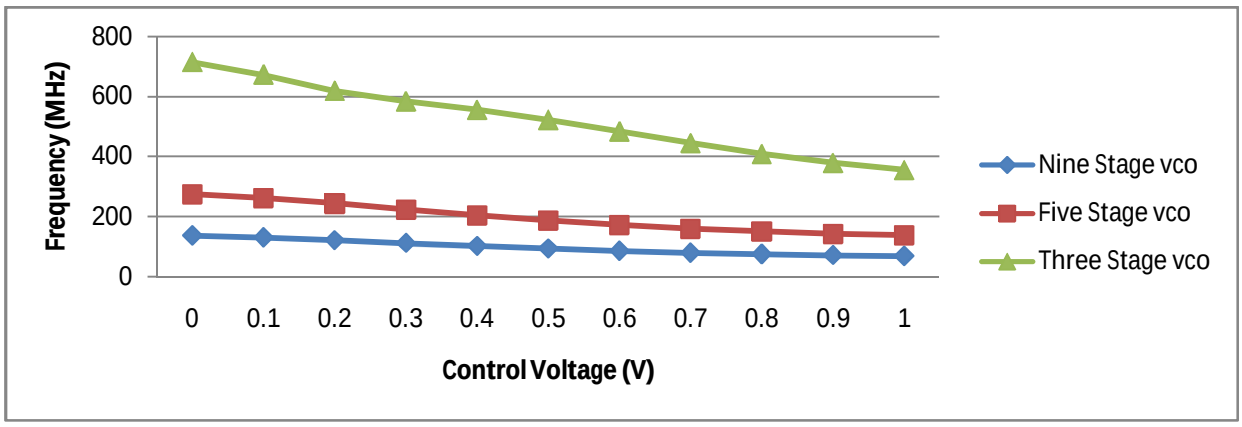

Fig. 10comparative analysis of the Kvco curve at different number of delay cells

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For the optimization of the phase noise, power dissipation and the frequncy range we have used the five stage delay cell structure. The comparative analysis of the frequency verses control voltage at different number of delay cells can be seen in the figure 10. Figure 10 shows the relative results and that is why there is difference of phase noise in each type of delay stage design VCO topology. But we have optimised the sizing of all CMOS and observed that five stage ring oscillator can be work at lower phase noise and good frequency range.

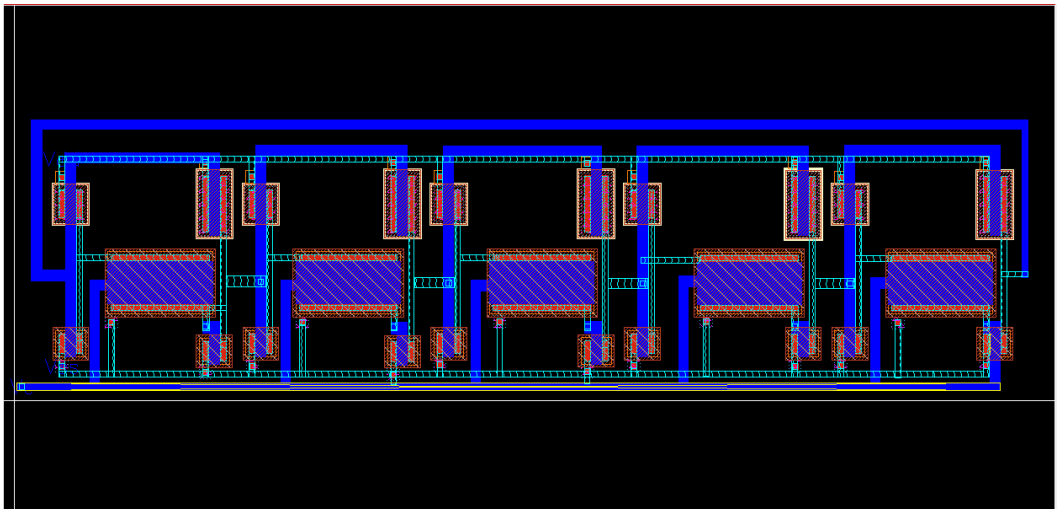

Fig. 11Layout of five stage ring oscillator

V. CONCLUSION AND FUTURE WORK

The simulation results shows that the designed CMOS VCRO noise is good compared to the other VCRO and thus we can use this oscillator in various applications such as FM radio telecommunication. Apart from the noise the designed VCRO is a low power dissipation oscillator. The proposed design supports us to use these two parameters efficiently and thus maximizes the figure of merit.As the performance of the proposed VCRO is analyzed between different numbers of stages, so in future with some modifications in design considerations the performance of the proposed VCRO can be Increase. We have used the pass transistor delay cell, as the type of frequency tuning and number of stages change, the complexity and the performance will change. We can increase the number of stages to improve phase noise but the frequency of oscillation will decrease.

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BIOGRAPHY

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