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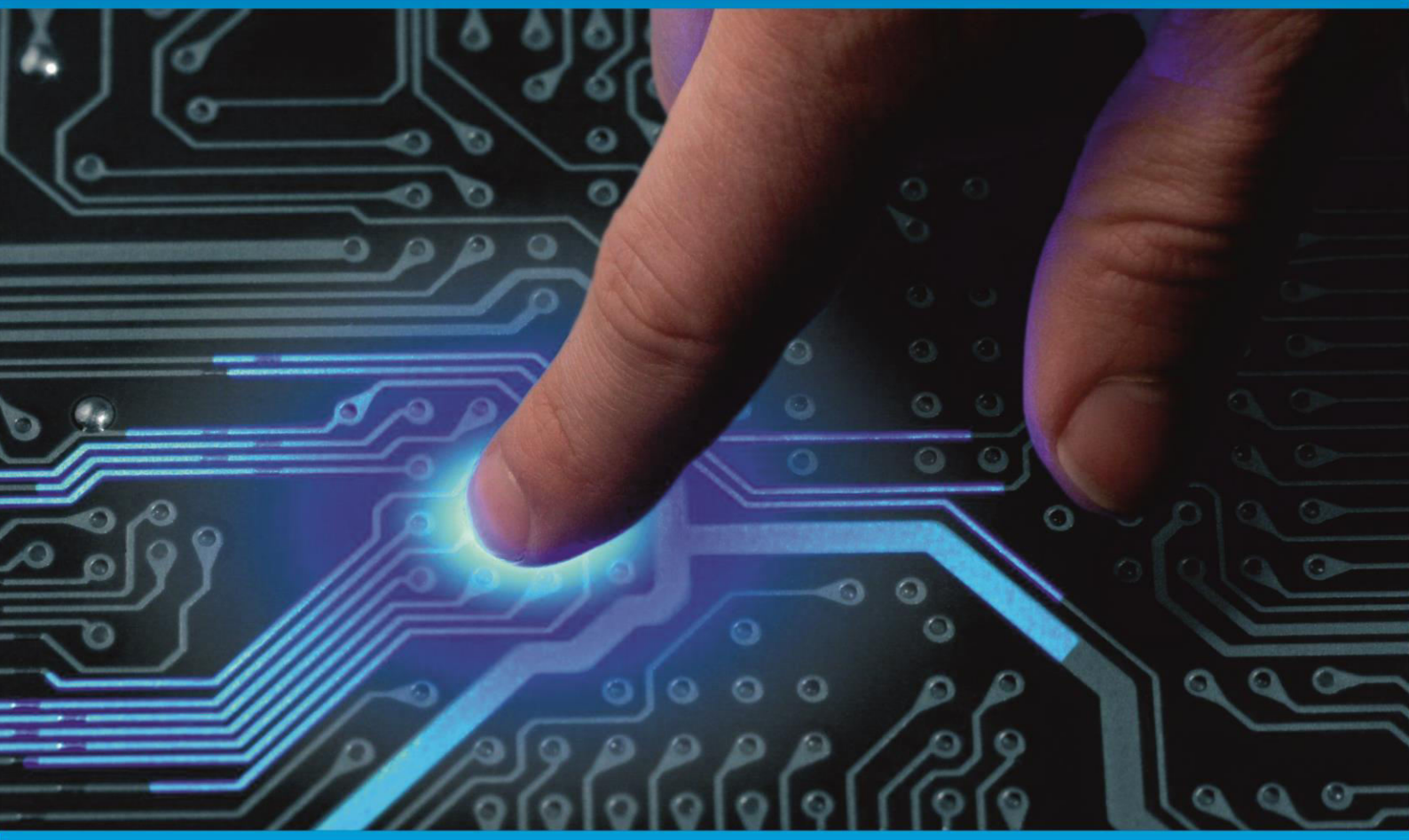

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A Power and Speed Energy Efficient RoBA Multiplier with MAC Unit

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ABSTRACT: In this paper, we design an approximate multiplier that is high speed yet ,less complex energy/power efficient. The approach to round the operands to the nearest exponent of two. This way the computational intensive as part of the multiplication is omitted improving speed and energy consumption at the price of the small error. The proposed approach is applicable to the both signed and unsigned multiplications. We propose three hardware implementations of the approximate multiplier that includes one for the unsigned and the signed operations. The efficiency of the proposed multiplier has evaluated by comparing its performance with those of some approximate and accurate multipliers using different design parameters. In addition, the efficacy of the proposed approximate multiplier is studied in two image processing applications, i.e., image sharpening and smoothing

KEYWORDS: accuracy, approximate computing, energy efficient, high speed, multiplier r

I. INTRODUCTION

High speed,low power consumaption energy minimization one of the main design requirements in almost any electronic systems, especially the portable such as smart phones, tablets, and different gadgets. It is highly desired to achieve this minimization with minimal performance (speed) penalty. Digital signal processing (DSP) blocks are key components of these portable devices for realizing various multimedia applications. The computational core of these blocks is the arithmetic logic unit where multiplications have the greatest share among all arithmetic operations performed in these DSP systems. Therefore, improving the speed and power/energy-efficiency characteristics of multipliers plays a key role in improving efficiency of processors.

High speed, low power consumption & low area are the main the main parameters in any electronic applications like DSP, ASIC & FPGA. Power efficiency & high performance can be obtained by approximate computing & it can also decrease the design complexity. A multiplier one of the key hardware blocks in most of the DSP systems. Typical DSP applications where a multiplier plays an important role. Now a days electronic devices are portable, so power dissipation is one of the main concern .since multipliers are rather complex circuit and operates at high system clock rate, reduces the delay of multiplication. In this paper, we pay attention to develop a high speed, low power & less complex approximate multiplier which withstands the error. This approach is called as rounding based approximate multiplication. It is workable for both signed & unsigned values.

1) Developing a new method of multiplication to improvising the typical multiplication approach.
2) It is workable for both signed & unsigned operations.

PROPOSED SYSTEM

- The concept approach the rounding operands to the nearest exponent of two.
- In this we implement to both signed and unsigned multiplications.
- let us denote the rounded numbers of input of *A and B by Ar and Br*
- Hence, to perform the multiplication process, and the following expression is used:

$$A \times B \sim= Ar \times B + Br \times A - Ar \times Br .$$

- Thus, the operation can be using three shift and two addition/subtraction operations

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BLOCK DIAGRAM:

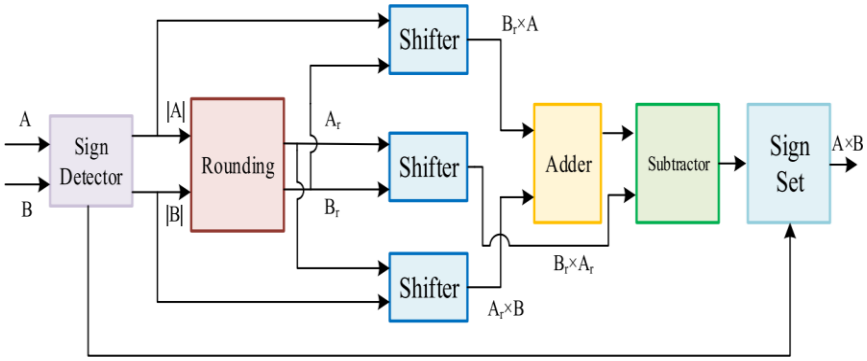


Fig.a. ROBA MULTIPLIER

WORKING PRINCIPAL

1 Sign detector

The Sign Detector detects the sign of the input values & gives the output. It extracts the most significant bit(MSB) of the input value. If the MSB of the input is '0', it will be considered as positive & it will MSB value is '1', it will be regarded as negative.

3.1.2Rounding

This block rounds off the input values to the nearest exponent of two. In the proposed method Z[i] is one in the following cases: In the first case, Z[i] is one and all the left sided bits are zero while Z[i-1] is zero. In the second case, whenZ[i] and all the left sided bits are zero, z[i-1] and z[i-2] are both one. Here we are using three barrel shifter blocks, the products Ar × B, Br × B, Ar × Br are determined. These input bits are shifted towards leftside.

3.1.3 Adder

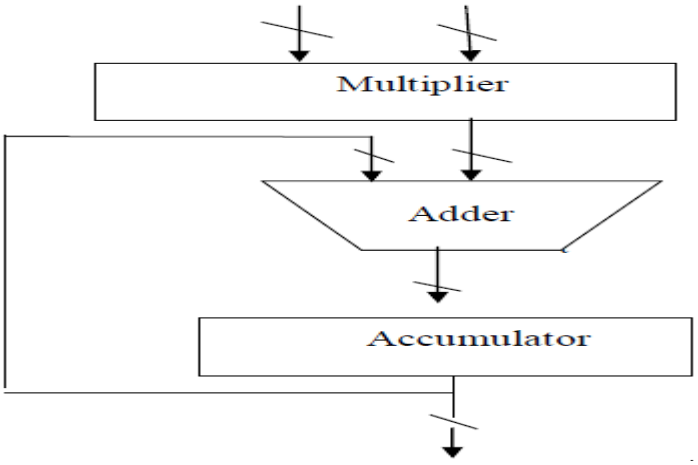
Parallel-Prefix adders perform parallel addition i.e. most important in microprocessors, DSPs, mobile devices and other high speed applications. Parallel- Prefix adders are primarily fast when compared to the adder. Calculation of carries Gi:j = Gi:k +Pi:k . Gk-1: Pi:j = Pi:k .Pk-1:j

Simple adder to generate sum

Si = Pi ⊕Gi-1:0

3.1.4 Sign Set

The main function sign set block is to set the sign the final of the multiplication result



A. Multiplier

- Two numbers are multiplied together, and added into an accumulator register. The basic MAC unit consists of multiplier, adder and accumulator. In general MAC unit the conventional multiplier unit.
- The proposed MAC unit in to enhance the performance of MAC using ROBA Multiplier to get the final result of the multiplication.

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B. Accumulator

- The Accumulator basically consists of register and adder. Register hold the output of previous clock from adder.
- Holding outputs in accumulator register can reduce additional add the instruction. An accumulator should be fast in response so it can be implemented with one of fastest adder like carry look ahead adder or carry skip adder or carry select adder.

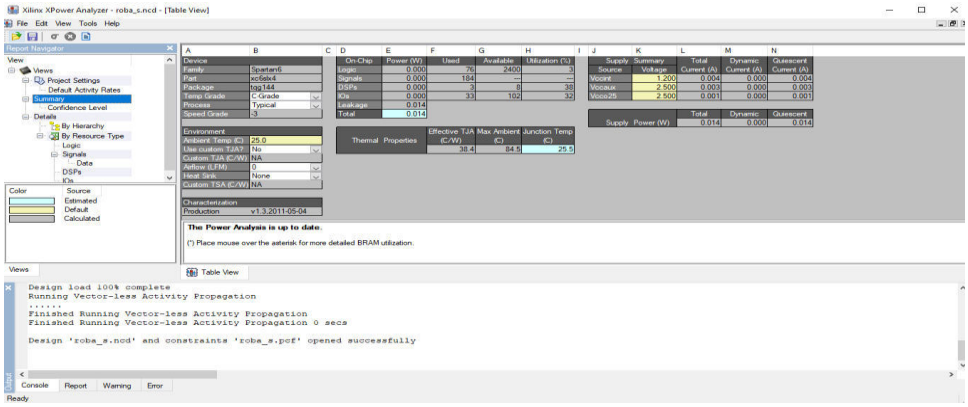
II. COMPARISION

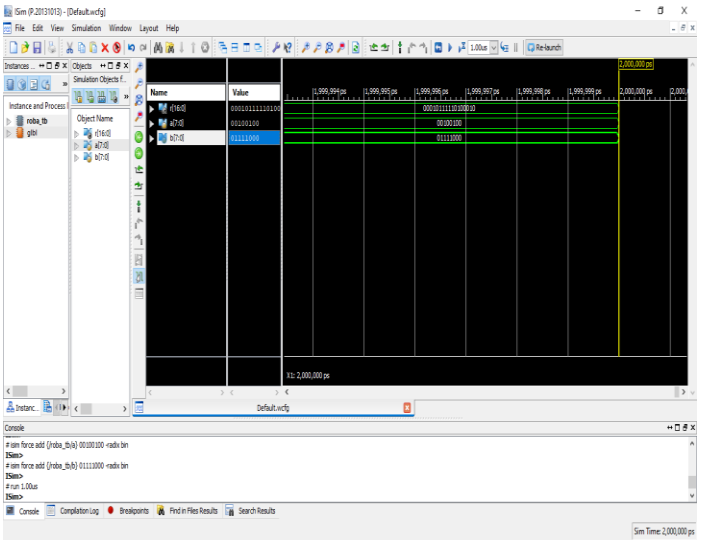
Parameter	ROBA	ROBA with MAC
Time	18.408ns	11.524ns
Power	13.68mw	13.69mw

III. APPLICATIONS

- ❖ Image sharpening
- ❖ Image smoothing

IV. RESULT





ROBA MULTIPLIER

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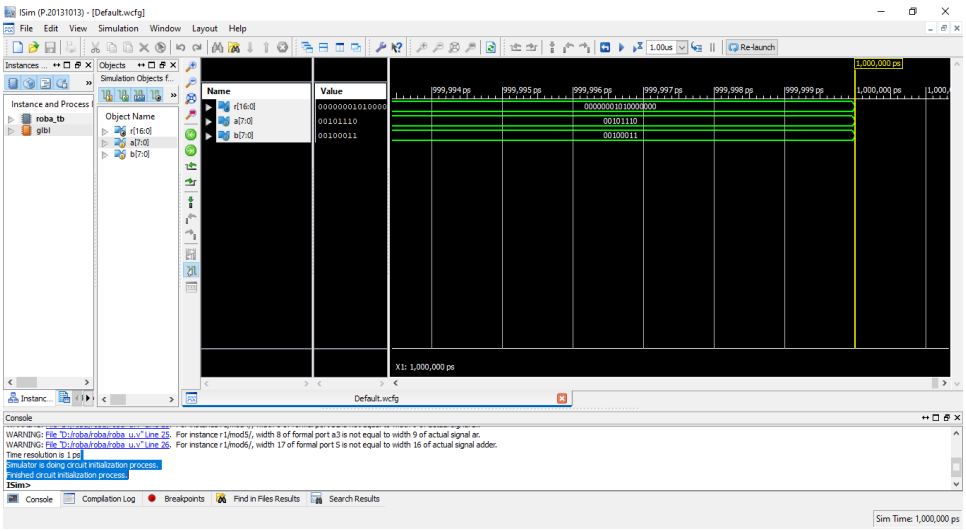

MAC UNIT

V. FUTURE SCOPE

- Han caulson adder
- FIR Filter

VI. CONCLUSION

In this project, we have proposed a 64 bit RoBA Multiplier with MAC unit which improves speed, decreases power consumption and low area. The implemented method is based on the rounding off the input values to the nearest exponent of two. The proposed approximate multiplier has high accuracy when compared. RoBA with MAC implementation provides low area, less delay and power in order to meet the current needs of the VLSI Industry. This approach is applicable for both signed and unsigned operations. In future, it can be used in various image processing applications.

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