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Designing and Implementation of Charge Pump for Fast-Locking and Low-Power PLL

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ABSTRACT : This design of wide band VCO used in PLL system which is suitable for wide range of application. PLL's with high speed, low noise and wide tuning range are preferred . Ring oscillators consist of odd number of inverter stages in order to avoid latch up and we have considered 5 stage current starved VCO with tuning range from 431.68MHz –1.5GHz . We have considered one more VCO design using Operational Transconductance Amplifier (OTA) tuning range from 271.2MHz –3.1GHz consist of OTA stage ,inverter stage and Biasing circuits . The circuits are simulated at schematic level and layout level using180nm technology with supply voltage 5 voltage

I. INTRODUCTION

PLL is used to recover a signal from a noisy communication channel, generate stable frequencies or distribute clock timing pulses in microprocessors. The PLL based frequency synthesizer plays a very significant role in direct frequency modulator, frequency demodulator and the regeneration of the carrier from the input signal in the wireless communications. PLL is used for clock and data recovery circuit in the broadband data communication network, which is used to recover the data from the NRZ clock and data re-timed decision.

II. PHASE LOCK LOOP DESIGN

BASIC PLL CIRCUIT

A PLL is a feedback system that compares the output phase with the input phase. The comparison is performed by a 'phase comparator' or 'phase detector'. The basic elements of a Phase locked Loop (PLL) are a Phase detector (PD), Low Pass Filter (LPF) and a voltage controlled oscillator (VCO) in a feedback loop.

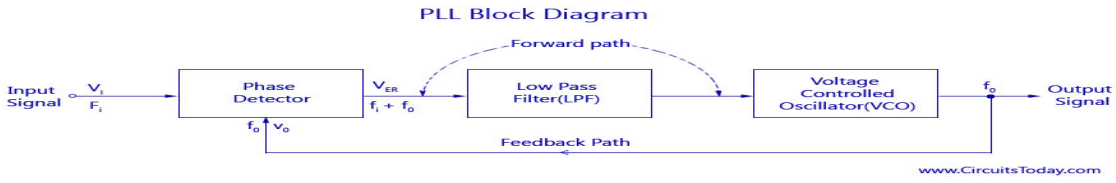

Fig. 1: Basic Block Diagram of PLL

The role of Phase detector is to compare the phase of Vout and Vin and then generating an error. Thus PD detects a phase error between the reference signal and the output signal of PLL. And the error detection range can be extended with PFD. The input phase errors are detected by Phase-Detector (PD) or Phase - Frequency Detector (PFD). These errors (phase or frequency errors) are converted into current or voltage to control the output frequency of Voltage Controlled Oscillator (VCO) by charge pump in a charge - pump PLL

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PHASE FREQUENCY DETECTOR CIRCUIT DESIGN

For the periodic signal it is possible to merge the phase and frequency detector, such that it can detect both phase and frequency. It is called as phase-frequency detector (PFD).

The PFD is shown in figure 3.2

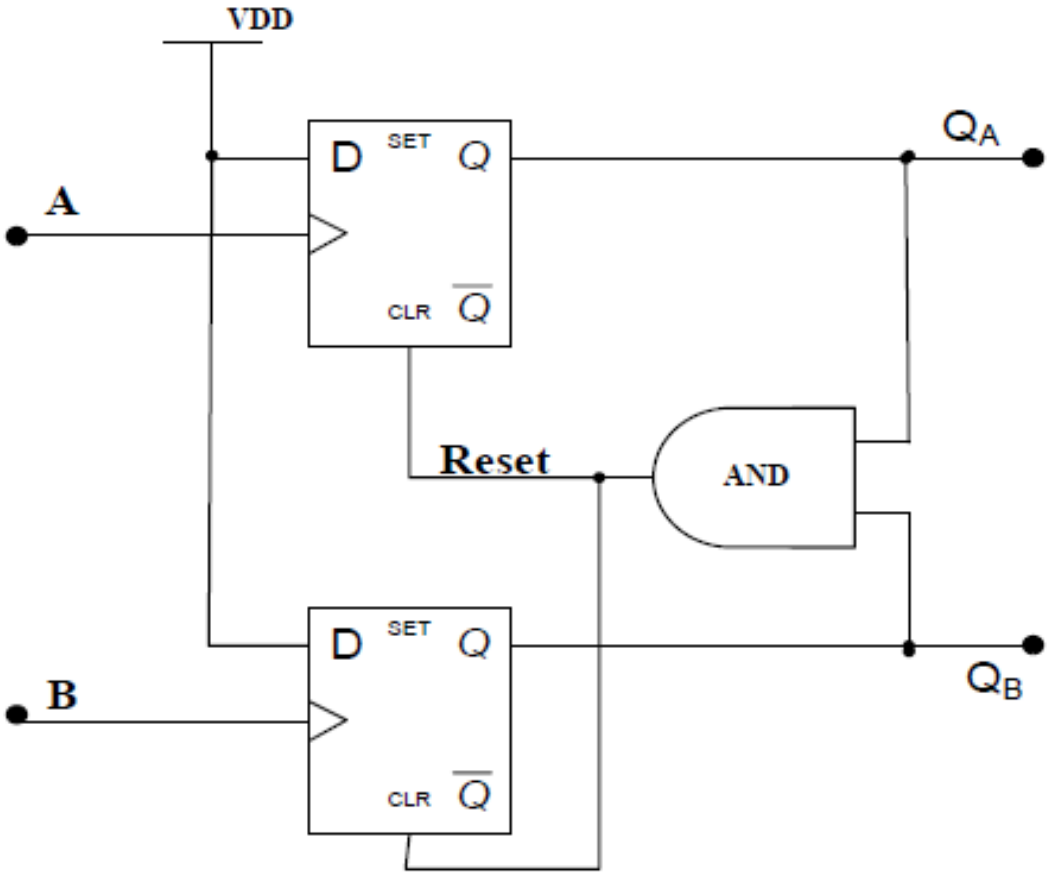

Fig. 2 Implementation of PFD

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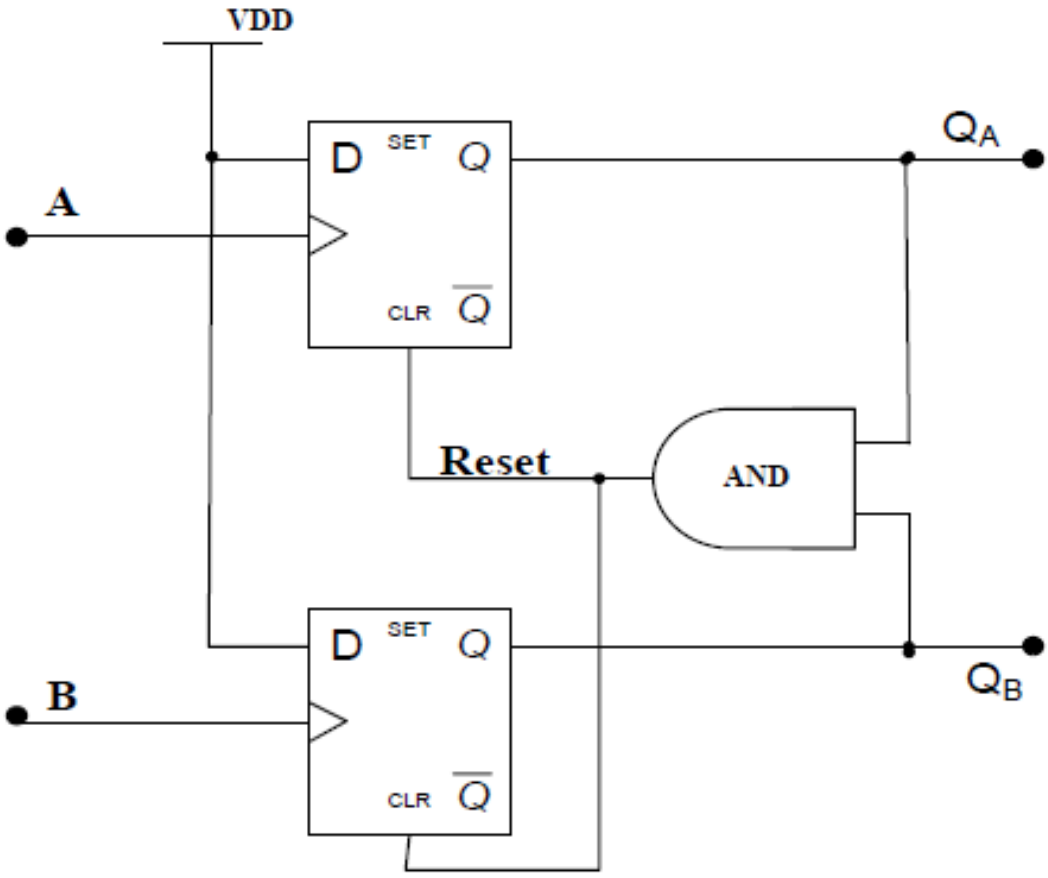

Fig. 3 Implementation of PFD

Design of Phase Lock Loop

These design criteria are often I conflicts and improving one particular aspect of the design constrains the other. So each sub block of PLL has been designed in this chapter to satisfy all these properties.

Thus the basic block of PLL consists of five fundamental blocks, namely, PFD, CP, LPF, VCO and FD. The proposed PLL is designed to achieve the following properties

. Reduced locking time
. Low power dissipation
. Delay reduction
. Transistor Count

Pull up and Pull down Charge Pump

This kind of charge pump circuit is designed for increased output voltage with reduced current mismatch. This type of charge pump circuit is divided into two pats namely, pull up network and pull down network as shown in figure 4.5. The UP signal is applied to the pull up network and DN signal is applied to the pull down network.

When the signal UP is high, P1 and P2 both are OFF, and the current source I_1 drives P3.P5 is also ON because P3 and P5 from a current mirror structure. Thus the capacitor C will be charged by the current source I1and the output voltage is increased At this time DN signal is low, so the pull down network is OFF. When the UP signal goes low, then P1 and P2both are ON. The current in P1 is sum of current in P1 and I1. Now the current in P3 and P5 are so small that they

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are negligible. At this condition the capacitor holds the previous charge and the output voltage remains at its original value. When the UP signal is again switched from low to high then P4 and N1 will be ON. These P4 and N1 are used to reduce the charging time delay of P3. When DN signal is high, then the pull down network is ON and capacitor C will be discharged. When they are both ON, they operate in the saturation region.

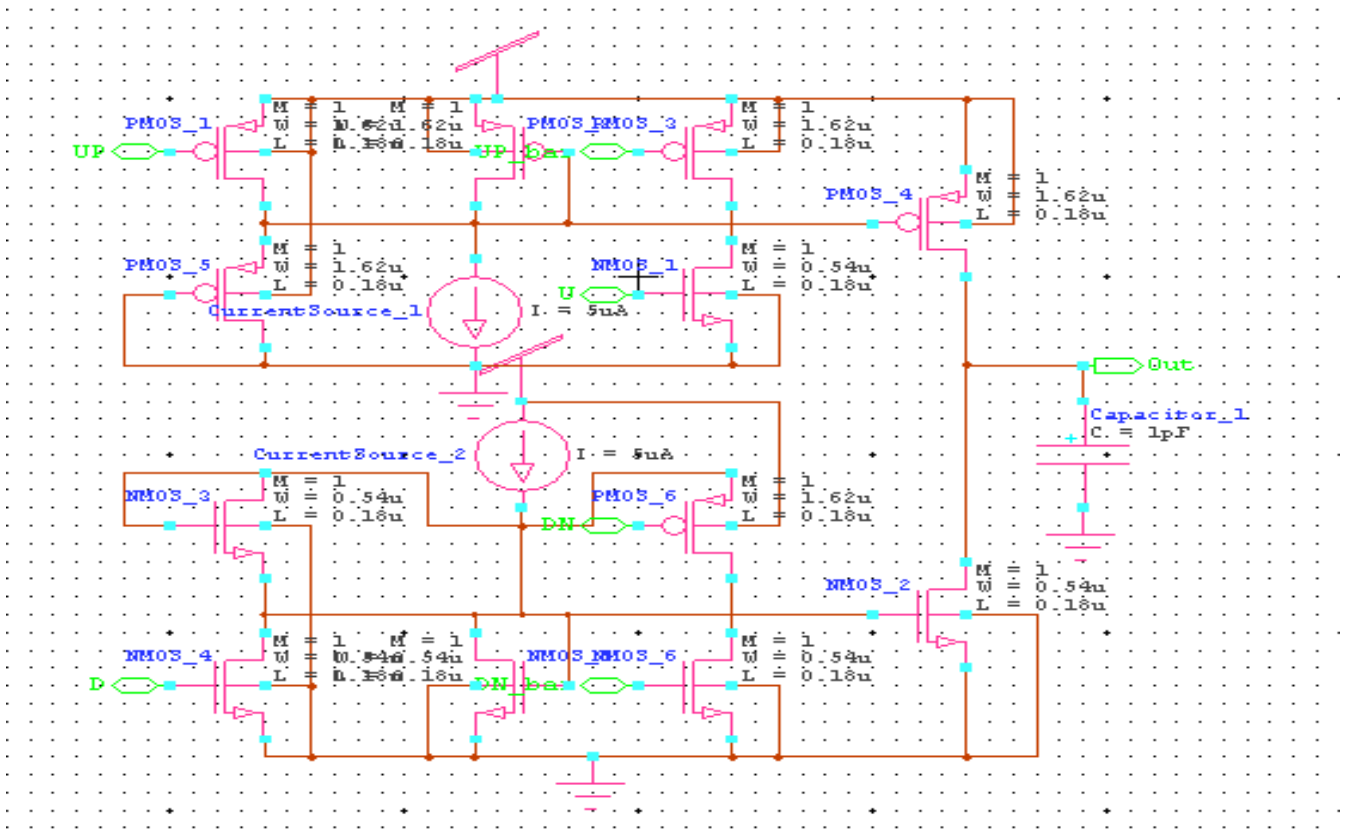

Fig. 4 Schematic of Pull UP and Pull DN charge pump

The current mirror structure is used in this circuit, so current mismatch is minimized. This charge pump also has increased output voltage but the power dissipation is again high. So another charge pump is designed to achieve both the properties of increased output voltage with low power dissipation.

III. SIMULATION RESULT

2Charge Pump

The proposed current mirror charge pump is designed and simulated using fully current mirrored structure for perfect current matching between source and sink. The simulation waveform of the current mirror charge pump at a supply voltage of 1.0 V, is shown in the figure 5.3.

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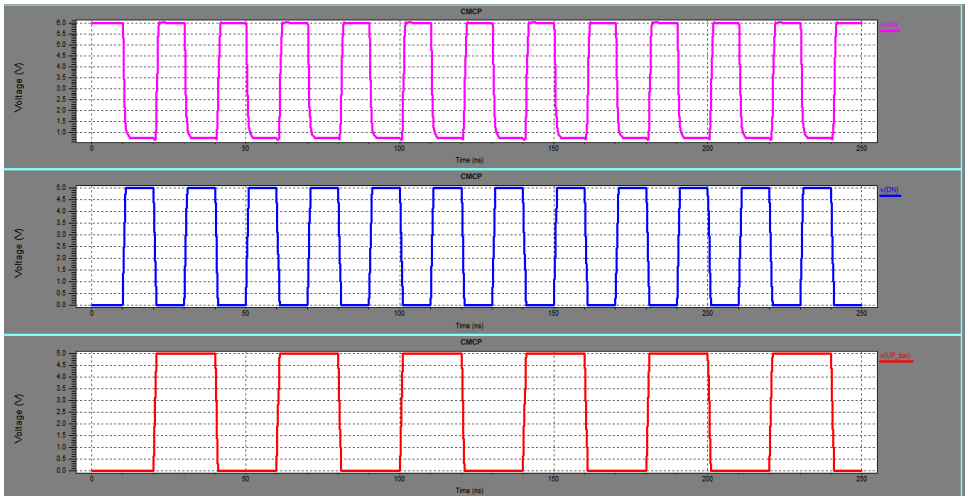

Fig.5Simulation waveform of current mirror charge pump

IV. CONCLUSION

The present work studies the important charge pump and PLL architectures and their performance. In this project, a high speed CMOS sense amplifier for PLL application has been designed and simulated using the 180 nm CMOS technology. Thus this project simulates and analyses some of the major reported sense amplifier architectures for fast locking and less transistor count compared with the design of PLL using charge pump.

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