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A Novel Low Power Vedic Multiplier using Modified GDI Technique in 45nm Technology

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ABSTRACT: In recent years, low power design has become one of the Prime focuses for digital VLSI Circuits. To cope up with the arising need, a novel low power Vedic Multiplier designs are proposed with less number of Transistors using Modified GDI technique implemented in 45nm process technology using CADENCE VIRTUSO. There is 75%(Design1) and 80.4% (Design2) reduction in power at 1Volt Supply w.r.t conventional Vedic Multiplier Designs.

KEYWORDS: Vedic multiplier; GDI(Gate Diffusion Input); Modified GDI Technique;

I. INTRODUCTION

Multiplier is an important building block in Digital Signal Processing, Microprocessors and in communications. Multiplication-based operations such as Multiply and Accumulate(MAC) and inner product are among some of the frequently used Computation- Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in microprocessors in its arithmetic and logic unit [4]. In Most DSP Algorithms execution time of multiplication is dominant which determines the instruction cycle time of DSP Chip [11]. In any system design, the three main constraints which determine the performance of the system are speed, area and power requirement. For High Speed Processors high Speed Multiplier is essential. The speed of multiplier determines the efficiency of the system as it is always a constraint in the multiplication operation. Increase in speed can be achieved by reducing the number of steps in the computation process. Multiplier Design involves 2 steps namely Partial Product Generation and Partial Product Addition. Integrating multiplication with Vedic Mathematics techniques results in the saving of computational time. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as sutras. Vedic Mathematics can be applied to computing and digital signal processing. Integrating Vedic mathematics for the multiplier design will enhance the speed of multiplication operation [12]. Several Designs are already been Proposed using Vedic Mathematics[5-6][11-12]. Vedic Multiplier Can be implemented with Adiabatic Logic[20], barrel shifters[8] and using Compressors[10]. In This Paper a Novel Low Power Technique will be proposed with Less Number of Transistors. With low number of transistors Less Silicon On-Chip area can be achieved.

Section II describes about Vedic Sutra. Section III describes about Multiplier Architecture and Modified GDI Technique. Section IV covers the simulation results of Proposed Vedic Multiplier, Comparison of Power consumption and Area with existing Vedic multiplier. Section V covers Conclusion.

II. VEDIC SUTRA- URDHVA TIRYAKBHYAM

Vedic mathematics employs 16 sutras (algorithms) [4]. Only Urdhva Tiryakbyham (UT) sutra has been discussed in this paper, which is implemented in the designing of faster and low power multiplier circuits. "Urdhva Tiryakbhyam" is a Sanskrit word. Urdhva means vertically and Tiryakbhyam means crosswise. UT is the general formula applicable to all cases of multiplication and also in the division of a large numbers by another large number. This sutra is one of the best sutras that provide an effective way to multiply the numbers that is applicable to many number systems. This sutra yields fast multiplication by generating partial product and sum terms in a single iteration step [3]. UT based multiplication for 2-bit numbers is illustrated using Fig 1.

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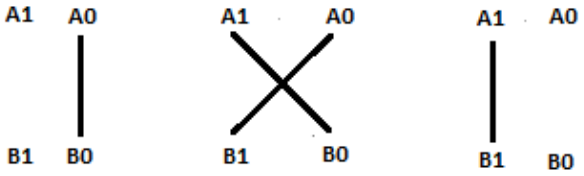

Fig. 1. 2x2-bit Multiplication using Vedic Mathematics

2×2 bit multiplication numbers involves following 3 steps

step1: A0 and B0 are mutliplied, which becomes the LSB bit.

Step2: The addition of (A0×B1) and (A1×B0) is performed. The LSB of this addition is placed to the left of A0B0 and the MSB is carry forwarded to the next stage.

Step3: Now the multiplication of A1 and B1 is performed and the carry is added to this term.

This approach performs addition and multiplication in single step therefore this multiplication scheme is fast [3]. This sutra can be extended for 4×4 bit and can be generalized for N×N bit multiplication. To understand the concept, the Block diagram of 4x4 bit Vedic multiplier is shown in Fig. 2 with each block implemented using 2x2 bit Vedic multiplier. First 2x2 bit multiplier inputs are A1A0 and B1B0. The last block is 2x2 bit multiplier with inputs A3 A2 and B3 B2. The middle one shows two 2x2 bit multiplier with inputs A3 A2 & B1B0 and A1A0 & B3 B2. So the final result of multiplication, which is of 8 bit,S7 S6 S5 S4 S3 S2 S1 S0.

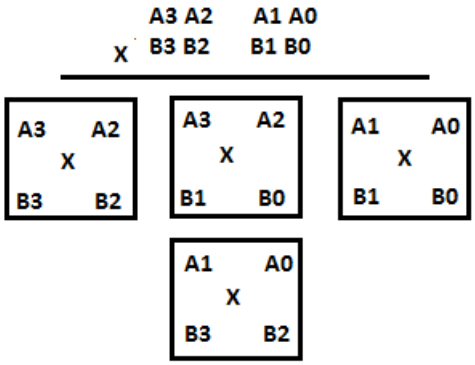

Fig. 2. 4x4-bit Multiplication using Vedic Mathematics

III. VEDIC MULTIPLIER USING GDI

Vedic Multiplication utilizes only logical AND operation, half adders and full adders to perform multiplication where the partial products are generated prior to actual multiplication. This saves a considerable amount of processing time. Moreover it is a robust method of multiplication. GDI technique is suitable for design of efficient low power circuits. It uses a reduced number of transistors as compared to CMOS. At the same time, it improves logic level swing and static power characteristics and allows simple top-down design by using small cell library. Realizing these functions using CMOS requires 6-12 transistors.But the same functions are very easy to implement using GDI method and require only two transistors per function. Basic GDI Cell is Shown in Fig3(a). Advantages of GDI technique are high throughput, low power consumption and low area as this technique reduces the transistor count. G, P and N are considered as inputs to the GDI Cell. G is the input applied common to the gate terminals of NMOS and PMOS. N input is applied to source/Drain of NMOS and P input is applied to the source/drain of PMOS. Applying different values to the inputs of

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basic GDI cell results in different logic functions. Despite of having many advantages with GDI its performance declines when used under 90nm.so Basic GDI Cell is Modified with Substrate terminals of PMOS and NMOS are connected to V_{DD} and GND respectively as shown in Fig.3(b)

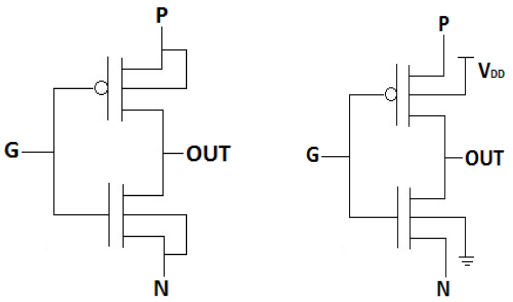

Fig. 3. *(a)Basic GDI Cell* *(b) Modified GDI Cell*

A. AND GATE using modified GDI

Previous Work AND Gate is Designed with 5T Transistors but with GDI Technique AND Gate can be constructed with only 2 Transistors as shown below by applying input A to G input and 0, B to P, N inputs respectively gives Output functioning as AND Gate

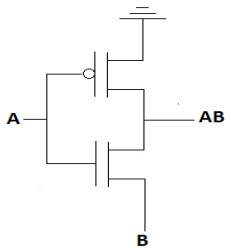

Fig. 4. AND Gate Implementation using GDI Technique

B. Half Adder using modified GDI

Half Adder can be constructed with 6 Transistors using modified GDI. Schematic of Half Adder is shown in Figure.5. This ensures High Speed and Low Power.

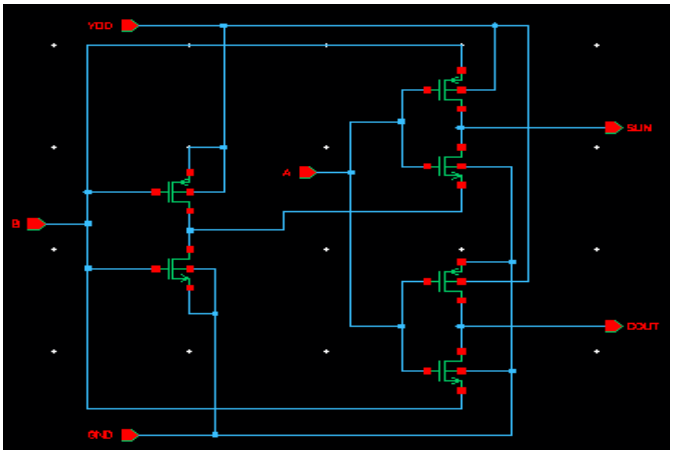

Fig. 5. Schematic of Half Adder Implementation using GDI Technique

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C. Full Adder using modified GDI :

Full Adder is an important Building Block of Multiplier. Already Several Full Adders are proposed but with less number of transistors [16]. But With modified GDI Technique full Adder is designed with 10 Transistors. Schematic of Full Adder is shown in Fig.6

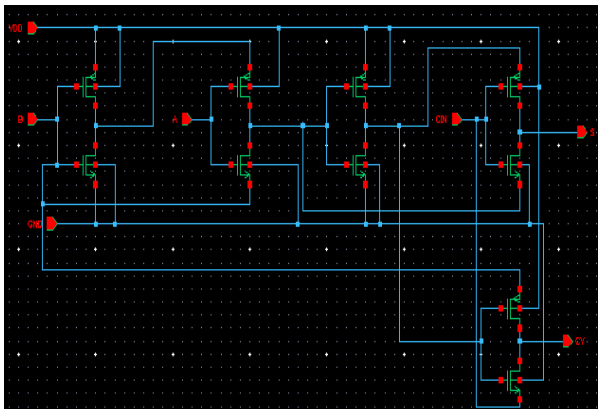

Fig. 6. Schematic of Full Adder Implementation using GDI Technique

D. 2-Bit Vedic Multiplier Architecture:

In implementing 2-bit Vedic multiplier, partial product generation requires 4 AND gates and 2 Half Adders for the required Addition process. Figure 7 shows the block diagram of 2X2 Vedic Multiplier. To Implement 2-bit Vedic Multiplier using modified GDI it requires 20Transistors. Figure 8 shows the Schematic of 2X2 Vedic Multiplier implemented using modified GDI

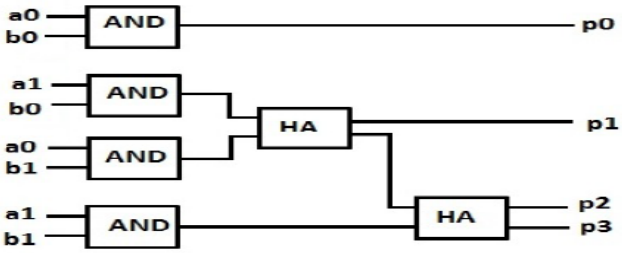

Fig. 7. Block Diagram of 2X2 Vedic Multiplier

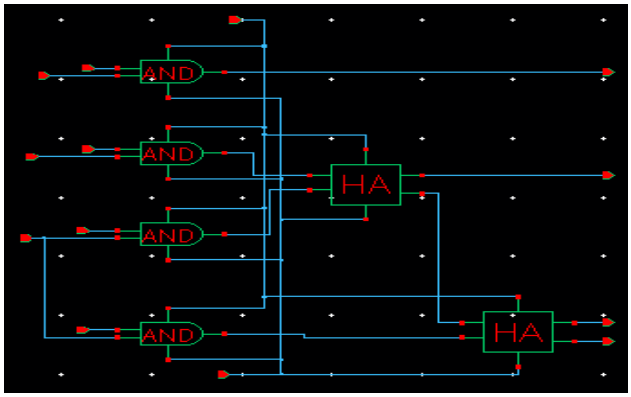

Fig. 8. Schematic of 2X2 Vedic Multiplier Implementation using GDI

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E. 4-Bit Vedic Multiplier Architecture (Design 1):

The Vedic mathematics based 4-bit binary multiplier can be realized using the Urdhva Tiryakbhyam sutra[1]. All the partial products are generated in parallel using a chain of AND gates. The addition of partial products can be accomplished by implementing several carry save adder arrangements and a final vector merging adder. The corresponding topology is given in Fig.9. Schematic implementation using modified GDI is shown in Figure.10 In The 4x4 Multiplier existing Design1 requires 228 Transistors but our proposed Vedic multiplier using modified GDI requires 136 Transistors out of which it requires 16AND Gates (32 Transistors) 4 Half Adders (24 Transistors) and 8 full adders (80 Transistors).

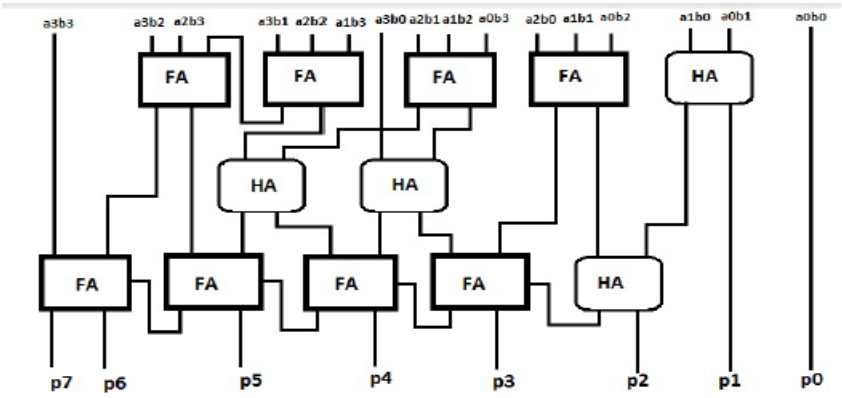

Fig. 9. Block Diagram of 4X4 Vedic Multiplier(Design 1)

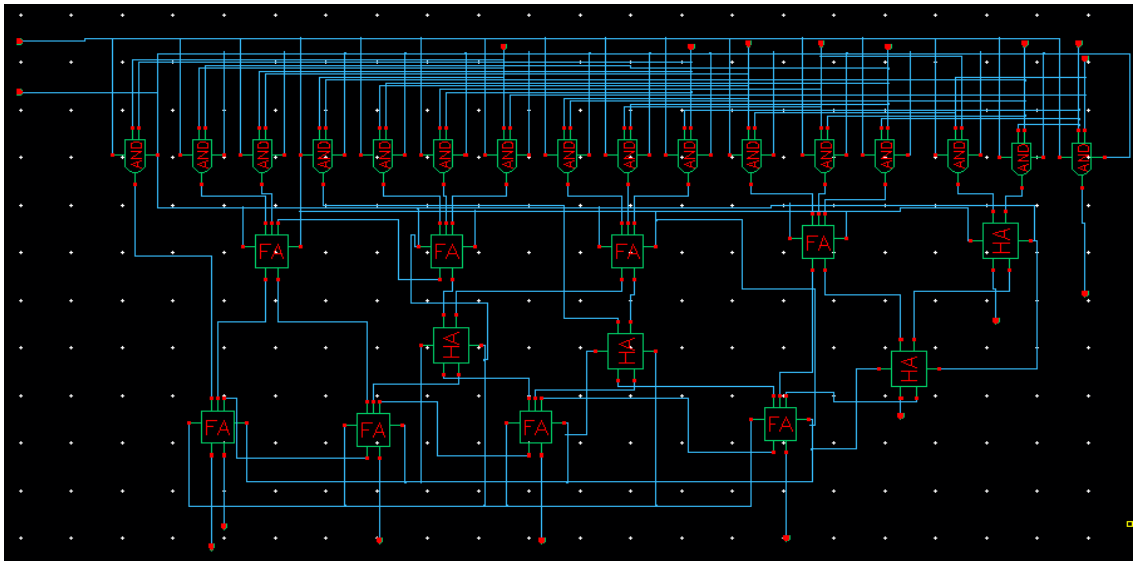

Fig. 10. Schematic of 4X4 Vedic Multiplier(design1) using modified GDI

F. 4-Bit Vedic Multiplier Architecture(Design 2):

The 4-bit binary multiplier can also be realized using 2-bit multiplier analogy as shown in Fig9. For Adding Partial products Carry Save addition is considered so that delay can be reduced. Existing Vedic Multiplier requires 320 Transistors but Design2 using GDI requires 200 Transistors. It requires four 2-bit Vedic Multipliers (80 Transistors),one Ripple Carry Adder(40 Transistors) and two carry Save Adders(80 Transistors).

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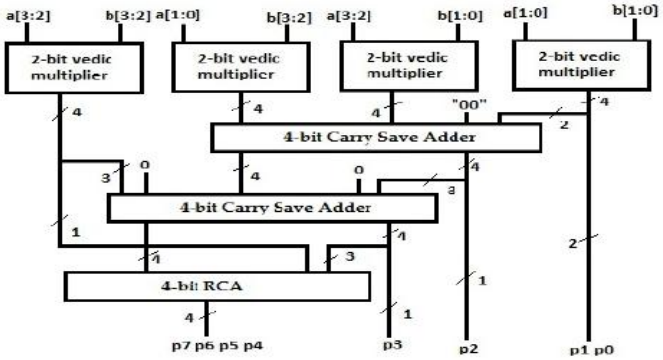

Fig. 11. Block Diagram of 4X4 Vedic Multiplier(Design 2)

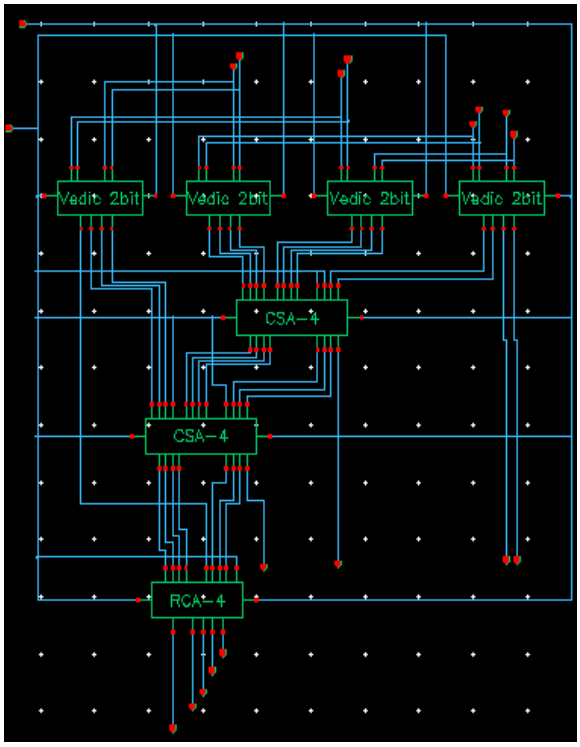

Fig. 12. Schematic of 4X4 Vedic Multiplier(design 2) using GDI

IV. RESULTS

Vedic Multipliers Designs are implemented and simulated using 45nm Technology in Cadence Virtuoso at 1V Supply. Power Consumption and Delay are calculated. Figure 13 and Figure.14 shows the Power consumption and Delay Comparison of Proposed Design with the existing Vedic Multiplier Designs. In Vedic Multiplier (Design1) using Modified GDI there is 75% and 53.9% reduction in Power Consumption and Delay respectively. In Vedic Multiplier (Design2) using Modified GDI there is 80.4% and 37.6% reduction in power Consumption and Delay respectively.

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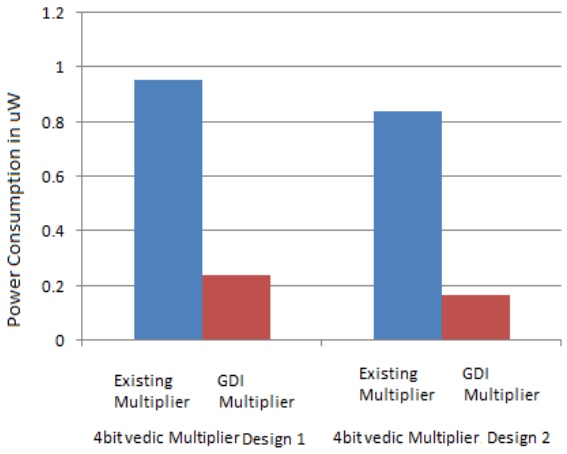

Fig. 13. Power consumption Comparison for proposed and Existing Vedic Multiplier

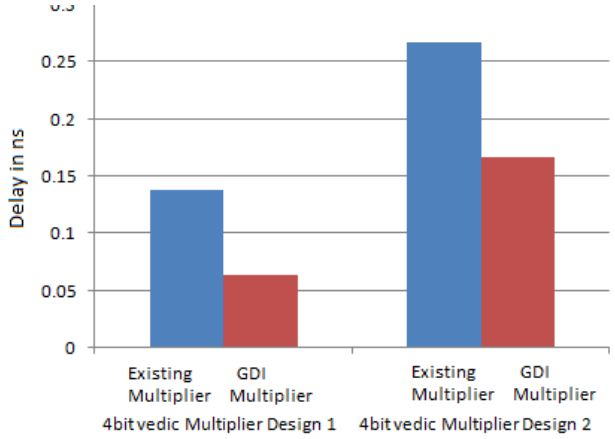

Fig. 14 Delay Comparison for proposed and Existing Vedic Multiplier

V. CONCLUSION

All the signal and data processing operations involve multiplication. As speed is always a constraint in the multiplication operation, increase in speed can be achieved by reducing the number of steps in the computation process. Vedic Multiplication involves less number of Steps. The speed of multiplier determines the efficiency of such a system. In any system design, the three main constraints which determine the performance of the system are speed, area and power requirement. Using Modified GDI Technique Low Power can be achieved with less number of Transistors. The 4-bit Vedic Multiplier Designs are implemented using Modified GDI technique implemented in Cadence Virtuoso in 45nm process technology. The results indicate performance is enhanced in terms of Power and Delay.

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