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Highly Efficient Reconfigurable FIR Filter Based on Modified Booth Multiplier Concept

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ABSTRACT: The two main challenging factors in VLSI design techniques are power and speed of the circuit. To optimize these to challenging factors, we have to minimise the delay of components like adders and multipliers used in the filter. This paper describes design of FIR filter using transpose form structure in a pipelined architecture with the reduction in delay and power consumption. In some applications the coefficients of FIR filters are not fixed, such filters are used for reconfigurable applications. In the proposed reconfigurable design, modified booth multiplier is used to increase the speed and also to reduce the area and power consumption. The proposed structure reduces the area, delay & power than the existing FIR structures.

KEYWORDS: FIR Filter, Transpose form Structure, Modified booth multiplier

I. INTRODUCTION

With explosive growth in the demand of portable computing and wireless communication systems, power dissipation is becoming an increasing concern. Higher power consumption reduces the battery lifetime of portable devices, affects device reliability, and increases cooling cost. Therefore, low-power methods are necessary for the design of these DSP-based systems. Since finite-impulse response (FIR) filters are critical to most DSP applications, an energy-aware filter design helps significantly in reducing the total power intake of the system. Reduction of hardware complexity directly relates to lower power consumption; therefore, several methods have been reported in the literature to reduce computational complexity.

Finite-Impulse response (FIR) digital filter is widely used in several digital signal processing applications, such as speech processing, loud speaker equalization, echo cancellation, adaptive noise cancellation, and various communication applications, including software-defined radio (SDR) and so on [1]. Many of these applications require FIR filters of large order to meet the stringent frequency specifications [2]–[4]. Very often these filters need to support high sampling rate for high-speed digital communication [5]. The number of multiplications and additions required for each filter output, however, increases linearly with the filter order.

There are some applications, such as SDR channelizer, where FIR filters need to be implemented in a reconfigurable hardware to support multi standard wireless communication [6]. Several designs have been suggested during the last decade for efficient realization of reconfigurable FIR (RFIR) using general multipliers and constant multiplication schemes. A RFIR filter architecture using computation sharing vector-scaling technique has been proposed. We explore the possibility of realization of block FIR filter in transpose form configuration in the inherent pipelining for area-delay efficient realization of large order FIR filters for reconfigurable applications. The main contributions of this paper are as follows.

1) Computational analysis of transpose form configuration of FIR filter and derivation of flow graph for transpose form block FIR filter with reduced register complexity.
2) Block formulation for transpose form FIR filter.
3) Design of transpose form block filter for reconfigurable applications.

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Based on a detailed computational analysis of transpose form configuration of FIR filter, they have derived a flow graph for transpose form block FIR filter with optimized register complexity. A generalized block formulation is presented for transpose form FIR filter. They have derived general multiplier based architecture for the proposed transpose form block filter for reconfigurable applications. The implementation of direct-form structure has less area delay product (ADP) and less energy per sample (EPS) for the short-length filters. But for medium or large length filters, it has high ADP and high EPS. In the FIR filter structure, the ripple carry adders are used to add the partial inner products. The well known adder architecture, Ripple Carry Adder is composed of cascaded full adders for n-bit adder. It is constructed by cascading full adder blocks in series. The carry out of one stage is fed directly to the carry-in of the next stage. For an n-bit parallel adder it requires n full adders.

II. RELATED WORKS

Pramod Kumar Meher (2006) proposed the structure that involves significantly less memory and less delay complexity compared with the existing DA-based structures for circular convolution. Besides, it is shown that the proposed systolic designs for circular convolution can be used for computation of linear convolution as well.

Basant Kumar Mohanty and Pramod Kumar Meher (2015) explore the possibility of realization of block FIR filter in transpose form configuration for area-delay efficient realization of large order FIR filters for both fixed and reconfigurable applications [7]. A generalized block formulation is presented for transpose form block FIR filter, and based on that they have derived transpose form block filter for reconfigurable applications. They have presented a scheme to identify the MCM blocks for horizontal and vertical sub expression elimination in the proposed block FIR filter for fixed coefficients to reduce the computational complexity. Performance comparison shows that the proposed structure involves significantly less ADP and less EPS than the existing block direct-form structure for medium or large filter lengths while for the short-length filters, the existing block direct-form structure has less ADP and less EPS than the proposed structure. Application-specific integrated circuit synthesis result shows that the proposed structure for block size 4 and filter length 64 involve 42% less ADP and 40% less EPS than the best available FIR filter structure for reconfigurable applications [1].

III. GENERAL BACKGROUND

The structure for transpose form block FIR filter is shown in Fig. 2 for the block size L = 4. It consists of one coefficient selection unit (CSU), one register unit (RU), M number of inner product units (IPUs), and one pipeline adder unit (PAU). The CSU stores coefficients of all the filters to be used for the reconfigurable application

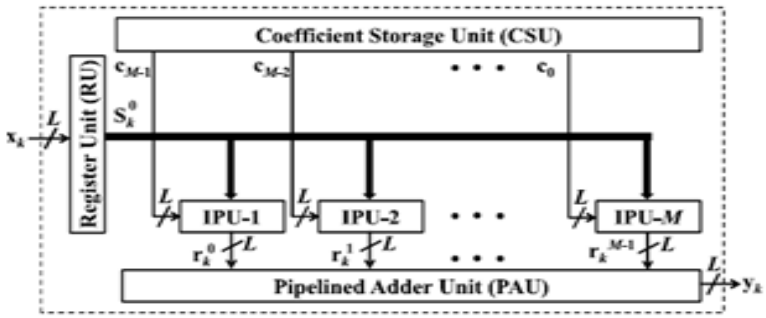

Fig.2. Structure for block FIR filter

It is implemented using N ROM LUTs, such that filter coefficients of any particular channel filter are obtained in one clock cycle, where N is the filter length.

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The RU [shown in Fig.3a] receives X_k during the k_{th} cycle and produces L rows of S_0 k in parallel. L rows of S_k^0 are transmitted to M IPUs of the proposed structure. The M IPUs also receive M short-weight vectors from the CSU.

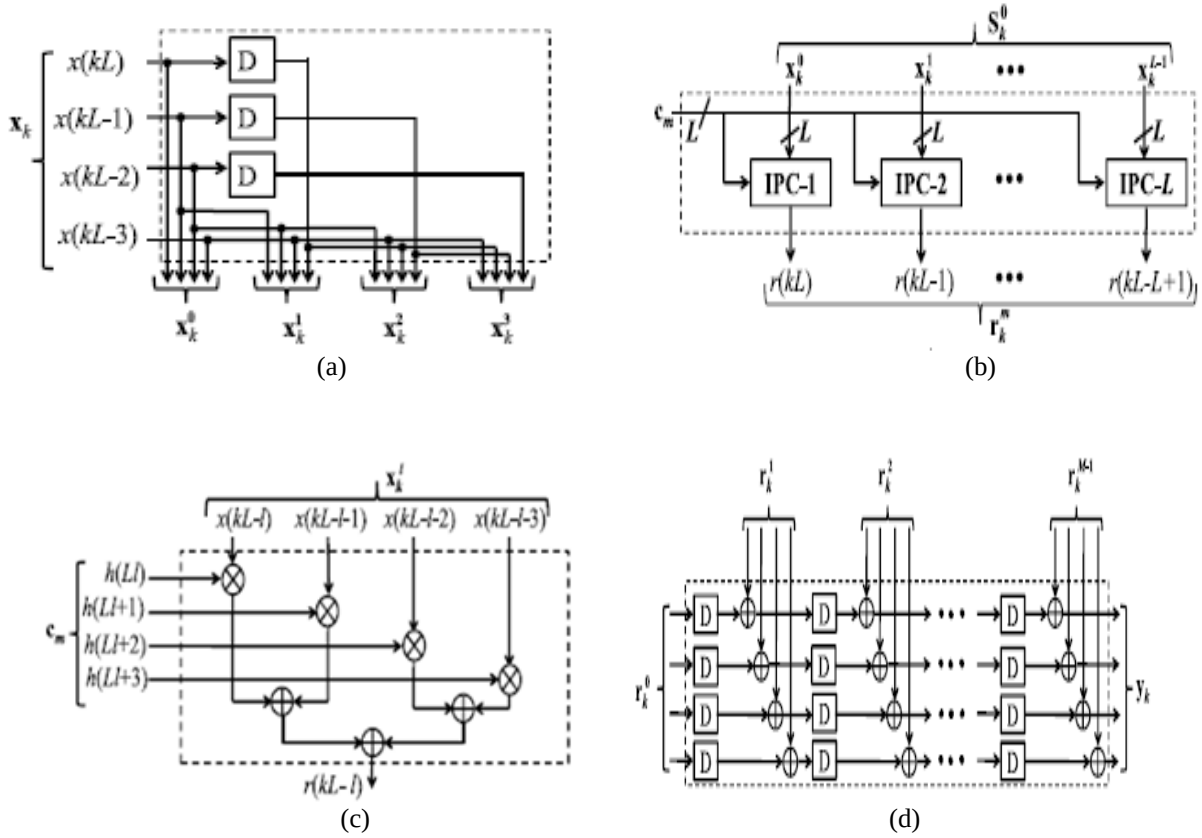

Fig.3. Internal structure (a) RU for block size L = 4 (b) (m + 1) th IPU (c) (l + 1) th IPC for L = 4 (d) PAU for block size L = 4

Structure of (m + 1)th IPU is shown in figure 3b. During the k_{th} cycle, the (m + 1)th IPU receives the weight vector C_{M-m-1} from the CSU and L rows of S_k^0 form the RU. Each IPU performs L inner-product computations of L rows with a common weight vector c_m. It consists of L number of L-point inner-product cells (IPCs). The (l +1)th IPC receives the (l +1)th row and the coefficient vector c_m, and computes a partial result of inner product $r(kL - l)$, for $0 \leq l \leq L - 1$. Internal structure of (l + 1)th IPC for L = 4 is shown in Figure 3c. All the M IPUs work in parallel and produce M blocks of result. These partial inner products are added in the PAU [shown in Figure 3d] to obtain a block of L filter outputs. In each cycle, the proposed structure receives a block of L inputs and produces a block of L filter outputs, where the duration of each cycle is T = TM + TA + TFA log2 L, TM is one multiplier delay, TA is one adder delay, and TFA is one full-adder delay.

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IV. PROPOSED METHOD

In the proposed reconfigurable design, modified booth multiplier is used instead of normal array multipliers. It will increase the speed and also reduce the area and power consumption. Carry look ahead adders are used to add partial products generated by the booth multiplier.

i. Pipeline Modified Booth Multiplier Architecture

The proposed architecture improves the performance and power saving of FIR filter. In the proposed architecture the multiplier in conventional is replaced with pipelined modified booth multiplier. This modified booth multiplier architecture efficiently saves power and improves performance with efficient trade off comparatively with conventional architecture. The pipeline technique is widely used to improve the performance of digital circuits. As the number of pipeline stages is increased, the path delays of each stage are decreased and the overall performance of the circuit is improved.

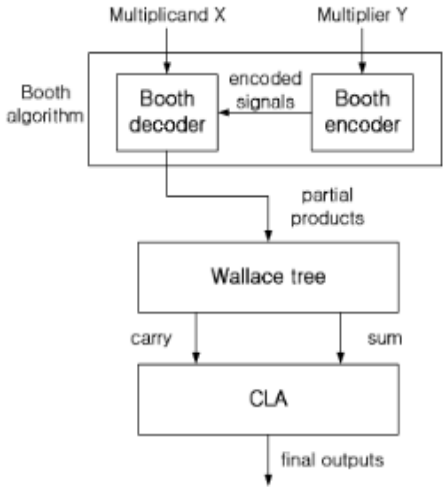

Fig.4. Booth multiplier

At first, we partitioned the modified Booth multiplier into three pipeline stages according to the functionality of the circuit as shown. The delay of the critical path of the 3-stage pipelined multiplier is reduced approximately by half compared to the non-pipelined one. The critical path of the 3-stage pipelined multiplier is in the Wallace tree because it requires the most intensive computation. It means that we can reduce the delays further by adding more pipeline registers within the Wallace tree.

ii. Modified booth multiplication algorithm

Modified Radix-4 Booth's Algorithm is made use of for fast multiplication. The salient feature of this algorithm is only *n*/2 clock cycles are needed for n-bit multiplication as compared to n clock cycles in Booth's algorithm. This type of multiplier operates faster than an array multiplier for longer operands because its computation time is proportional to the logarithm of the word length of operands. Booth multiplication is a technique that allows for smaller, faster multiplication circuits, by recoding the numbers that are multiplied. Multiplier is recorded, and then fewer steps may be needed on multiplication process.

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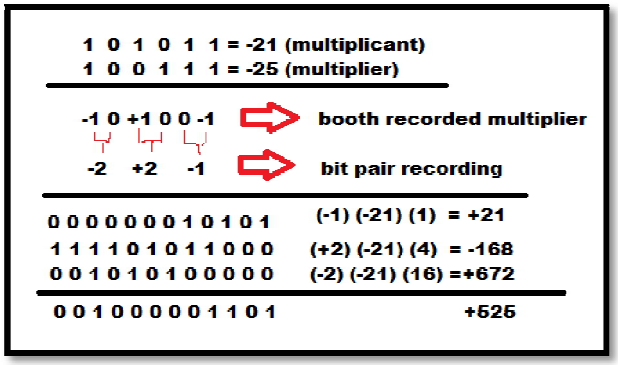

Fig.5. Example of modified booth algorithm

Booth recorded multiplier is obtained by scanning the original multiplier from right to left placing -1 in position where the first 1 in a string is encountered and placing +1 in a position where next 0 is encountered. An example of modified booth multiplication is shown in the figure 5. Bit pair coding are done using booth recording table, which is shown in figure 6.

Booth pair $(i+1, i)$			Recoded bit pair (i)	Corresponding multiplier bits $(i+1, i, i-1)$
0	0	=	0	000 or 111
0	+1	=	+1	001
0	−1	=	−1	110
+1	0	=	+2	011
+1	+1	=	—	
+1	−1	=	+1	010
−1	0	=	−2	100
−1	+1	=	−1	101
−1	−1	=	—	

Fig.6. Booth recording table

Finally, these sequences of sum bits and carry bits are given to a CLA. The CLA provides another speed boost to the system. They are the fastest adders. CLA consists of a set of full adders. A CLA shown in Figure 7 is identical to the half adder except that it has an additional input, C_{in}, so that a carry from a previous addition may be passed along.

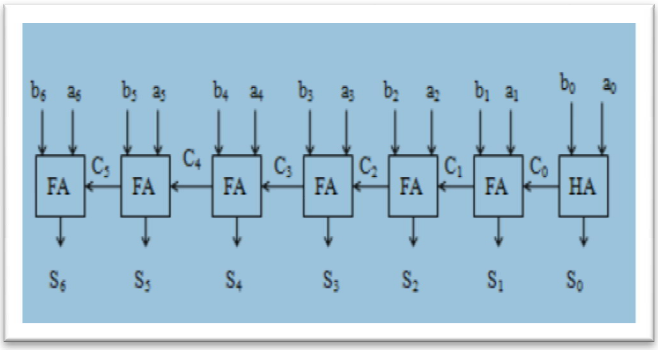

Fig.7. Carry- look ahead adder

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Furthermore, instead of a carry out, C_{out}, propagate (P) and generate (G) signals are produced. CLA calculates the carry signals in advance, based on the input signals. Carry generate and propagate signals only depend on the input bits.

$$S_i = A_i \text{ xor } B_i \text{ xor } C_{in}$$
$$P_i = A_i \text{ xor } B_i$$
$$G_i = A_i \times B_i$$
$$C_{i+1} = G_i + P_i C_i$$

The carry bits can be computed in parallel with the sum bits, which increases the speed of the adder compared to a ripple style adder. CLA is used to avoid the rippling carry present in ripple carry adder (RCA). Because, rippling carry produces an unnecessary delay in the circuit. CLA uses the concepts of generating and propagating the carry and it produces the final output and this is the output of the FIR filter.

V. RESULTS AND COMPARISON

The proposed block FIR filter using modified booth multipliers and carry-look ahead adder is simulated using model sim software. We have coded the proposed structure in VHDL. The area, power and time delay of the proposed FIR filter is analysed using Xilinx software. A comparison study between the existing method and proposed method is done and then graphs are plotted.

TABLE I
COMPARISON OF EXISTING AND PROPOSED METHOD

Parameter	Existing method	Proposed method
	Array multiplier based FIR	Booth multiplier based FIR
Slices	1800	1450
LUTs	3456	2699
Delay (ns)	20.510	16.894
Power (mW)	268	257

Application-specific integrated circuit synthesis result shows that the proposed structure for block size 4 and filter length 64 involve 42% less ADP and 40% less EPS than the best available FIR filter structure for reconfigurable applications. Area delay product of the proposed system is 42% less than the existing system. The energy per sample of the proposed Scheme is 40% less than the existing FIR filter structures.

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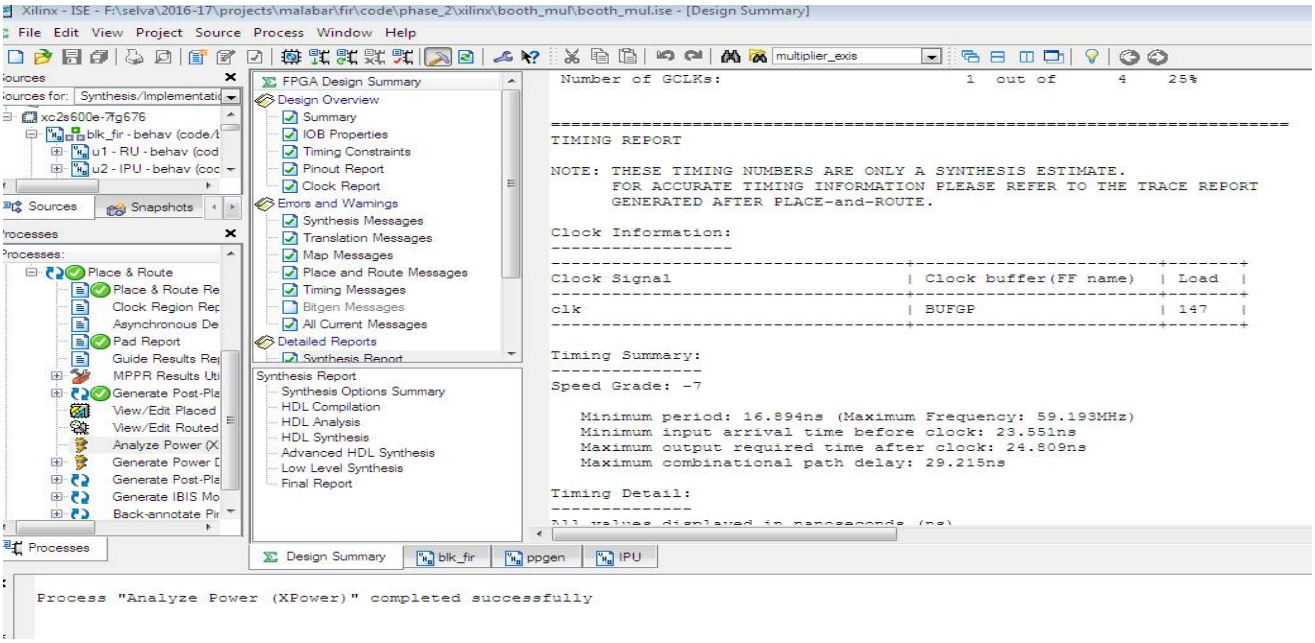
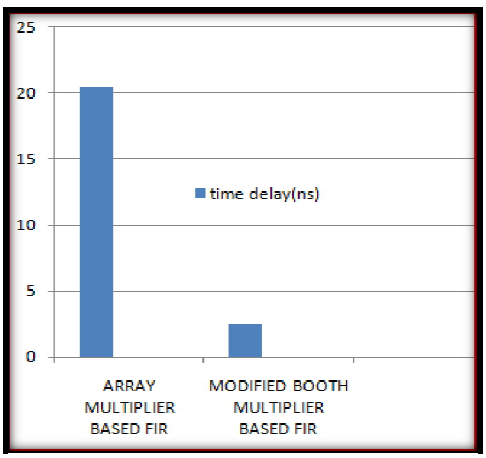
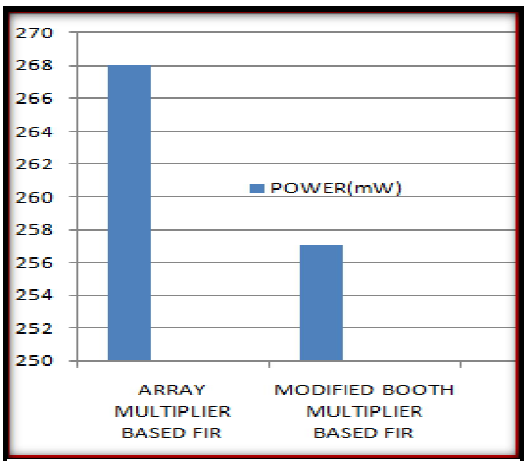


The time delay report is shown in the figure 8. The time delay of the existing method was 20.510 ns. Using the proposed method, this time delay is reduced to 16.894. So the time delay is reduced by 3.616 ns. The saving in cycle period in the transpose form structure for higher filter lengths is significant with respect to the cycle period of direct-form structure. Therefore, the overall ADP of the proposed structure is found to be less than that of direct form structure for higher filter lengths. The hardware and time complexities of the proposed structure and the extracted direct-from structure of [7] are listed in Table I for comparison. We have estimated hardware and time complexities of the proposed structure for block sizes L = 4, 8, and filter lengths N = 32 and 64



(a)



(b)

Fig.9. Parameter Comparison plot between existing and proposed method (a) Time delay (b) Power consumption

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The power report is shown in figure10. The total power required for the proposer system is 257mW. For the existing system using array multiplier, required power was 268mW. So the power is reduced by 11mW.

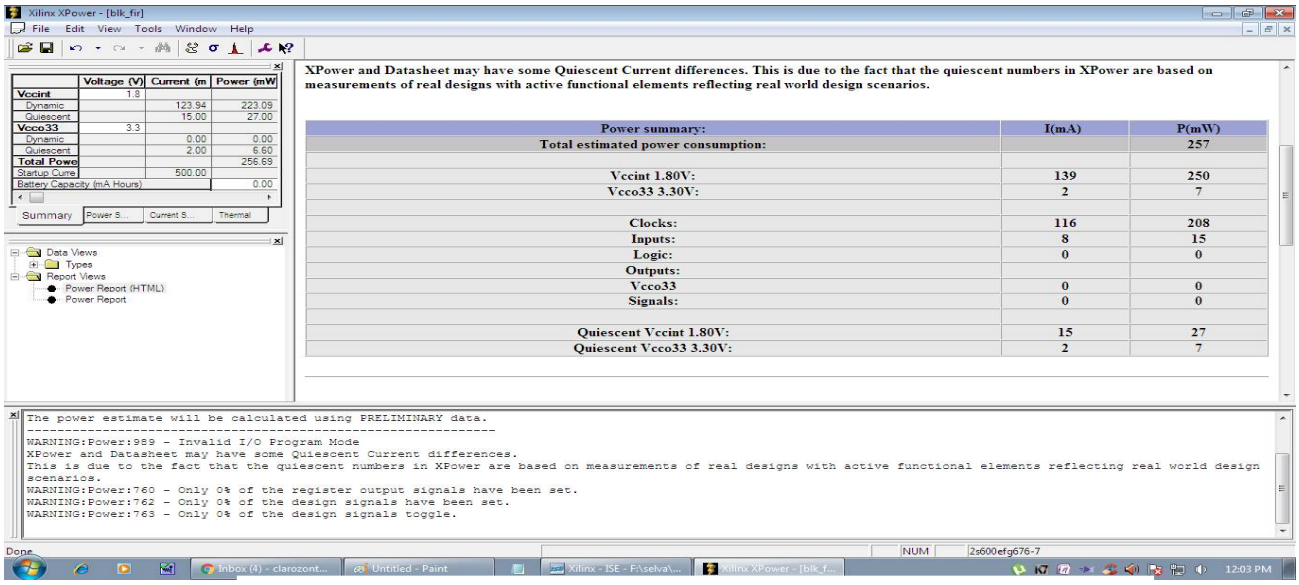

Fig.10. Power report of the proposed system from Xilinx software

The synthesis report is shown in figure11. The number of slices required for the array multiplier based method was 1800. It is reduced to 1480 when array multiplier is replaced by modified booth multiplier. Correspondingly the area of the filter is also reduced. The number of look up tables required for the array multiplier based method was 3456. It is reduced to 2699 when modified booth multiplier is used.

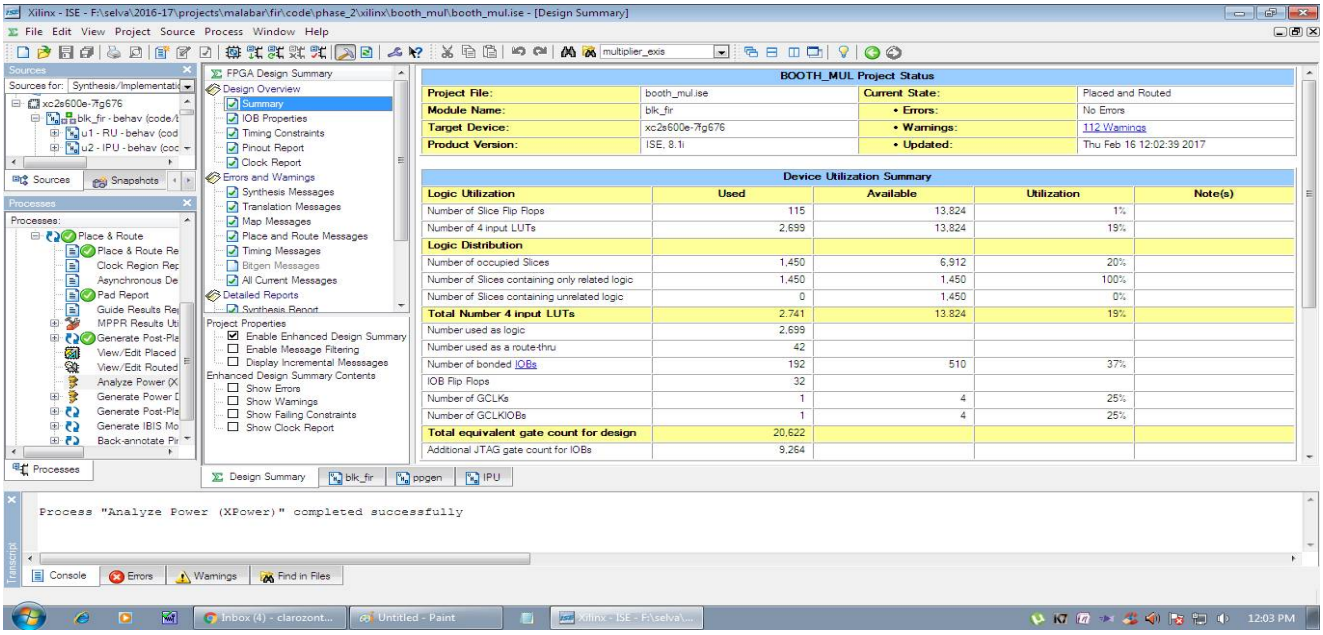

Fig.11. Synthesis report of the proposed system from Xilinx software

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VI. CONCLUSION

Area and delay efficient realizations of reconfigurable FIR applications were explored. The impact of power consumption, delay, area has been successfully done. Smaller truncation error and error compensation yields considerable time saved for the compensated circuit. A high-accuracy, low-cost, and flexible fixed-width got by using modified booth multiplier. The possibility of realization of FIR filter in transpose form configuration to achieve efficient area and delays for large order FIR filters were explored. In the FIR filter structure, the carry look ahead adder is used to add the partial inner products. The carry look ahead adder provides efficient area utilization by using this method. Application-specific integrated circuit synthesis result shows that the proposed structure for block size 4 and filter length 64 involve 42% less ADP and 40% less EPS than the best available FIR filter structure for reconfigurable applications.

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BIOGRAPHY

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