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FPGA Realization of FIR Filter by Efficient Multiple Constant Multiplication for Fixed Application

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ABSTRACT: This brief presents FPGA implementation of digital FIR Filter using Multiple Constant Multiplication (MCM) algorithm. MCM handled efficient implementation of filter using addition, subtraction and left shift of input signal. Many DSP application require FIR filter for attenuates or enhance the input signal. More no. of Multiplication in filter increases the hardware complexity.by using the MCM algorithm we reduce the computational multiplication and it reduces the implementation complexity. In this paper we explore the possibility of area-delay efficient realization of FIR.

KEYWORDS: Multiple Constant Multiplication algorithm;Field Programming Gate Array; Finite Impulse Response (FIR); Digital Signal Processing (DSP)

I. INTRODUCTION

Digital Signal Processing System is a physical device that performs an operation on signal that changes the signal characteristics like amplitude, shape and phase and frequency component of signal. Filters plays important role in to enhance or attenuates frequency components of signal.

Filters can be classified into Analog Filters and Digital Filters.Analog Filters require analog signal for their operation and also gives analog signal as output. Digital Filter is Linear Time Invariant discrete time system and require digital signal as input and gives digital output signal. Infinite Impulse Response (IIR) and Finite Impulse Response (FIR) are types of Digital Filters. FIR Filters are non-recursive type filters where output depends on present input and previous input signal. Finite Impulse Response Filters are widely used in many DSP application such as loud speaker equalization, adaptive noise cancellation, echo cancellation, speech processing and various communication application.

Along with the filtering operation the system should have low power, less area, less delay. For electronic application demanding low power, low area, less delay and high performance system. On FPGA and ASIC platforms different Filter schemes are implemented. FPGA gives better performance than the other ASIC and General Purpose platforms. Different designs are suggested by different researchers to implementation of FIR using Distributed Arithmetic and Multiple Constant Multiplication Algorithm for fixed coefficient applications.

TO reduce complexity of design DA based algorithm used LUTs to store results. MCM algorithm reduces design complexity by reducing no. of additions for multiplication. DA based Reconfigurable FIR structure suggested recently using direct form configuration.

II. RELATED WORK

In [2] authors proposed and presented the area-delay-power efficient FIR Filter implemented by Distributed Arithmetic algorithm using systolic decomposition. This DA-based efficient realization of FIR Filter using implemented on Xilinx Vertex-E XCV2000E FPGA for different order performance analysis can be done by number of slices, power consumption, energy throughput, maximum operating frequency. The proposed FIR implementation on FPGA gives less area delay structure than existing DA-Based structure implementation. FIR Filter implemented on the FPGA using direct and transpose form architecture in [3]. This proposed structure implemented using Verilog Hardware Description Language on Xilinx SPARTAN2-XC2S50-5I-tq144 FPGA.

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Authors [4] resented Low Complexity and Reconfigurable FIR Filter for wireless communication. In this paper Constant Shift method and Programmable Shift methods are implemented for Reconfigurable FIR Filter. Proposed architecture capable for operating filter coefficient with different word length without hardware complexity. This proposed architecture implemented on VERTEX 2V3000ff1152-4 Field Programming Gate Array and simulated on 0.18 CMOS Technology. Design structure gives good area and power and speed improvement. The MCM based approach presented for FIR Filter in [5].

A given set of fixed point constant multiplies with variable using multiplier block .Multiplier Block consist of Addition, subtraction and shift operation. This authors provide solution for MCM problems it gives 20 percent less Addition and subtraction.

III. PROPOSED ALGORITHM

FIR Filter structure are simply add and shift operation and minimizing the additions and subtraction operation is the main goal of research.

Proposed structure for fixed application consist of

- Coefficient Storage Unit (CSU),
- Register Unit,
- MCM Units,
- Pipeline Adder unit.

Input x (k) is given to Register Unit during kth cycle and produces S_k^0 of L rows parallel. The CSU stores all coefficients of Filter. For lower complexity multiplication is mapped into MCM Unit.

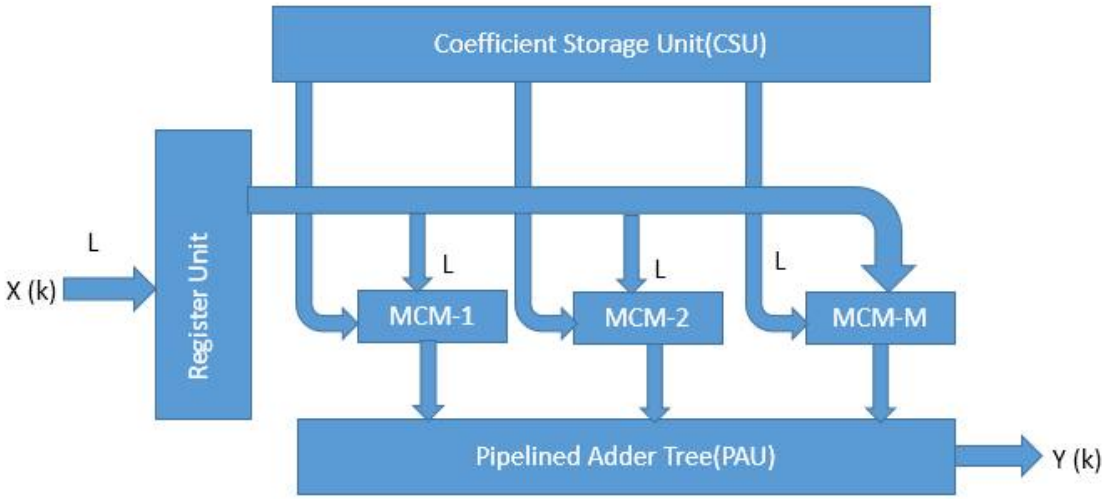

Fig.1.Proposed Structure for FIR Filter

Multiple Constant Multiplication (MCM) is an arithmetic operation where fixed point variable is multiples with set of fixed point constants. For MCM based implementation filter uses vertical and horizontal common subexpression elimination method. This reduces the no. of shift and add operation.

Avoiding costly multipliers is important for hardware implementation and replacing adders and shifts is important for software implementation.MCM scheme is more effective when more number of constants multiplies with common operand. Therefore MCM scheme is more effective for large order filters for fixed applications.

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Input Sample	Coefficient Group
x(4k)	{h(0),h(4),h(8),h(12)}
x(4k-1)	{h(0),h(4),h(8),h(12)} {h(1),h(5),h(9),h(13)}
x(4k-2)	{h(0),h(4),h(8),h(12)} {h(1),h(5),h(9),h(13)} {h(2),h(6),h(10),h(14)}
x(4k-3)	{h(0),h(4),h(8),h(12)} {h(1),h(5),h(9),h(13)} {h(2),h(6),h(10),h(14)} {h(3),h(7),h(11),h(15)}
x(4k-4)	{h(1),h(5),h(9),h(13)} {h(2),h(6),h(10),h(14)} {h(3),h(7),h(11),h(15)}
x(4k-5)	{h(2),h(6),h(10),h(14)} {h(3),h(7),h(11),h(15)}
x(4k-6)	{h(3),h(7),h(11),h(15)}

Table.1.MCM for block FIR Filter

Table 1 shows MCM is applied to coefficient matrix in both Horizontal and vertical direction. It shows that the particular input sample is required particular coefficient for computation. Only four coefficient is required to input sample x (k) for computation but x (4k-3) required for rows and four column coefficients.
For large order filter coefficient matrix size is larger because of that for all samples MCM size also become larger and it will reduce complexity of filter computation. Each MCM block produces necessary product terms shown in table 1.

IV. SIMULATION RESULTS

A. Implementation Setup

We have coded the proposed structure in VHDL for filterlengths 16and block sizes 4.XILINX ISE web pack 14.1used for design, synthesis and implementation. Verilog are used to describe the behaviour and structure of system and circuit designs. The proposed structure simulated on the Xilinx System Generator.

B. Performance Comparison

The performance comparison table shows that proposed structure requires less number of multipliers and adders than existing algorithm.

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Resources	Proposed structure	Mohanty structure
Length	16	16
Flip-Flop	834	312
Multiplier	46	64
Adder	49	60

Table. 2. Performance Comparison

C. Synthesis And Simulation Result:

Synthesis report shows the no of flip-flops, counters, LUTs for implementation of block FIR Filter using MCM. It also gives information about device utilization. Simulation result gives output of Filter.The experimental results indicate that Parallel processing FIR filter implementation of Multiple Constant Multiplication.

Device Utilization Summary				[-]
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	840	12,480	6%	
Number used as Flip Flops	834			
Number used as Latch-thrus	6			
Number of Slice LUTs	1,330	12,480	10%	
Number used as logic	1,180	12,480	9%	
Number using O6 output only	918			
Number using O5 output only	195			
Number using O5 and O6	67			
Number used as exclusive route-thru	150			
Number of route-thrus	486			
Number using O6 output only	307			
Number using O5 output only	141			
Number using O5 and O6	38			
Number of occupied Slices	516	3,120	16%	
Number of LUT Flip Flop pairs used	1,752			
Number with an unused Flip Flop	912	1,752	52%	
Number with an unused LUT	422	1,752	24%	
Number of fully used LUT-FF pairs	418	1,752	23%	
Number of unique control sets	7			
Number of slice register sites lost to control set restrictions	6	12,480	1%	
Number of bonded IOBs	20	172	11%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Average Fanout of Non-Clock Nets	2.79			

Fig .2.Proposed structure Simulation Report

After completion of simulation process, synthesis process is takes place to calculate gate count and delay report. Fig. below shows output of FIR Filter using MCM Scheme when input sample and filter coefficients are given.

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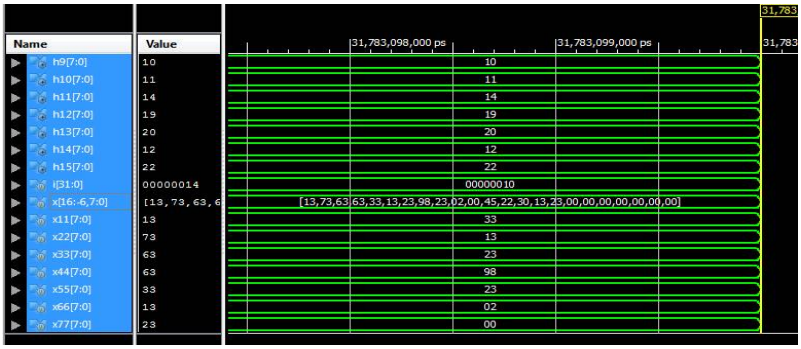

Fig .3.Proposed structure output for FIR filter

V. CONCLUSION AND FUTURE WORK

In this paper, proposed structure provide area delay efficient realization for Fixed and Reconfigurable Application. The design of block FIR Filter using MCM Scheme reduces the computational complexity of structure by reducing no. of addition and multiplication.

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BIOGRAPHY

Kishori Kalidas Birdawade received the B.E. degree in Electronics and Communication Engineering in the year 2013 and pursuing M.E.degree in VLSI Design from Siddhant College of Engineering. Her area of interests includes VLSI Signal Processing and VLSI Design.