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Design of Hardware accelerator for Singular Value Decomposition

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ABSTRACT: The main objective is to design a high performance implementation of the Givens Rotation in VLSI Hardware. The Givens Rotation algorithm has many applications in computer vision (CV) and artificial intelligence area. Givens Rotation is the major part in the matrix operations like singular value decomposition or eigen value and eigen vector computation, which has many applications. A few examples include –object recognition, face recognition and dimensionality reduction, principle component analysis etc. These matrix operations involve lot of Givens Rotation applied in iterative manner. Though the iterative approach of the matrix operations implemented in software gives decent performance on the high end processors, it's still slow to compute on low end desktop computers or embedded devices. In this scenario, providing a hardware accelerator that can be used to improve the performance of Givens Rotation computation is necessary.

In this project VLSI architecture for computing the Givens Rotation will be proposed. The architecture will be coded using Verilog HDL language. The design will be simulated to see the performance improvement and synthesized to see the area required by the hardware on FPGA.

Tools:Altera quartus II Modelsim simulator
Language: Verilog HDL Language.

KEYWORDS: Givens Rotation, Singular value decomposition, FPGA, HDL.

I.INTRODUCTION

The Singular Value Decomposition (SVD) is an important matrix factorization procedure used extensively in signal and image processing algorithms. It is very well suited to analyzing data matrices from sensor arrays. The singular values can also be used to determine the rank of a matrix in numerically reliable manner. Computation of SVD from characteristic equation approach is time consuming because of so many calculations required; this is too costly to have in software as well as hardware. So, finding eigen values in a different way is must.

SVD algorithms require costly arithmetic operations such as division and square root in the computation of rotation parameters. Increased efficiency may be obtained through the use of hardware oriented arithmetic techniques that relate better to the algorithm. Special VLSI structures have been proposed for SVD. The Coordinate Rotation Digital Computer (CORDIC) algorithms, which allow easy computation of inverse tangents and vector rotations, have proven extremely useful in this context.

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II.RELATED WORK

Hardware acceleration is a technique which uses computer hardware to perform some operations more effectively than in software. The hardware which performs acceleration when it is the separate unit from CPU is called as hardware accelerator. Givens Rotation hardware accelerator is used to enhance the performance of Givens Rotation by using FPGA.

III.PROPOSED SYSTEM

A. *Block Diagram:*

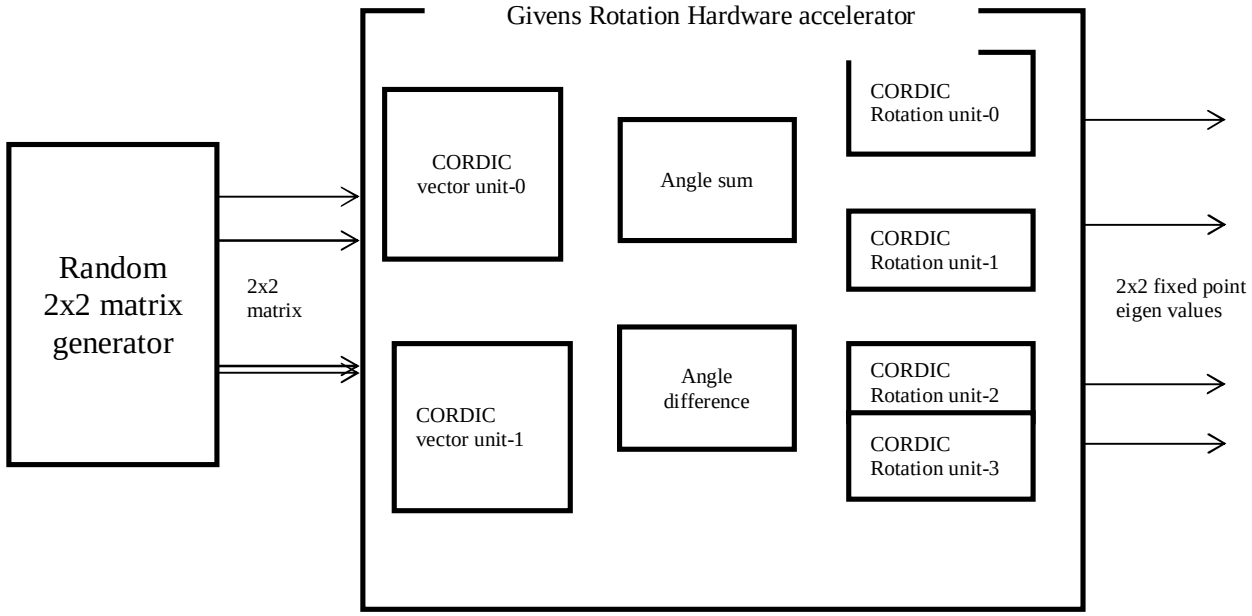

Fig. 1.Block Diagram of the system

Functional blocks in the above fig. are

- Random 2x2 matrix generator
- CORDIC Vector unit
- Angle Sum and Angle Difference
- CORDIC Rotation unit.

The input matrices are generated by random 2x2 matrix generator using MATLAB which are given as an input to the model simulator. It is coded in Verilog Hardware Description Language. CORDIC Vector units compute the angle up to which we rotate to get SVD. Angle sum and angle difference are used to find out left rotation angle(θ_l) and right rotation angle(θ_r). CORDIC Rotation unit rotate the matrices by $\theta_r$and θ_l. Finally SVD of matrices was obtained which are represented in fixed point format. Later, the whole design is synthesized on FPGA to see performance improvement.

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B. *Random matrix generator:*
Random matrix generator consists of look up tables, multiplexers, SVD top level module as shown in below fig.

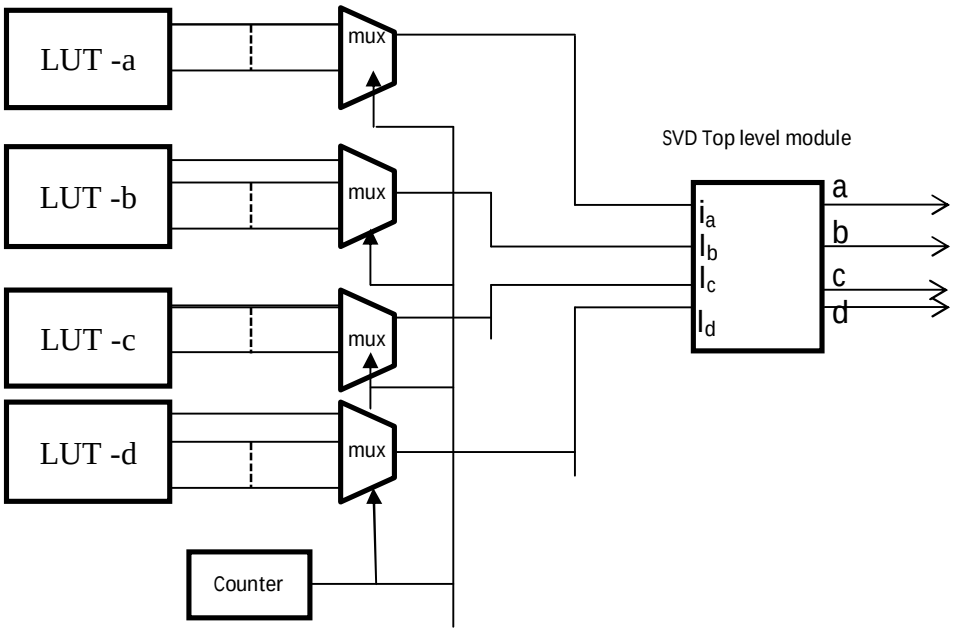

Fig. 2.Random matrix generator

Look up tables stores the values to which SVD to be computed. Multiplexer prefetches the value from the look up table and selects corresponding value based on the counter value. The value of the counter depends upon the number matrices to be generated.

CORDIC:
Coordinate Rotation Digital Computer (CORDIC) is a method of calculating math functions using much simpler math operations in a loop called a binary search. Most commonly CORDIC is used to calculate angle and hypotenuse of a point. CORDIC uses simple shift- add operations for several computing tasks such as calculation of trigonometric, hyperbolic and logarithmic functions, real and complex functions, division, square root calculations, solution of linear systems, eigen value estimation, SVD, QR factorization and many others .

C. *CORDIC Vector unit:*
In this unit the vectors in Cartesian coordinates are converted in to polar coordinates and represented in fixed point forat. Let say you have a point(X, Y) then

$$\theta = \tan^{-1}(Y/X)$$

In general the angle of line joining (X, Y) with respect to the origin can be computed with respect to X-axis in iterative manner.

$Y=X \tan\theta$

Where $\theta = \frac{\pi}{4}, \frac{\pi}{8}, \frac{\pi}{16}, \frac{\pi}{32}, \frac{\pi}{64}$……..

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If Y is less than the absolute then the angle will incremented else the angle will decremented. This process will continued until we reach the angle at which Y is very close to the absolute value. Reduce or enhance the θ by half until value of Y very close to the value we have. The fig. below describes the working of usual CORDIC algorithm.

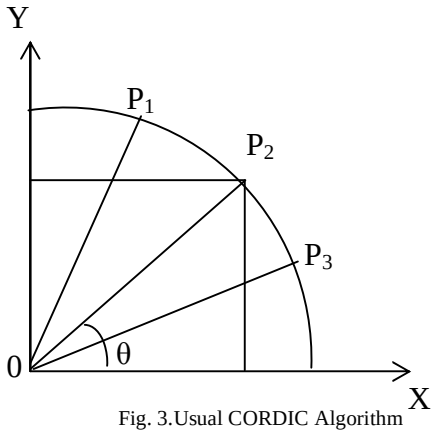

Fig. 3.Usual CORDIC Algorithm

$Y = X \tan(\pi/4) = X*1$

$Y = X \tan(\pi/8) = X*0.4142$

$Y = X \tan(\pi/16) = X*0.1989$

$Y = X \tan(\pi/32) = X*0.0985$

This is the usual way which was used in CORDIC algorithm. It needs a multiplier which is not desirable because it takes a lot of area and complex to design. So, we avoid multiplier.

We replace the multiplier with arithmetic right shift operation by taking angles $\tan^{-1}(1)$, $\tan^{-1}(1/2)$, $\tan^{-1}(1/4)$…….. Instead of $\pi/4,\pi/8,\pi/16,\pi/32$…….

$Y = X \tan\theta$

$Y = X \tan(\tan^{-1}1) = X*1$

$Y = X \tan(\tan^{-1}(1/2)) = X*\frac{1}{2}$

$Y = X \tan(\tan^{-1}(1/4)) = X*\frac{1}{4}$

The number which is divided by 2^n is equal to the number right shifted by n bits. It does not require any hardware.

CORDIC algorithm which is used for finding an angle is as follows:

If Y is positive then

$X_{new} = X+(Y>>\text{iteration number})$

$Y_{new} = X-(Y>>\text{iteration number})$

Sum angle= Sum angle + Angle table [iteration number]

Iteration number = Iteration number + 1

If Y is negative

$X_{new} = X-(Y>>\text{iteration number})$

$Y_{new} = X+(Y>>\text{iteration number})$

Sum angle= Sum angle + Angle table [iteration number]

Angle table stored with set of angles. The total number of angles in the table depends upon the number of iterations to be performed. Number of iterations is equals to number of angles in the table.

D.*Angle sum and Angle difference:*

The outputs of CORDIC vector units are angle sum and angle difference. By using these angles we can compute left rotation angle and right rotation angle which are used for finding SVD or diagonalized matrix.

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$\theta_{sum} = (\theta_r + \theta_l) = \tan^{-1}(\frac{c+b}{d-a})$ …… (1)

$\theta_{diff} = (\theta_r - \theta_l) = \tan^{-1}(\frac{c-b}{d+a})$ ……..(2)

E. *CORDIC Rotation unit:*
It is the reverse process of CORDIC vector unit. When we started with point(X,Y) using number of iterations we got an angle. By doing reverse process with same number of iterations we will get to the SVD.

IV.INPUT-OUTPUT FORMATS

Table 1.Input-Output representation formats

Type	Inputs	Outputs	Format for angle
CORDIC Vector Unit	X,Y	Θ	Q.14
CORDIC Rotation Unit	X, Y ,θ	X_0, Y_0	Q.6

The above table describes about input-output formats. Here X, Y are inputs to the CORDIC Vector Unit and θ is the output. The input and outputs of the CORDIC rotation unit are X, Y, θ and X_0, Y_0
Where Q.14 and Q.6 represents after radix or decimal point 14, 6 digits are taken to consideration respectively.

V.RESULTS

Top level module on Test bench:

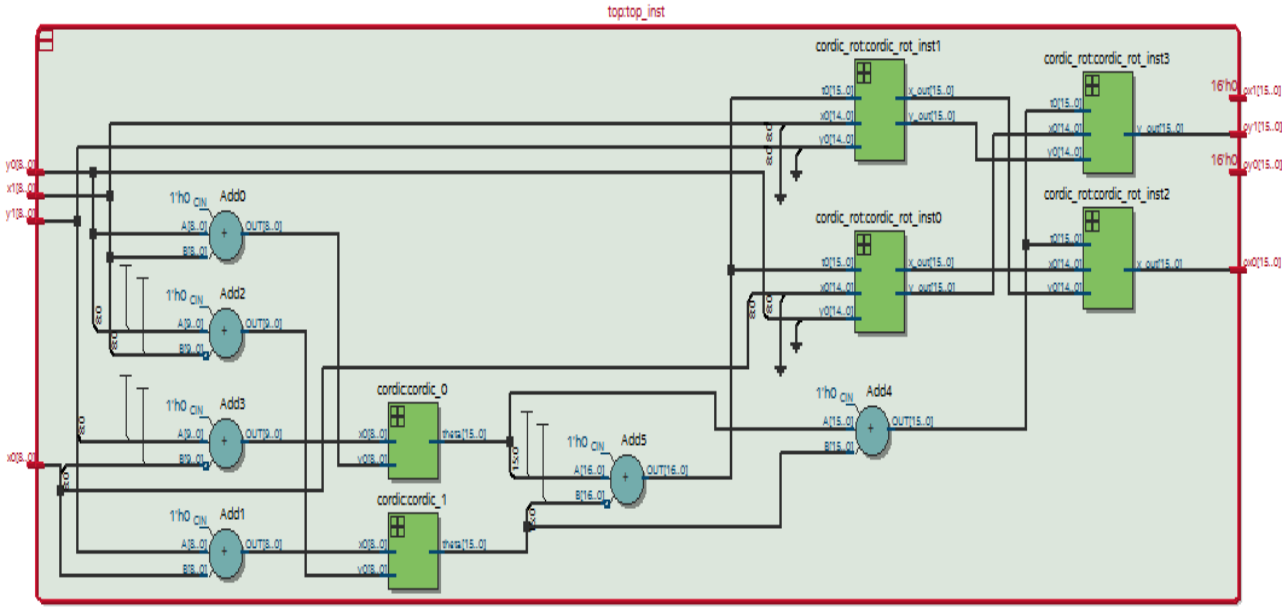

Fig. 4.Top level module

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The fig. above describes the internal structure of block diagram obtained on test bench. The 2x2 matrix is given as inputs which are generated by using random matrix generator. Adders in the above fig are used for compute eq. (1) and eq. (2) which are given to CORDIC Vector unit then angle sum and angle difference are obtained. Then, by using angle sum and angle difference compute $\theta_r$and θ_l(from eq.(1) and eq.(2)). Finally, CORDIC Rotation unit gives the diagonal matrix as an output.

Modelsim Simulation Result:

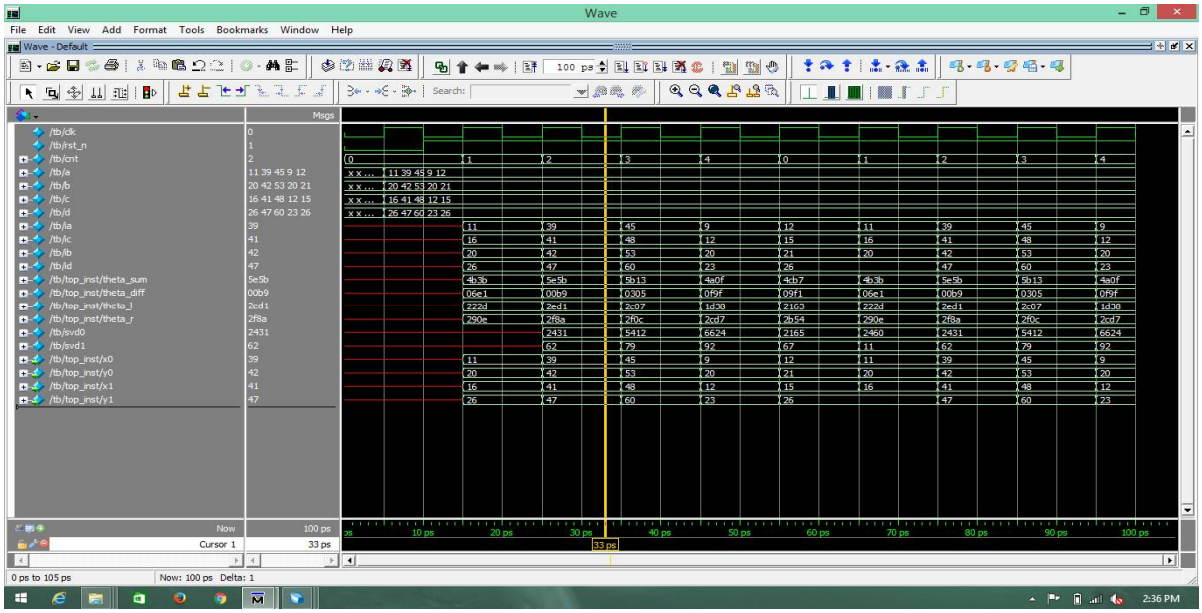

Fig. 5.Modelsim output waveform

The fig. above shows the inputs and outputs obtained by using Modelsim software.

Synthesis Result using FPGA:

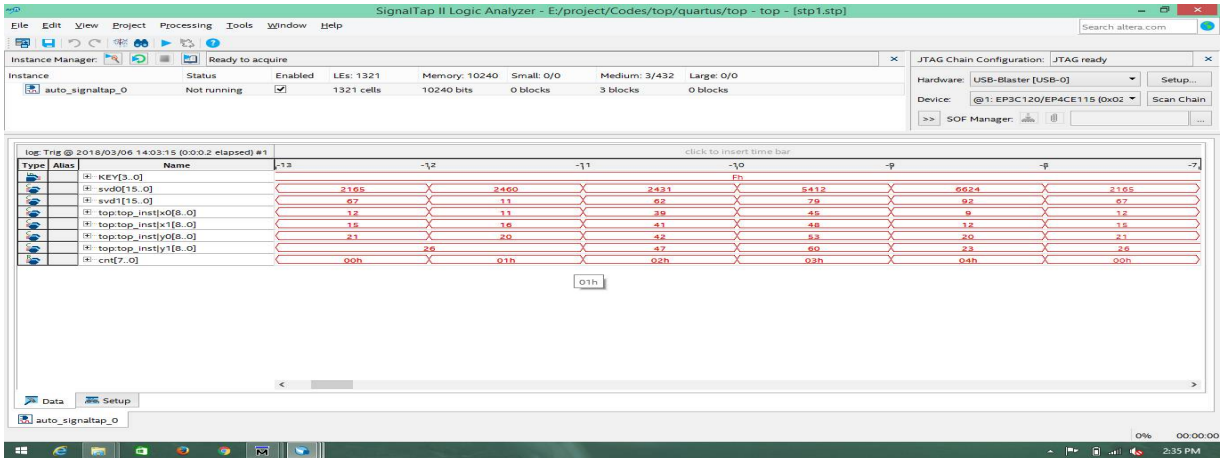

Fig. 6.Synthesis result using FPGA

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The above fig. shows the output waveforms obtained by performing synthesis on FPGA

VI. PERFORMANCE IMPROVEMENT

Singular Value Decomposition (SVD) of a 2x2 matrix can be computed by using rotations and is expressed as follows

$$R(\theta_r)^T \begin{bmatrix} a & b \\ c & d \end{bmatrix} R(\theta_l) = \begin{bmatrix} d1 & 0 \\ 0 & d2 \end{bmatrix}$$

Where $R(\theta) = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix}$ is a rotation matrix and $\begin{bmatrix} a & b \\ c & d \end{bmatrix}$ is the input 2x2 matrix.
By solving this equation results 40 cycles as shown in fig. 7.

Operation	Count
Addition	8
Subtraction	4
Multiplication	24
Sin	2
Cos	2
Total	40

Table 2.Comparision between software and hardware implementation

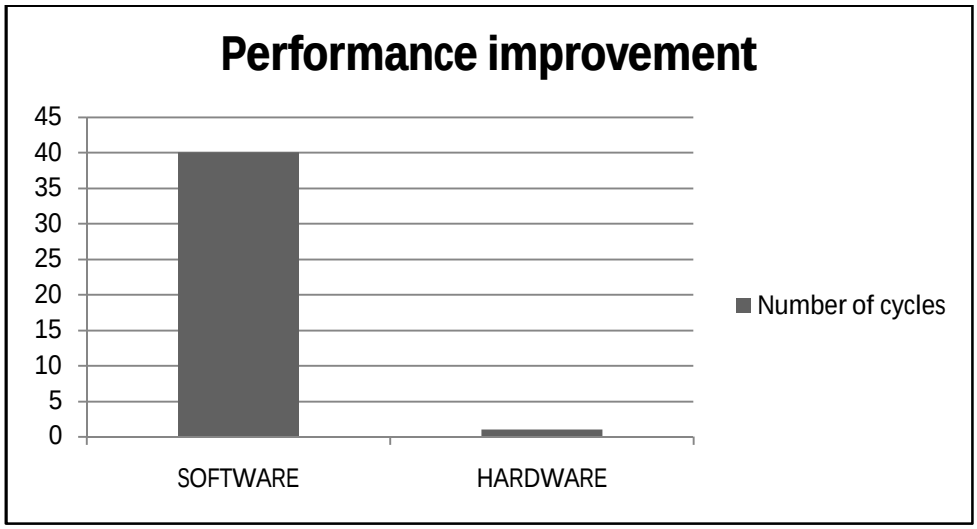

Fig. 7.No of operations to be performed by using software

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So, it requires 8 adders, 4 subtractors, 24 multipliers, 2 Sin and 2 Cosine operations. The software implementation would take minimum 40 cycles for a 2x2 SVD computation. This means the hardware accelerator is minimum 4oX faster than software implementation.

VI.CONCLUSION

Hardware accelerator for Givens Rotation was designed and eigen values are computed. It gave the same output as in MATLAB. Time consuming to compute eigen values are reduced from 40 cycles to one cycle. So, performance was enhances extensively.

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