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Improving Processor Load by using Token Memory Approach

[1]**Buddh Bhagwan Sahu,** [2]**Prof. Rajesh Tiwari**

[1]M.E, Dept. of Computer Science & Engineering, Shankaracharya Group of Institutions, Bhilai (C.G.), India

[2]Associate Professor, Dept. of Computer Science & Engineering, Shankaracharya Group of Institutions, Bhilai (C.G.), India

ABSTRACT: A parallel computer (or multiple processor system) is a collection of communicating processing elements (processors) that cooperate to solve large computational problems fast by dividing such problems into parallel tasks, exploiting Thread-Level Parallelism (TLP).The major issues involved in parallel processing are the concurrency and communication characteristics of parallel algorithms for a given computational problem, The number of processing elements (PEs), computing power of each element and amount/organization of physical memory used, how the processing elements cooperate and communicate and how data is shared/transmitted between processors. The major approach of the work is to propose a token memory architecture to reduce the load on CPU parallel processing .During peak period the heavy tasks will be transferred to this token memory so as to reduce load on CPU.

KEYWORDS: CPU (Central Processing Unit), Token memory, Parallel Processing.

I. INTRODUCTION

Parallel processing is a method of simultaneously breaking up and running software endeavours on multiple microprocessors, thereby reducing processing time. Parallel processing may be accomplished via a computer network or via a computer with two or more processors. Parallel processing can be called parallel computing.
The significant advantages of parallel processing comprise:

- In theory, throwing more resources at a job will shorten it's time to completion, with potential cost savings. Parallel computers can be assembled from cheap, commodity components.
- Many issues are not so small and/or complicated that it's impossible or impractical to solve them on a single computer, particularly given small computer memory.
- Multiple compute resources can do many things concurrently. Using computer resources when local compute resources are inadequate or scarce.
- Modern computers laptops are concurrent in structure with multiple processors/cores. Parallel software is specifically intended with multiple cores, threads, etc. for hardware that was parallel usually, successive software run on modern computers "waste" potential computing power.

The major issues involved in parallel computing architecture are:-

- The number of processing elements (PEs), computing power of each element and amount/organization of physical memory used .i.e. the amount of computational resources are allocated to each processing element.
- One of the major issues involved is how data is shared between the processors.
- Parallel Processing Performance and Scalability Goals by minimizing parallelization overheads and balancing workload on processors thereby enhancing the scalability of performance on larger subsystems.
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II. RELATED WORK

According to [1] the main challenge as computer architects is to deliver end-to-end performance growth at historical levels in the presence of technology discontinuities. We can address this challenge by focusing on power optimization at all levels. Compared to DRAM, the new memories have two major differences, non-volatility and write overhead in terms of endurance, latency and power. The impact of new memory-aware software/hardware designs on program

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performance on a DRAM/SRAM hybrid memory [2]. Each system has large, shared semiconductor memories. The models are validated using simulation. They can be utilized to quickly reduce the design space and study various trade-offs [3]. As DRAM faces scaling limit, several new memory technologies are considered as candidates for replacing or complementing DRAM main memory. And SRAM Compared to DRAM, the new memories have two major differences, non-volatility and write overhead in terms of endurance, latency and power. The impact of new memory-aware software/hardware designs on program performance on a DRAM/SRAM hybrid memory [4].

III.EXPERIMENTAL ENVIRONMENT

The problem of optimally assigning the modules of a parallel program over the processors of a multiple-computer system is addressed.The major approach of the work is to propose token memory architecture to reduce the load on CPU parallel processing:

- During peak period the heavy tasks will be transferred to this token memory so as to reduce load on CPU. As the number of processor increases in a parallel computer, the fixed load is distributed to more processor for parallel execution therefore; the main objective is to produce the results as soon as possible.
- In other words minimal turnaround time is the primary goal.
- During system initialization, as per the token memory approach the system assigns each block as T tokens, stores them at the block's home memory.T is at least as large as the number of processors. During excessive work load on CPU the additional processes are transferred to these token blocks so as to reduce the load on CPU. The processes assigned to these blocks are then retrieved to be processes when the CPU is free.
- In many practical applications that demand a real time it is response, the computational work load is often fixed with a fixed problem size. As the number of processor increases in a parallel computer, the fixed load is distributed to more processor for parallel execution therefore; the main objective is to produce the results as soon as possible. In other words minimal turnaround time is the primary goal. Speedup obtained for time-critical application is fixed load speedup.

The performance evaluation is based on experimental measurements. The machine we have used for all experiments is a standard Core i3 processor with a physical memory space of 2 GB. The main aspects of performance where:-

- Availability: Availability of a system is typically measured as a factor of its reliability - as reliability increases, so does availability.
- Response time: Response time is the total amount of time it takes to respond to a request for service.
- Processing speed: It is the measure of speed of processing in megahertz.
- Latency: Latency is a time delay between the cause and the effect of some physical change in the system being observed.

During experiments processing performance was observed using some major programs during the peak load time without Token Memory Approach which is as given below:

Program	Availability (%)	Response time (%)	Processing speed (%)	Latency (%)
Word Processing	8	6	5	7
DMBS	6	3	4	2
Tool software of CAD	2	1.5	3	2.5
MIS	4	1.5	4	3

Table: Performance statistics without Token Memory Approach

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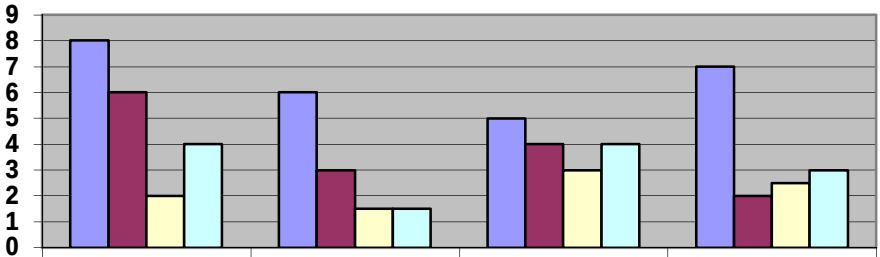

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DMBS	6	3	4	2
Tool software of CAD	2	1.5	3	2.5
MIS	4	1.5	4	3

Figure: Performance graph without Token Memory Approach

Program	Availability (%)	Response time(%)	Processing speed(%)	Latency (%)
Word Processing	10	8	7	9
DMBS	8	5	6	4
Tool software of CAD	4	3	5	4.5
MIS	6	4	5	5

Table: Performance statistics with Token Memory Approach

Experiments clearly show that the performance of the processing is improved greatly if used with Token Memory approach.

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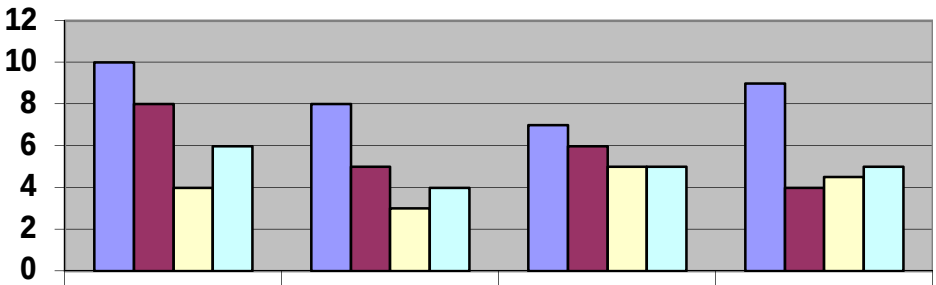

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Figure: Performance graph with Token Memory Approach

IV. CONCLUSION

This current work presents a new approach which involved using of token memory. The token memory (TM) stores mainly the instructions which are transferred to basically reduce the overload on processing similar to accumulators or registers in conventional computers. When there is the size of the TM is expected to be relatively small because the data values occupy space in the TM for a very short time. The small scale TM in our architecture makes it possible to reduce the complexity of the switch mechanism between functional units and memories, and the size of the control circuit. Learning arises from the patterns of activation that

1. Extended circuitry
2. Best performance and heat less work
3. Faster services

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