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Quaternary Adder Design on FPGA

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ABSTRACT: The high speed digital circuits became more prominent with incorporating information processing and computing. Arithmetic circuits play a very critical role in both general-purpose and application specific computational circuits. The modern computers lead to the deterioration in performance of arithmetic operations such as addition, subtraction, multiplication, division, on the aspects of carry propagation delay, large circuit complexity and high power consumption. Designing this adder using QSD number representation allows fast addition/subtraction which is capable of carry free addition and borrows free subtraction because the carry propagation chain are eliminated, hence it reduce the propagation time in comparison with radix 2 system. QSD number system based on quaternary system, each digit can be represented by a number from -3 to 3. Operation on large number of digits such as 64, 128 or more, can be implemented with constant delay and complexity.

KEYWORDS: QSD-Quaternary Arithmetic Unit, FPGA-Field Programmable Gate Array, MVL-Multi Valued Logic, VHDL.

I. INTRODUCTION

In digital systems like computers and digital signal processors arithmetic operation plays a very important role. Arithmetic operations based on binary number system include problems like higher propagation delay, circuit complexity. When the number of bits increases the hardware also increases which means complexity goes on increasing. According to moor's law the number of transistors in an integrated circuit has doubled approximately every two years hence in integrated circuits the number of components goes on increasing because of this interconnects increases, nearly 70 percent area of the chip is occupied by interconnections. This problem can be overcome by multiple value logic concepts [1]. In this multiple value logic concept more number of logics are inserted into the wire. This paper implements a quaternary logic in which four different logic levels are used. The arithmetic operations performed here are carry free addition i.e. elimination of carry from further propagation, borrow free subtraction. Operation speed of adder is faster because of the carry free addition and the borrow free subtraction [3]. The QSD numbers are both positive and negative numbers. As the technology is evolving the number of devices accommodated on the IC goes on increasing because of this many problems are arise. The interconnection inside and outside of the integrated circuits becoming very complicated and area occupied by the interconnect goes on increasing. Inappropriate routing results in a large chip size and hence causes crosstalk and timing problems. This problem has the highest priority in deep submicron designs. The solution for this problem is to use quaternary number system. The interconnections will be more efficient when more than two levels of logics are injected into the single wire, this concept is known as multiple value logic (MVL) concept. This multi value logic concept improves overall information efficiency. The routing area for quaternary logic design is two times smaller than the corresponding binary logic system. The arithmetic operations performed on quaternary number system are addition, subtraction and multiplication. The speed of operation of digital processors, computers are depending on the arithmetic unit. The quaternary adder performs carry free addition hence no carry is generated at the output and because of this quaternary adder is faster as compared to binary adder. The benefits of multi value logic implementation technique were considered for application in the reconfigurable domain. A new lookup table (LUT) structure was proposed where the information is represented by quaternary values. A new quaternary logic cell was presented and a result demonstrates interesting area and power reductions in comparison to equivalent binary structures. Some of the benefits of multi value logic include increased data density, reduced dynamic power dissipation, increased computational ability. The drawback of this multi value logic implementations are that they either based on current mode devices or demands extra steps in the fabrication process.

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II. RELATED WORK

In quaternary adder which is made up of radix 4 system, the operations performed are carry free addition and borrow free subtraction. The addition performed here is carry free addition so the speed of operation is very fast in comparison with standard adders [1]. In this paper standard CMOS design is used to design adder. Clock boosting technique is used to optimize the switches resistance and power consumption. In CMOS technology the full adder prototype based on LUT works at 100 MHz and it consumes power of 122 μ W [2]. The result shows efficiency of the proposed design. In quaternary adder the number of input bits are independent, the final result we get has the constant delay this delay is not depend on number of input bits i.e. when the input is of 4 bit, 8 bit, 16 bit, 32 bit and more, the delay is same. So for the higher number of bits and complex circuit the delay is independent. The current mode circuit allow successful improvement in terms of area. In the voltage mode look up table the major problem is power dissipation and it uses standard CMOS process, the threshold voltage is different for different transistors hence more number of fabrication steps are required and this is very expensive.

III. METHODOLOGY

In digital systems like computers and digital signal processors arithmetic operation plays a very important role. Arithmetic operations based on binary number system include problems like higher propagation delay, circuit complexity. When the number of bits increases the hardware also increases which means complexity goes on increasing. According to moor's law the number of transistors in an integrated circuit has doubled approximately every two years hence in integrated circuits the number of components goes on increasing because of this interconnects increases, nearly 70 percent area of the chip is occupied by interconnections. This problem can be overcome by multiple value logic concepts. The QSD numbers are both positive and negative numbers. The input to the system is binary numbers, the binary to quaternary conversion unit converts binary input to the quaternary and then it proceeds towards the quaternary adder unit. The quaternary adder unit performs the arithmetic operations like carry free addition on the input data. Finally the output of the quaternary adder unit is given to the quaternary to binary conversion unit to convert it back to binary form.

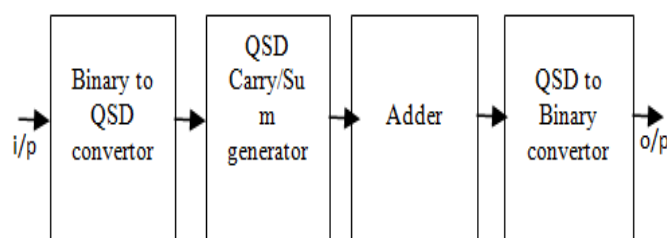


Fig. 1. Block Diagram of Quaternary Adder

3-bit 2's complement representation is used for QSD numbers. The formula for decimal conversion is given below.

$$D = \sum_i^n x_i 4^i \text{eq. (1)}$$

Where, x_i be any value between -3 to 3. The quaternary signed digit negative number is represented by complementing the positive QSD number. For applications like image processing, video processing requires large number of bits i.e. 64, 128 or more, this is achieved using quaternary adder because it gives output at constant delay i.e. output does not depend on the number of input bits. This constant delay gives the faster addition, subtraction of higher number of bits. This quaternary number system also used to store large data, the circuit will be less complex and hence less number of components is present in the system.



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IV. ADDER/SUBTRACTOR DESIGN

In arithmetic operations adder plays a very important role. To reduce the operation time carry free addition and borrow free subtraction is done. The two steps are available for carry free addition. These two steps involves the generation of intermediate sum and carry and this previously generate intermediate carry is added with current intermediate sum. There are also two rules to avoid carry propagation chain. These two rules says that the sum should not be greater than 2 and carry should not be more than 1 hence by this two rules the addition of second step adder is not greater than 3 and hence it will be single digit QSD number. The range of addition of all combination of addend and augend is from -6 to 6 which are shown in table I.

Table II. Addition of All Combination of Addend and Augend

A \ B	-3	-2	-1	0	1	2	3
-3	-6	-5	-4	-3	-2	-1	0
-2	-5	-4	-3	-2	-1	0	1
-1	-4	-3	-2	-1	0	1	2
0	-3	-2	-1	0	1	2	3
1	-2	-1	0	1	2	3	4
2	-1	0	1	2	3	4	5
3	0	1	2	3	4	5	6

The above all combinations of addend and augend have the range between -6 to 6. The QSD number representation of this combination is shown in table II. There are multiple representations for these numbers but the numbers which strictly follow the rules are chosen. The representations of the QSD numbers are in a 3 bit 2's complement binary number. The intermediate carry lies from -1 to 1 and because of this it require two bit binary number.

Table II. The QSD Represented and Coded Numbers

Sum	QSD represented number	QSD coded number
-6	$\bar{2}2, \bar{1}2$	$\bar{1}2$
-5	$\bar{2}3, \bar{1}1$	$\bar{1}1$
-4	$\bar{1}0$	$\bar{1}0$
-3	$\bar{1}1, 0\bar{3}$	$\bar{1}1$
-2	$\bar{1}2, 0\bar{2}$	$0\bar{2}$
-1	$\bar{1}3, 0\bar{1}$	$0\bar{1}$
0	00	00
1	01, $\bar{1}3$	01
2	02, $\bar{1}2$	02
3	03, $\bar{1}1$	$\bar{1}1$
4	10	10
5	12, $\bar{2}3$	11
6	12, $\bar{2}2$	12

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In the next step the intermediate carry from LSB is added with the sum of the current digit to get the final output because of the previously defined two rules, the next carry is not produce and hence no carry propagation should occurs. The addition in this step has the range from -3 to 3 which is single digit QSD number.

Table III. The Input and Output of Second Step Adder

Input				Output		
QSD		Binary		Decimal	QSD	Binary
A _i	B _i	A _i	B _i	Sum	S _i	S _i
1	2	01	010	3	3	111
1	1	01	001	2	2	010
0	2	00	010	2	2	010
0	1	00	001	1	1	001
1	0	01	000	1	1	001
-1	2	11	010	1	1	001
0	0	00	000	0	0	000
1	-1	01	111	0	0	000
-1	1	11	001	0	0	000
0	-1	00	111	-1	-1	111
-1	0	11	000	-1	-1	111
1	-2	01	110	-1	-1	111
-1	-1	11	111	-2	-2	110
0	-2	00	110	-2	-2	110
-1	-2	11	110	-3	-3	001

In the first step of addition the QSD carry/sum generator generates the 3 bit sum and the 2 bit carry, this 2 bit generated carry is given to the second step QSD adder which adds the previously generated carry with the current sum and finally the result is obtained. The QSD carry/sum generator and Second step QSD adder is shown in figure 2 and figure 3.

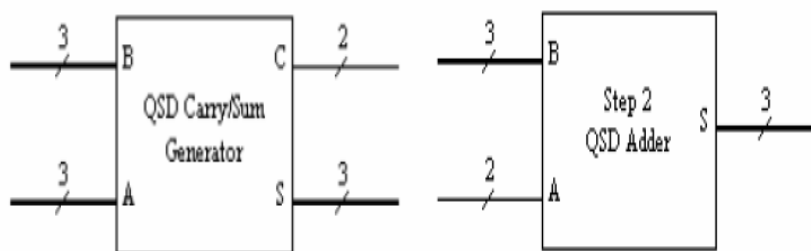


Fig. 2. QSD Carry/Sum Generator Fig. 3. Second Step QSD Adder

To implement the n-digit QSD adder, it requires n number of QSD sum and carry generators with the n-1 QSD adders which shown in figure 4.

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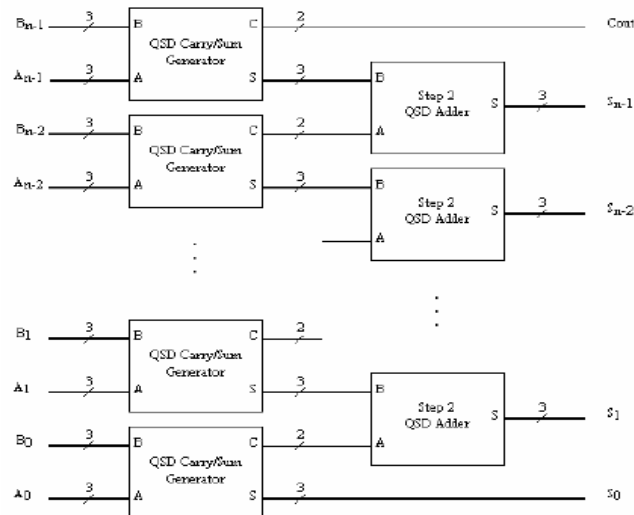


Fig. 4. QSD adder for n number of digits.

V. SIMULATION RESULTS

The QSD adder programming is written in VHDL and implemented on Spartan 3A (XC3S200A) FPGA board. The simulation is done on Modelsim and the simulation results are shown in the following figures. The figure shows simulation result of quaternary adder. The overall delay of the quaternary adder is total of conversion delay and computation delay.

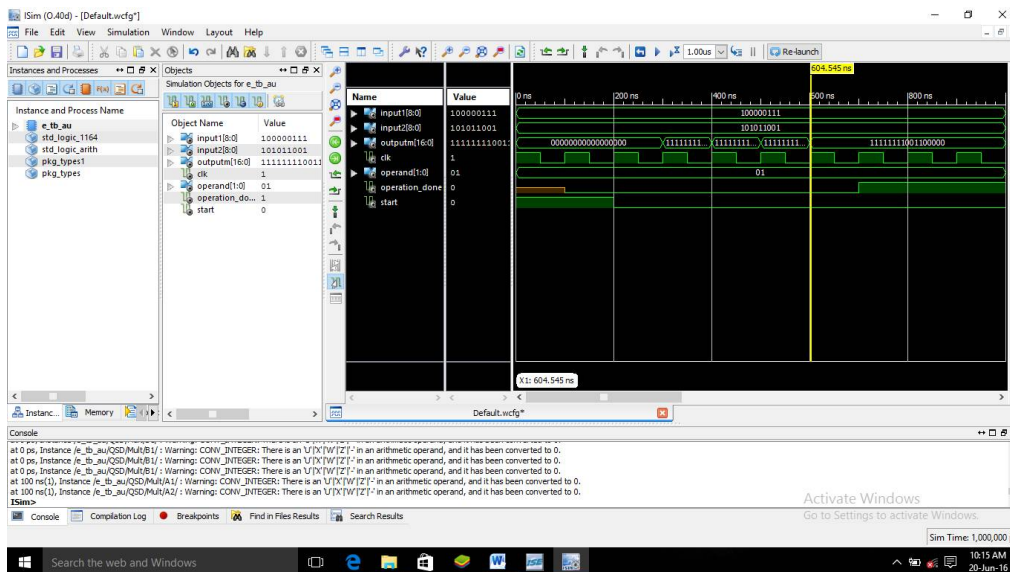


Fig. 5. Simulation Result of Quaternary Addition



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VI. CONCLUSION AND FUTURE WORK

The quaternary adder is designed and implemented on Spartan 3A FPGA board. The result shows that the performance of quaternary adder is better than binary adder. The quaternary signed digit adder, subtractor is better than any other adder because there is a constant delay which is not depending on number of input bits. Using QSD addition different algorithms for arithmetic operation can be directly implemented. The conversion of binary to quaternary circuit is feasible and efficient in terms of power consumption and speed while being implemented in a standard CMOS technology. As technologies are becoming more complex, multi valued logic (MVL) will be the future of circuit design. Since the research is still in initial stage on MVL the work is fundamental. When hardware implementation using MVL circuits is famous and more exposed to companies then one day MVL will surely turn over the binary logic. The advantages of lower power, higher performance, and reduced interconnect congestion motivate the use of quaternary circuits in a wide variety of applications.

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