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Low Power Memory Circuits Design using CMOS and Beyond CMOS Devices: A Study

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ABSTRACT: - Over the past 4/5 decades, the success story of CMOS technology scaling has truly revolutionized the life-style of human beings. Alot of challenges are, however, being faced for further downscaling of the devices. In particular, finding an optimal solution to come up with a device with relatively easier fabrication technology and higher speed of operation at manageable power dissipation is the key challenge. In today's world of consumer electronics there is a requirement of high frequency circuits which is having low power consumption so that it can be used in designing battery driven handheld devices. On the other hand there is a huge requirement of CMOS technology compatible device which can be used as power amplifiers for communication devices like repeaters and routers. In this paper the study of different types of CMOS circuit and analysis.

KEYWORDS:- CMOS Circuit, Low Power, Power Dissipation

I. INTRODUCTION

In today's age, the mankind and its societies have become explicitly technology dependent on every possible level. Everywhere in our daily life, e.g., from our leisure time to official works, transports to residences, newspapers to communications, amusements to security, etc., sophisticated electronic gadgets rule the modern human mind. Consequently, the market is becoming extremely competitive and as to survive in the market, technocrats weigh the important factor of cost effectiveness in every level from R&D of better electronic devices to their marketing. To decrease the cost & increase the performances of the electronic devices the semiconductor industry increases the package density of the electronic devices, in accordance with Moore's law [1]. As per Moore's law, the number of transistors integrated into an IC chip doubles in every two years by scaling the devices. Successive down scaling of transistors now has been reached below 20 nm technology and such technology faces lots of challenges due to scaling. For example, the drive current of the device is inversely proportional to the length of the channel that is directly proportional to the scale of that device [2, 3]. Due to the downscaling, when drive current increases, high frequency operation is observed for those devices. Simultaneously, the short channel length increases the leakage current as well as power dissipation for those devices. So it is very challenging to get a device with higher frequency at lower power dissipation. The overall aim of the current technology available in this field is to find the optimization between the frequency and the power dissipation. Intel has already incorporated FinFET technology in the market but as per performance parameters, this FinFET technology has also saturated. Some advanced CMOS devices like junctionless transistor, Negative capacitance transistor with better performances than conventional CMOS devices are currently being investigated. Those advanced CMOS devices also provide us with higher frequency of operation, lower sub-threshold swing, lower leakage current and many other better performance characteristics over conventional MOSFET technology [4].

II. LITERATURE REVIEW

Sai Srinivas Chandra et al. [1], rogue third parties and rogue foundries have emphasized the importance of hardware security in the real world. Due to globalization of the integrated circuit (IC) design line in semiconductor industry, hardware security issues need to be taken to prevent intellectual property (IP) Copyright infringement. Logical encryption is an effective method to protect circuits against IP hacking, reverse engineering, and spoof malicious ICs to insert trojans. Researchers have proposed many logical ciphers leads to overloads in circuit design parameters such as area, capacity, and efficiency. This article aims to compromise between these parameters, security is the main key and secure the design metrics by proposing a new logic coding method at the

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transistor level for CMOS ports. Experimental results show that, when using the proposed encryption key gateways, Design costs such as area, capacity, latency and energy are reduced by an average of 42.94%, 37.37%, 26.79%, and 50.96%, respectively, compared with existing topologies based on logical encryption.

K. Rajashekhar et al. [2], threshold voltage scaling causes sub-threshold leakage current to rise in CMOS circuits. Leakage power dissipation is the most important power dissipation technique in CMOS (complementary metal oxide semiconductor) circuits due to scaling down silicon technology. The device becomes more productive as its power consumption is reduced. As a result, CMOS technology became the most widely used technology for low-power devices. Reduced voltage supply causes reductions in quadratic dynamic power loss and linear leakage power loss. Due to leakage, weak inversion current is the most likely candidate for the utilization of standing power. It is difficult to design a CMOS circuit with no leakage current. The power dissipation of VLSI (Very-large-scale integration) CMOS circuits can be reduced in a limited number of effective ways. For reducing CMOS logic circuit leakage current, propagation delay, and power, a stack ONOFIC circuit is presented here. Inverter based CMOS rationale circuits are used for addressing the impact of introduced plot in CMOS circuits. In order to demonstrate a comparable reduction in terms of delay and dissipation, a comparison is made between the presented scheme and one of the reduction methods, such as LECTOR.

H. You et al. [3], Flip-flops (FFs) can significantly reduce the power consumption of digital systems by optimizing their power consumption as fundamental components. An energy-efficient retentive true-single-phase-clocked (TSPC) FF is suggested in this article. The proposed TSPC FF uses an input-aware precharge scheme and only precharges when absolutely necessary. To further guarantee the FF's high energy efficiency without significantly increasing its area, floating node analysis and transistor level optimization are utilized. Postlayout simulations using SMIC 55-nm CMOS technology show that the proposed FF consumes 84.37% less power at 10% data activity than a conventional transmission-gate flip-flop (TGFF) at 1.2 V supply voltage. As the data activity decreases to 0%, the reduction rate rises to 98.53 percent. At 10% data activity, the proposed FF consumes only 0.411 fJ/cycle, 84.23% less than TGFF, when the supply voltage drops to 0.6 V. The proposed FF's high energy efficiency is demonstrated by the measurements of ten test chips. A method for predicting the yield distribution of CMOS circuits based on electrical parameter distributions is presented, and the CK-to-Q delay of the proposed FF is 26.18 percent lower than that of the TGFF at a supply voltage of 1.2 V. In order to project the yield of the circuit within a particular design window, this method makes use of the mean and standard deviation of the measured threshold voltage as well as the mobility of NMOS and PMOS transistors. The bivariate normal distribution of the transistor parameters serves as the foundation for the prediction method, which is based on a probability model. It is demonstrated that the circuit designer's design window has a significant impact on the predicted yield. As a result, the method offers a quantitative approach for evaluating tradeoffs between design windows and product yield.

Ritesh Ray Chaudhuri et al. [4], in CMOS circuits, the decrease of the edge voltage because of voltage scaling prompts expansion in sub limit spillage current and thus, static power disperses. Power dissipation and process parameter variations have emerged as major design considerations in the nanometer technology regime. Leakage power continues to become a major source of power consumption, resulting in these issues. On the other hand, variations in circuit parameters like delay and leakage are translated by systematic and random variations in the parameters of the device. The International Technology Roadmap for Semiconductors (ITRS) predicts that leakage power dissipation will grow at an exponential rate over the next ten years. Because of their lengthy idle times, portable battery-operated devices like cell phones and PDAs are directly affected by this. This paper examines a number of methods for effectively reducing leakage power loss. Here, we present a comparison of CMOS inverters with low leakage power. The results show that the sleepy stack technique uses 52% less power than the standard CMOS technique in 45nm technology.

Laxmi Kumre et al. [5], power dissipation has emerged as an important indicator of chip performance with the development of integrated circuits (ICs). The sources and types of chip power dissipation are first discussed in this paper, followed by an introduction to static and dynamic power dissipation analysis techniques and IC chip digital layout design stage power dissipation analysis and optimization methods.

Xiaoke Tang et al. [6], leakage power dissipation has increased in importance among all power dissipation mechanisms of complementary metal oxide semiconductor (CMOS) circuits as silicon technology has decreased. A standby leakage power reduction method for combinational logic circuits is the minimum leakage vector (MLV). Even though power gating is a superior method for reducing leakage power when compared to MLV standalone power gating, there are some inherent disadvantages, such as a longer wake-up time and circuit state loss. In this paper, we combine MLV and power gating to overcome the disadvantages of full circuit power gating and reduce leakage power

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more than with MLV alone. We devised a straightforward linear-time algorithm as an alternative to full-circuit power gating to identify the gates with the highest leakage power dissipation around which power gating can be performed when combination logic is fed with its MLV. The circuit's flip flops and input ports were altered to feed MLV in both scan mode and standby mode. Flop modifications also make it easier to do partial power gating in the flops when they are in standby mode, and the flops' states are kept so that they stay the same when the circuit switches back to active mode. Fast HSPICE simulations were used to test our proposed combinational approach with four selected ISCAS89 benchmarks. We were able to reduce standby leakage power by 30% to45% more than a standalone MLV implemented with blocking logic with a maximum of 5% extra area trade off.

S. Thayaparan et al. [7], power leakage is a major issue that needs to be addressed as technology progresses. The MTCMOS method has proven to be the best for significantly reducing power consumption in standby mode while maintaining acceptable performance in active mode. To address the design issues presented by MTCMOS, additional design effort is required. It is presented a self-sleep circuit with improved performance that does not require the distribution of a sleep signal.

R. Rao et al. [8], MTCMOS sleep-wake scheduling can be implemented more easily thanks to this circuit. The tests and complexities of sleep signal distribution in a distributed MTCMOS design are the focus of this work. It has been designed a self-sleep circuit that uses less power, takes up less space, and has less delay. The self-sleep circuit uses 90nm technology and operates at a 2-Giga Hertz clock frequency. It performs well in active mode and eliminates sleep distribution network overheads, allowing for swift transitions between active and standby modes.

S. Chaudhary et al. [9], a novel approach to reducing sub-threshold leakage current is presented in this paper. Leakage-controlled transistors are used to dynamically alter the ground voltage level in response to the logic gate's output voltage level. Leakage controlled transistors (LCTs) are used to maintain delay performance while simultaneously reducing leakage power and static energy consumption (static power-delay product). The proposed method outperforms conventional designs in terms of performance, as demonstrated by simulation results based on the 32nm Berkeley predictive technology model.

III. POWER DISSIPATION

Power dissipation in digital logic circuits can be broadly divided into two categories: dynamic power dissipation and static or leakage power dissipation. Dynamic power dissipation is mainly caused by the current flow due to charging and discharging of parasitic capacitances in the logic circuit. Static power dissipation occurs during the static input states of the device [10, 11]. With the down scaling in technology, contribution by static power dissipation increases in the overall power dissipation. In deep submicron CMOS technologies, the role of sub threshold leakage power dissipation becomes dominant among other leakage power components because of down scaling in technology. Under such condition, the static power dissipation is approximately equal to the sub threshold leakage power dissipation and is expressed as

$$P_{Static} \approx P_{Subthreshold} \tag{1}$$

A general formula for the total power dissipation in a digital logic circuit in deep submicron CMOS technologies can be expressed as

$$P_{total} = P_{dynamic} + P_{static} \tag{2}$$

$$P_{total} \approx P_{dynamic} + P_{subthreshold} \tag{3}$$

Where $P_{dynamic}$ is the dynamic power dissipated by the circuit, $P_{subthreshold}$ is the switching component of the power caused by charging/discharging of the circuit output load capacitance C_l, and P_{sc} and P_l reflect the power dissipated due to short- circuit and leakage currents respectively(I_{sc} and I_l). By employing appropriate design techniques both short circuit and leakage current should be reduced to a negligible level leaving the charging and discharging of the node capacitances as the dominant factor of power consumption [12].

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IV. CMOS INVERTER

Figure 1 depicts the schematic structure of the CMOS inverter with a load capacitance CL. To consider the effects of parasitic capacitance in the transient analysis, we use two different values of CL as 1.5 × Cgg and 2 × Cgg. Here, Cgg is effective gate capacitance of the n- and p-FinFETs in parallel. As the parasitic capacitances cannot be estimated accurately for the simulation study, the use of two different values of CL allows us to capture the effect of varying values of the parasitic capacitance. Cgg values used in this study are 44, 34, and 27 aF (33, 25, and 19 aF) for 14-, 10-, and 7-nm technology nodes, respectively, for the devices with spacer (without spacer). The method of estimation of Cgg has been described in [13].

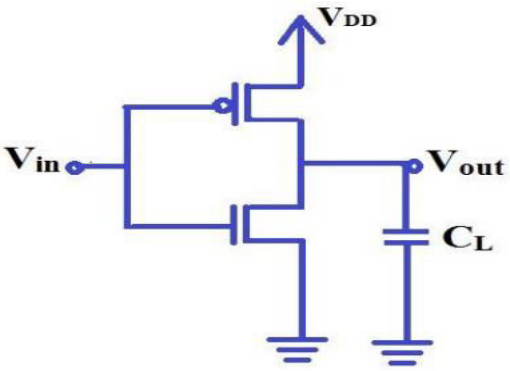

Figure 1: Schematic of the CMOS inverter

Voltage transfer characteristics (VTCs) for both types of inverters consisting of devices with and without spacer for CL = 1.5 × Cgg are shown in Figure 2. The variation in the inverter threshold voltage is observed in Figure 4.4 for different inverters, which is due to the variation in ID values for different devices, as observed in Table 4.2 [4.35]. It may be noted that the presence or absence of a spacer does not make much of a difference in the VTC of either type of inverters.

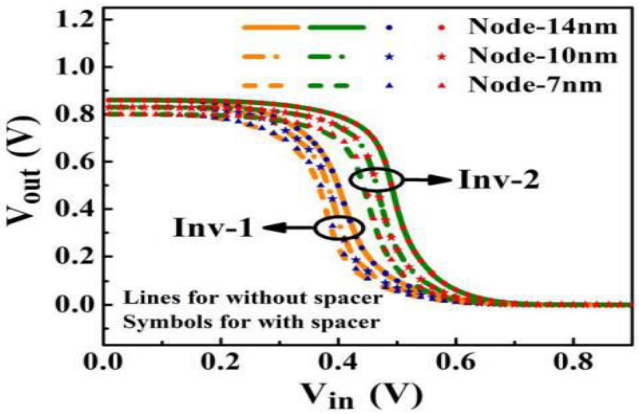

Figure 2: Voltage transfer characteristics both with and without spacer at CL = 1.5× Cgg for three different technology nodes.

NAND Gate: - The Figure 3 inferences the digital schematic diagram for basic NAND gate using microwind tool.

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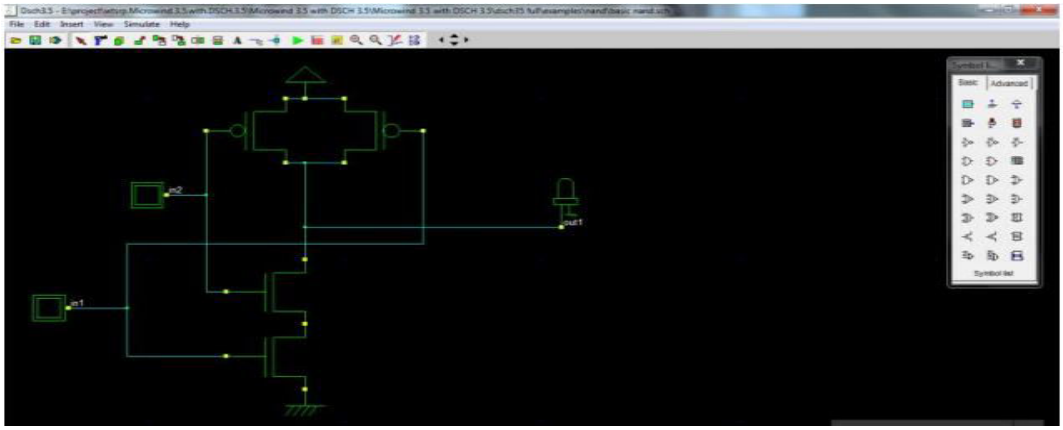

Figure 3: Design of basic NAND gate

The Figure 4 inferences the digital schematic diagram for basic NOR gate using microwind tool.

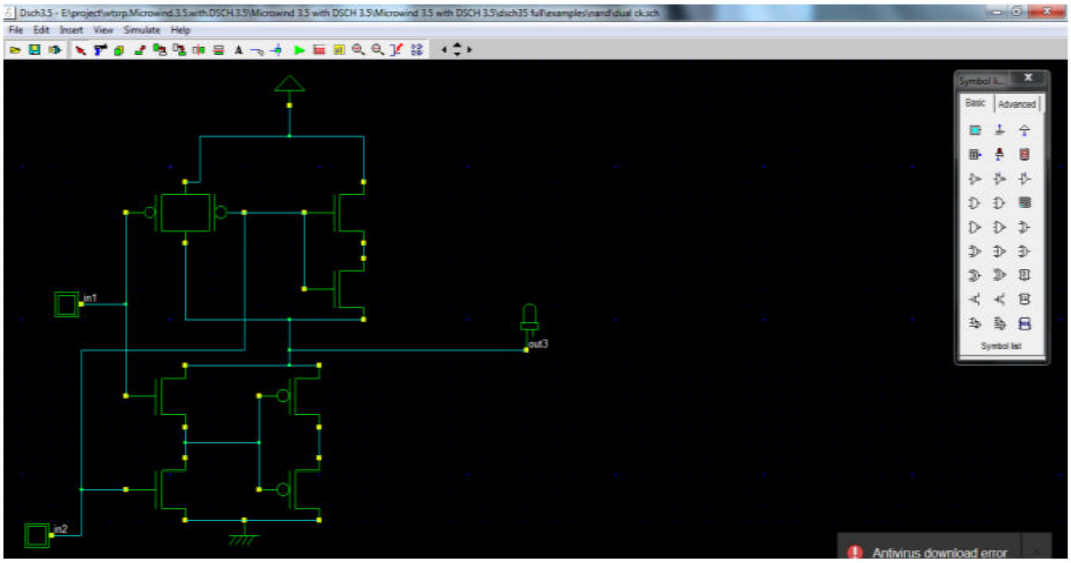

Figure 4: Basic NOR gate

V. CONCLUSION

The design of integrated circuits capable to work under low voltage and low power constraints has observed a very considerable boom and sought attention of contemporary researchers. Reducing supply voltage and power consumption of integrated circuits is a crucial factor since in general it ensures the device reliability, prevents overheating of the circuits and in particular prolongs the period of operation of devices with the available battery. The ever growing electronic industry encounters many advances in digital signal processing as digital domain functions form about eighty percent of the overall functionality of the chip [10-13]. Low voltage CMOS digital circuits are useful in the design of microelectronic systems as they find varied applications ranging from cellular phones, data communication equipment to home audio entertainment centers.

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