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VLSI Architecture for Kogge- stone High Speed Addition Technique using XOR Gate

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ABSTRACT: In this Technical era the high speed and low area of VLSI chip are very- very essential factors. Day by day number of transistors and other active and passive elements are growing on VLSI chip. In Integral part of the processor adders play an important role. In this paper we are using proposed kogge-stone adders for binary addition to reduce the size and increase the efficiency or processor's speed. Proposing kogge stone adder provides less components, less path delay and better speed compare to other existing kogge stone adder and other adders. Here we are comparing the kogge stone adders of different-different word size from other adders. The design and experiment can be done by the aid of Xilinx 14.1i Spartan 3 device family.

KEYWORDS: Kogge Stone Adder, Ripple Carry Adder, Proposed Kogge Stone Adder, 14.1i Spartan 3 Device Family.

I. INTRODUCTION

The processor's speed mostly depends on adder design techniques. Adder is the device by which two or more than two bit information can be added. For the high speed processing of the data transfer area must be less of the passive and active element. Adder has two outputs specially sum and carry. For making fast adder carry can be reduced and replaced in different ways. The propagation delay or gate delay of a gate is basically the time interval between the application of the input pulse and the occurrence of the resulting output pulse. The propagation delay is a very important characteristic of logic circuits because it limits the speed at which they can operate. The shorter the propagation delay, the higher the speed of the circuit and vice-versa. Propagation delay should be minimizing as possible as, for high efficient addition. For instance 4 bit addition generally propagation delay is occurred highly.
When we add one high bit to another high bit carry is occurred due to normally addition operation, shown in figure 1. This carry propagates to next bit and now bit addition is performed by 3 bit adder. So carry will propagate to the next bit over and over, this cause propagation delay will be occurred. On the other hand propagation delay can be reduced by the aid of suitable structural designing process. For instance full adder can be designed with one XOR gate, three AND gate and one OR gate. That type of designingwill provide 8.326 ns propagation delay. On the other hand full adder can be design by using two half adder and one OR gate.This type of designing will provide only 8.036 ns propagation delay.

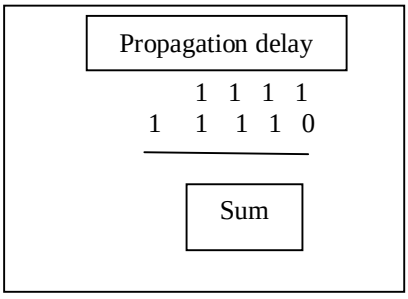

Figure 1: Propagation delay in bit addition

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Carrypropagation delay can be reduced by using ripple carry adder, fast adder that is also called look a-head carry generator, parallel adder, and specially kogge stone adder.

II. RIPPLE CARRY ADDER

Ripple carry is a combinational circuit for adding more than two bit information. It is also called parallel adder. Ripple carry adder can be designed by using full adder in cascading form. Carry output of first full adder is connected with input of the next full adder, so carry is rippled from one adder to another adder. That is by it is called ripple carry adder.

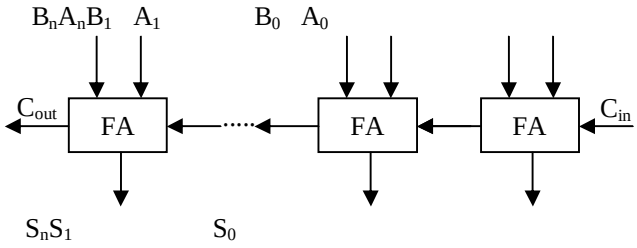

Figure 2:N-bit Ripple Carry Adder

$$S_0 = A_0 \oplus B_0 \oplus C_{in} \quad (1)$$

$$C_0 = (A_0 * B_0) + (B_0 * C_{in}) + (C_{in} * A_0) \quad (2)$$

$$S_1 = A_1 \oplus B_1 \oplus C_0 \quad (3)$$

$$C_1 = (A_1 * B_1) + (B_1 * C_0) + (C_0 * A_1) \quad (4)$$

$$S_2 = A_2 \oplus B_2 \oplus C_1 \quad (5)$$

$$C_2 = (A_2 * B_2) + (B_2 * C_1) + (C_1 * A_2) \quad (6)$$

$$S_n = A_n \oplus B_n \oplus C_{n-1} \quad (7)$$

$$C_n = (A_n * B_n) + (B_n * C_{n-1}) + (C_{n-1} * A_n) \quad (8)$$

III. KOGGE STONE ADDER

Kogge Stone Adder was proposed by Peter M. Kogge and Harold S. Stone. Kogge Stone Adder is an advanced technology of Look a- head Carry Adder. That is also called parallel prefix adder. It has more area than to Brent Kung Adder but less Fan-out. This adder provides the carry signal $O(\log n)$ time and become fastest adder for industrial level.

First block of KSA (Kogge Stone Adder) is Pre- Processing that will generate and propagate the carry. Processing of carry will be done over the carry processing area and all the carry signal go through the post processing block. In the pre preprocessing stage we find the, generate and propagate signals from each inputs. Propagating and generating equation can be shown in equation 9&10.

$$P_n = A_n \oplus B_n \quad (9)$$

$$G_n = A_n * B_n \quad (10)$$

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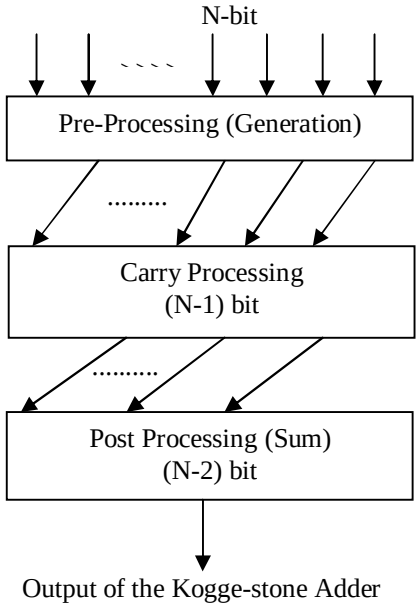

Figure 3: Block Diagram of Kogge-stone Adder

Carry processing stage provides the carries corresponding to each bit. Execution of these bit operation is carried out from parallel. After finding the carries in parallel they are segmented in to smaller pieces. Carry equations can be shown in equations 11&12.

$$CP_{n-1} = P_{n-1} * P_n \quad (11)$$

$$CG_{n-1} = (P_n * G_{n-1}) + G_n \quad (12)$$

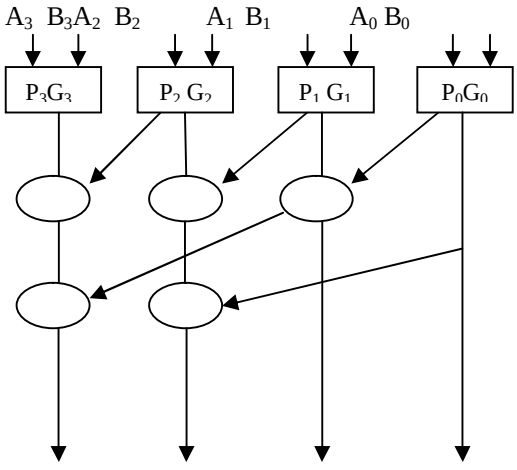

Figure 4: Function Diagram of 4-bit Kogge-stone

Above diagram is a functional diagram of kogge stone adder for 4 bit addition. Here elliptically symbol defined as a carry processing stage. The output of the preprocessing stage is fed to next carry stage and post processing as well.

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IV. MODIFIED KOGGE STONE ADDER

The main object of this paper is to reduce the route delay and logic delay. As soon as we increase the bit for addition in kogge stone adder area will be increased. So, area and propagation delay can be reduced by the aid of modified KS adder. This adder will be designed like as ripple carry adder. Carry output of one KS adder is connected with another KS adder but this method is very beneficiary for high efficient digital devices as per concerning propagation delay.

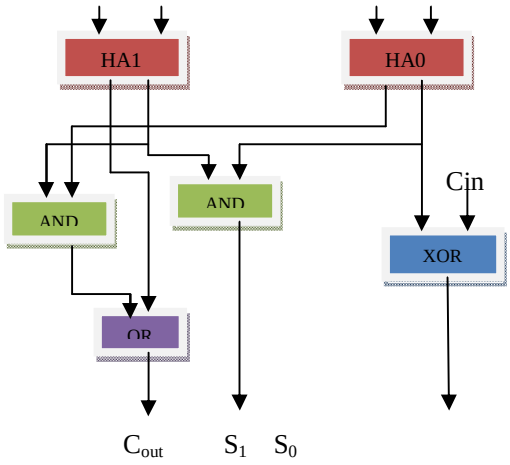

Figure 5- Logic diagram of modified 2 bit KS adder

Generally, 2 bit KS adder is comprised with two half adder, two AND gate, one XOR gate and one OR gate. Area of the any circuit is played an important role. Area can be calculated with the help of number of primary gates. Primary gates are AND, OR and NOT.

Table 1: Calculation of gates in logic circuit

Gate & Devices	Number of gates	Propagation delay
AND	1	1
OR	1	1
NOT	1	1
XOR	5	3
Half adder	6	3

This table shows that how to calculate area of any logic circuit and area of any circuits must be less as possible as. So here our proposed kogge stone adder has less area than other adder existing adder.

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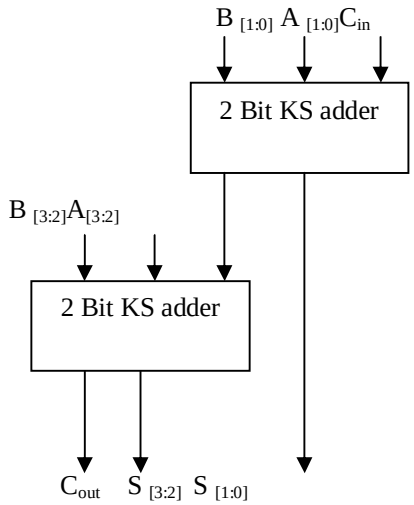

Figure 6:Modified 4-bit Kogge stone adder

Above diagram is same like as ripple carry adder. This modified structure provides less propagation delay and less area than to other adder. This adder can be enhanced by cascading structure designing.

V. SIMULATION ANALYSIS

Simulation of these experiments can be done by using Xilinx 14.2 i VHDL tool. In this paper we are focusing on propagation delay. Propagation delay must be less for better performance of digital circuit.

```
Device utilization summary:
---------------------------

Selected Device : 3s50pq208-5

 Number of Slices:                        5  out of    768     0%
 Number of 4 input LUTs:                  9  out of   1536     0%
 Number of IOs:                          25
 Number of bonded IOBs:                  25  out of    124    20%
```

Figure 7: Device Utilization for 8-bit

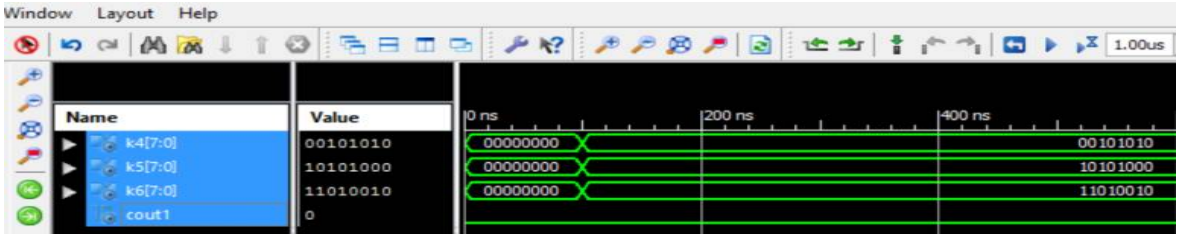

Figure 8: Output waveform of the 8-bit KS Adder

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Device utilization summary:
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Selected Device : 3s50tq144-5

 Number of Slices:                        9  out of    768     1%
 Number of 4 input LUTs:                 16  out of   1536     1%
 Number of IOs:                          48
 Number of bonded IOBs:                  48  out of     97    49%
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Figure 9: Device Utilization for 16 bit KS Adder

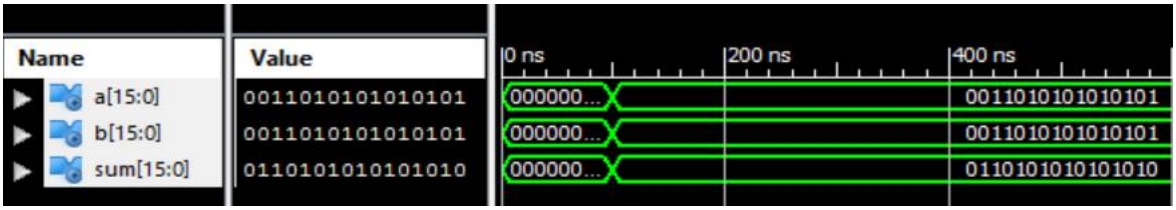

Figure 10: Output waveform of the 16-bit KS Adder

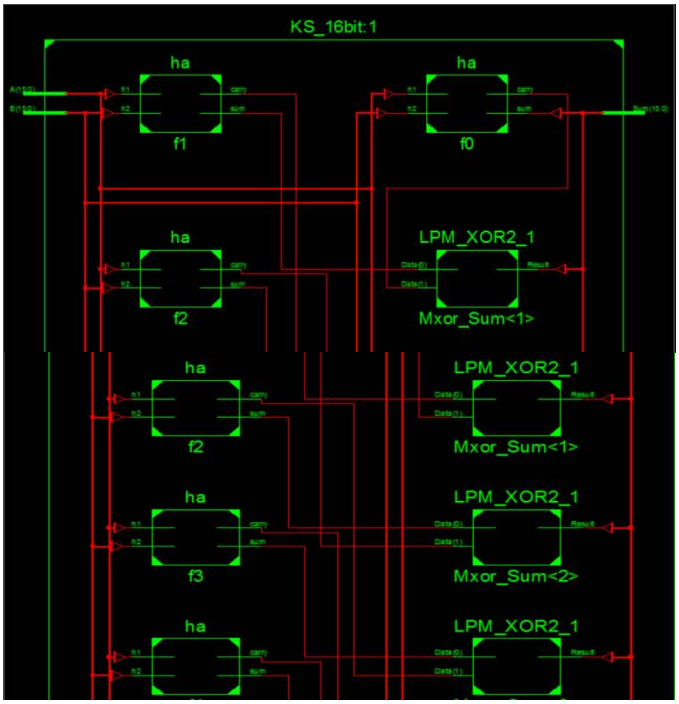

Figure 11: RTL View of the 16-bit KS Adder

Table 2: Comparison of Kogge stone from other adders

Word size	Adder	Area	Delay(ns)
8 bit SQRT CSLA	Regular (RCA)	144	11.92
	BEC	132	13.69
	Modified (CBL)	111	11.15
	Proposed Kogge Stone	83	7.959

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16 bit SQRT CSLA	Regular (RCA)	348	16.15
	BEC	291	18.77
	Modified (CBL)	276	15.48
	Proposed Kogge Stone	166	14.85
32 bit SQRT CSLA	Regular (RCA)	698	28.97
	BEC	762	34.44
	Modified (CBL)	552	26.23
	Proposed Kogge Stone	332	24.56
64 bit SQRT CSLA	Regular (RCA)	1592	52.82
	BEC	1498	64.61
	Modified(CBL)	1104	47.74
	Proposed Kogge Stone	664	43.25

VI. CONCLUSION

Eventually, all the digital processors are dependent on the adder structure and its properties, so here I am designing a modified and high speed adder that is modified KS adder which has less propagation delay. With the help of this adder we can design a fast multiplier which is main component for any processor.

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