ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 4, April 2017

A Survey on Reconfigurable Architecture Based on FPGA for OFDM Transmitter

Shephali Swami[1], Prof. V. B.Raskar[2]

Department of Electronics and Telecommunication Engineering, Imperial College of Engineering and Research, Wagholi, Pune, India. [1,2]

***ABSTRACT*:** OFDM is a special case of multi-carrier modulations, which is of great use in various wireless communications, such as DAB, DVB, HDTV, CMMB, TMMB, 802.11a. The OFDM frame structure is similar to each other.Nowadays, wireless mobile communications have expanded dramatically all over the world, leading to a need to increase their bandwidth capacity. One way to increase the capacity of a wireless mobile communication system is to improve the communication technology. Orthogonal Frequency Division Multiplexing (OFDM) is considered the technology for the next-generation broadband wireless systems. Therefore, the main communication blocks must be designed with high capability in terms of reconfigurability. This paper presents the architecture and implementation of a reconfigurable Orthogonal Frequency Division Multiplexing (OFDM) transmitter with such capabilities. This transmitter supports 4/16/64-QAM (Quadrature Amplitude Modulation) modulation in superimposed training (ST) and data-dependent superimposed training (DDST). The proposed architecture is capable of generating frames for the Long Term Evolution (LTE) standard and with minimal modifications can also generate frames for IEEE 802.11a and 802.11g standards. Results have shown a moderate FPGA (Field Programmable Gate Array) consumption and good SQNR (signal to quantization-noise ratio) performance of 50 dB average.

KEYWORDS: OFDM, LTE, FPGA.

I. INTRODUCTION

Orthogonal frequency division multiplexing (OFDM) is one of the multi-carrier modulation (MCM) techniques that transmit signals through multiple carriers. These transporters (subcarriers) have diverse frequencies and they are orthogonal to each other. Orthogonal recurrence division multiplexing systems have been connected in both wired and remote correspondences, for example, the uneven computerized supporter line (ADSL) and the IEEE 802.11 standard. It is outstanding that Chang proposed the first OFDM standards in 1966, and effectively accomplished a patent in January of 1970. Later on, Saltzberg broke down the OFDM execution and watched that the crosstalk was the extreme issue in this framework. Albeit each subcarrier in the foremost OFDM frameworks covered with the area subcarriers, the orthogonality can at present be protected through the amazed QAM (SQAM) procedure. Be that as it may, the trouble will rise when a substantial number of subcarriers are required. In some early OFDM applications, the quantity of subcarriers can be picked up to 34. Such 34 images will be affixed with excess of a protect time interim to wipe out intersymbol interference (ISI). Orthogonal recurrence division multiplexing (OFDM) is a strategy for encoding computerized information on various bearer frequencies. OFDM has formed into a mainstream conspire for wideband computerized correspondence, utilized as a part of utilizations, for example, advanced TV and sound telecom, DSL Internet get to, remote systems, control line systems, and 4G versatile interchanges. Orthogonal Frequency Division Multiplexing (OFDM) could be followed to 1950's yet it had turned out to be exceptionally mainstream at nowadays, permitting high speeds at remote correspondences. OFDM could be considered either a regulation or multiplexing procedure; its progressive system relates to the physical and medium get to layer. An essential OFDM framework comprises of a QAM or PSK modulator/demodulator, a serial to parallel/parallel to serial converter, and an IFFT/FFT module. The iterative way of the FFT and its computational request makes OFDM perfect for a devoted engineering outside or parallel to the principle processor. Utilizing FPGA rather than an ASIC gives likewise adaptability for

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 4, April 2017

reconfiguration, which is a requirement for the Software Defined Radio (SDR) idea. These days, remote portable interchanges have extended significantly everywhere throughout the world, prompting to a need to build their data transfer capacity limit. One approach to expand the limit of a remote versatile correspondence framework is to enhance the correspondence innovation. Specifically, Orthogonal Frequency Division Multiplexing (OFDM) is viewed as the innovation for the cutting edge broadband remote frameworks. In actuality, it has been embraced for some guidelines, for example, third Generation Partnership Project-Long Term Evolution (3GPP-LTE), Digital Audio Broadcasting (DAB), Digital Video Broadcasting–Terrestrial (DVB-T), Digital Video Broadcasting-Handheld (DVB-H), and IEEE 802.11.

II. MOTIVATION

The motivation of this paper is that the Future communication systems such as 5G will require high interoperability between standards, obligating current designs to contemplate the inclusion of multiple standards into a single device.

III. OBJECTIVES

The objectives of this paper are given below:

- To increase bandwidth capacity.
- To increase the capacity of a wireless mobile communication system is to improve the communication technology.

IV. LITERATURE SURVEY

In literature, the problem and the previous techniques of reconfigurable architecture is described

Revanna et.al In this paper the scalable radix-2 N-point novel FFT processor architecture based on a reasonable balance between performance, power, area, flexibility and scalability parameters was proposed. The versatile FFT processor was outlined, executed utilizing VHDL, simulated utilizingModelSim and integrated on an Altera Stratix V FPGA gadget 5SGSMD5K2F40C2. The FFT processor fulfills the prerequisites as far as speed, control, territory, adaptability and versatility required by wide scope of numerous remote norms, for example, IEEE 802.11a/g, IEEE 802.16e, 3GPP-LTE, DAB and DVB. Thus, the FFT processor engineering can be received in SDR stages supporting indicated different remote guidelines. The proposed engineering beats the current settled and variable length FFT processors as far as speed, power, region, adaptability and versatility. In addition, the processor architecture can also be adopted in any other applications where a reasonable balance between specified design parameters is essential.[1]
Bautista-Contreras et.al [2] in this paper, architecture for a reconfigurable computerized baseband transmitter under the SDR worldview was displayed. It has the capacity of select on-the-fly from three diverse plan of preparing: ST, DDST and express; seven distinctive sorts of balance: 4/16/64 QAM, BPSK, DBPSK, OQPSK, DQPSK and bolster for up to 32 sorts; the waveform of the beat forming channel; the length of the drive reaction of such channel; the upsampling component; the recurrence operation of the clock base and the information rate. Comes about demonstrate that it accomplished couple of assets of the focused on FPGA (< 1% of the total resources) at a frequency operation adequate its use in practical communication standards [2]
Zhang, B. et.al [3] It has been presented that the entire outline can fit for OFDM modulators of various remote wireless standards with different IFFT length, sub-carrier index, cyclic prefix and guard interval, whose resource consumption is quite low as well. Additionally, executing this work on FPGA demonstrates that the SDR idea can be acknowledged on current customary gadgets like Twister IV arrangement. Reducing repetitive work makes the system design more convenient and efficient.[3]
This work was performed utilizing abnormal state apparatuses like System Generator and displaying devices asMatLab and Simulink that encourage this undertaking. The outcome displayed demonstrated that is conceivable to actualize an OFDM modulator for IEEE Std. 802.11a utilizing an accessible gadget like Virtex 2 (utilizing around 10 % of the accessible assets). These outcomes demonstrate that genuine gadgets could bolster the SDR idea at IF preparing level even at high number juggling requesting benchmarks or prepare. It is achievable to decrease more assets utilizing

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 4, April 2017

VHDL improving procedures like the work introduced by M. Canet . However that optimization would require much more time than using a high level tool.[4]

Zhang, B.et.al [5] . It has been introduced that the entire plan can fit for OFDM modulators of various remote norms with various IFFT length, sub-bearer file, cyclic prefix and protect interim, whose asset utilization is very low too. Additionally, executing this work on FPGA demonstrates that the SDR idea can be acknowledged on current common gadgets like Cyclone IV arrangement. Diminishing redundant work makes the framework plan more helpful and proficient [5].

Garcia, J. et.al [6] second International Conference on, 2005. It has been introduced the entire plan, approval and usage of an OFDM modulator consistent with the Std. IEEE 802.11a. This work was performed utilizing abnormal state instruments like System Generator and demonstrating devices as MatLab and Simulink that encourage this assignment. The outcome exhibited demonstrated that is conceivable to actualize an OFDM modulator for IEEE Std. 802.11a utilizing an accessible gadget like Virtex 2 (utilizing around 10 % of the accessible assets). These outcomes demonstrate that real gadgets could bolster the SDR idea at IF handling level even at high number-crunching requesting benchmarks or process [6].

Mr. Rahul et.al [7] The primary reason for this project is that, they can move the flag from low recurrence to the high recurrence and from high recurrence to low recurrence i.e.vice-versa. So that a same flag can be utilized as a part of two or more recurrence extents. It implies that if one recurrence range is not accessible then they can move it on another scope of recurrence. It is been implemented using OFDM model. At the same time they are going to find the Bit Error Rate (BER) & Peak to Average Power Ratio (PAPR).[7]

MeghanaShetty et.al [8] an architecture for DS-CDMA/CI transmitter utilizing Cordic Algorithm. As the framework generator configuration show sets aside more range and opportunity to play out the operation, it is thusly actualized utilizing the FPGA to lessen the range furthermore, control. The design utilizes CORDIC Square to create transporter and to keep away from utilization of complex augmentations the stage counterbalance equal to spreading code is added to the stage generator yield. Code selector piece adds runtime re-configurability to the model. At that point these modules are actualized in SPARTAN3 FPGA by utilizing Xilinx ISE 13.4 and mimicked in modalism 6.3f. The Chip scope master Analyzer is utilized to see the execution after effects of FPGA.[8]

V. PROPOSED SYSTEM

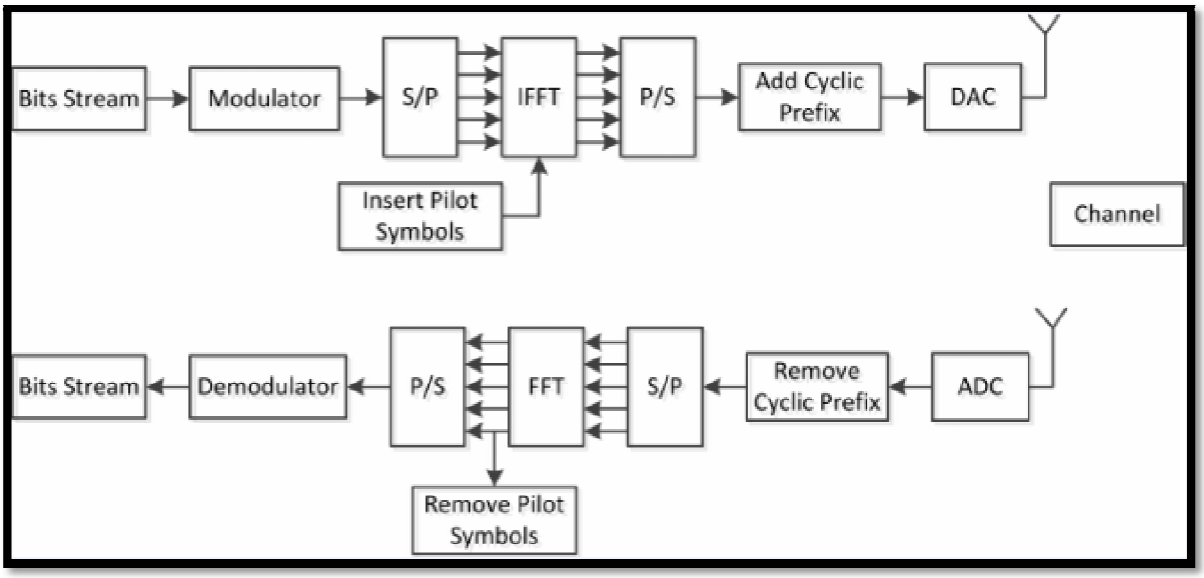

Fig: System Architecture

The block diagram of the proposed system is given above. The input to the system is the bit stream. The modulator is used to modulate the streams. The pilot streams are inserted in the stream. Fourier analysis converts a signal from its original domain (often time or space) to a representation in the frequency domain the DAC is the digital to analog

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 4, April 2017

converter it is used to convert the digital data into analog data then the streams are broadcasted after the broadcasting the next step is receiver side the ADC converts the bits into analog bits and the pilot streams are removed and the streams are demodulated.

VI. CONCLUSION

Orthogonal Frequency Division Multiplexing (OFDM) has been studied by researchers all over the world, which makes a great difference in modern modulate techniques. It has been presented that the complete design can fit for OFDM modulators of different wireless standards with different IFFT length, sub-carrier index, cyclic prefix and guard interval, whose resource consumption is quite low as well. In this paper, a reconfigurable OFDM transmitter architecture for 4G-LTE applications was presented. It has the capability of selecting on-the-fly from five different transmission modes: 1.4, 3, 5, 10, and 20 MHz; three modulations: 4/16/64 QAM, frame size, OFDM symbols/slot, and the assembly configuration parameters of each OFDM symbol, such as the number of null carriers, the CP size, the pilot inclusion, etc. The proposed architecture outperforms the existing fixed and variable lengthFFT processors in terms of speed, power, area, flexibility and scalability. In addition, the processor architecture can also be adopted in any other applications where a reasonable balance between specified design parameters is essential.

REFERRENCES

[1]Revanna, D. and Anjum, O. and Cucchi, M. and Airoldi, R. and Nurmi, J. A scalable FFT processor architecture for OFDM based communicationsystems. Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS XIII), 2013 International Conference on, 2013

[2]Bautista-Contreras, B. and Parra-Michel, R. and Carrasco-Alvarez, R. and Romero-Aguirre, E. A SDR architecture based on FPGA for multistandardtransmitter.Global Conference on Signal and Information Processing (GlobalSIP), 2013 IEEE, 2013.

[3]Zhang, B. and Guo, X. A Novel Reconfigurable Architecture for Generic OFDM Modulator Based on FPGA. In Advanced Communication Technology(ICACT), 2014 16th International Conference on, pages 851-854.IEEE, 2014.

[4] Garcia, J. And Cumplido, R. On The Design Of An Fpga-Based Ofdm Modulator For Ieee 802.11a. Electrical And Electronics Engineering, 2005 2nd International Conference On, 2005.

[5] Zhang, B. What's More, Guo, X. A Novel Reconfigurable Architecture For Generic Ofdm Modulator Based On Fpga. In Advanced Communication Technology (Icact), 2014 Sixteenth International Conference On, Pages 851-854. Ieee, 2014.

[6] Garcia, J. What's More, Cumplido, R. On The Outline Of A Fpga-Based Ofdm Modulator For Ieee 802.11a. Electrical And Electronics Engineering, 2005 Second International Conference On, 2005

[7] Mr. Rahul S. Bilwane ; Prof. Amit G. Fulsunge "Literature Review On Design Of Ofdm Model" International Journal Of Research Available At Http://Internationaljournalofresearch.Org/ P-Issn: 2348-6848 E-Issn: 2348-795x Volume 02 Issue 03 April 2015 Available Online: Http://Internationaljournalofresearch.Org/ P A G E | 348 - 351

[8] MeghanaShetty , Yuvraj , Praveen , RaghavengraRao "A Novel Architecture For A Dscdma-Ci Transmitter Using Cordic And Its Fpga Implementation" International Journal Of Innovative Research In Electrical, Electronics, Instrumentation And Control Engineering And National Conference On Advanced Innovation In Engineering And Technology Vol. 3, Special Issue 1, April 2015 Doi 10.17148/Ijireeice