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Reversible Parity Generator Design and Simulation using Nanoscale Quantum Dot Cellular Automata Technology

Vinti Sharma[1], Mr. Pradeep Singh Yadav[2]

MTech Scholar, Dept. of Electronics & Telecommunication, Shri Shankaracharya Technical Campus, Bhilai, India

Assistant Professor, Dept. of Electronics & Telecommunication, Shri Shankaracharya Technical Campus, Bhilai, India

ABSTRACT: This work proposes a reversible odd parity generator with minimal QCA cell and latency, minimizing the circuit size with greater efficiency in terms of energy. Building fast, energy-efficient, and as tiny as possible devices is the main goal of QCA nanotechnology. The designers are now faced with the difficulty of creating designs that satisfy the specifications. A unique reversible odd parity generator is designed and a Quantum Dot Cellular Automata nanotechnology-based logical representation of the reversible Feynman gate. Findings of The QCA designs and simulation outcomes were produced using QCA designer2.0.3. Lesser cells and less space are required by the suggested QCA architecture. In comparison to the best design currently available, the area of the suggested odd parity generator is 0.022μm^2, which is 37% better. The suggested odd parity generator has 22 cells and 0.75 clock cycle delay(latency). Comparing the proposed designs to the best ones now available, the occupied area is the lowest.

KEYWORDS: Quantum-Dot Cellular Automata (QCA); Reversible Logic; Nanotechnology; Parity generator; Reversible Feynman gate, Nanoelectronics, reversible odd parity generator

I. INTRODUCTION

I.1REVERSIBLE LOGIC:

Reversible logic is a form of computing that allows inputs to be uniquely determined from outputs and vice versa without losing any information. The logical operations can be reversed via reversible logic gates.
The following conditions must be followed in order to satisfy reversible logic requirements:

- Conservation of Information: Reversible logic assumes that no information should be lost during calculation, which is known as **conservation of information**. In other words, every input combination should map specifically to a single output combination, and vice versa.
- Reversibility: Reversible logic gates enable unique input/output identification, enabling computation to be reversed. This means original inputs can bee uniquely determined from outputs.
- No fan-out: Fan-out is not allowed for reversible logic gates, which means that each gate's output should only be connected to one input of the next gate.

Reversible logic gates and circuits can be created by meeting these requirements, and they have uses in many industries including cryptography, low-power computing, and quantum computing.

I.2 QCA FUNDAMENTALS

QCA is anticipated to offer a number of advantages in the creation and application of subsequent-generation high-performance systems. Comparatively speaking, the QCA relies on the fundamental fundamentals of tunneling between nearby dots and Coulombic contact between adjacent cells. These principles effectively sum up some of the limitations of CMOS technology. Figures 1(a), 1(b) display Depending on where the electrons are positioned in the cell, the value of the molecular QCA can be encoded as either a logic value of 0 or a logic value of 1. According to a number of experimental findings, a double-dot cell's electron has the capacity to switch, affecting the position of an individual electron in a distinct cell.

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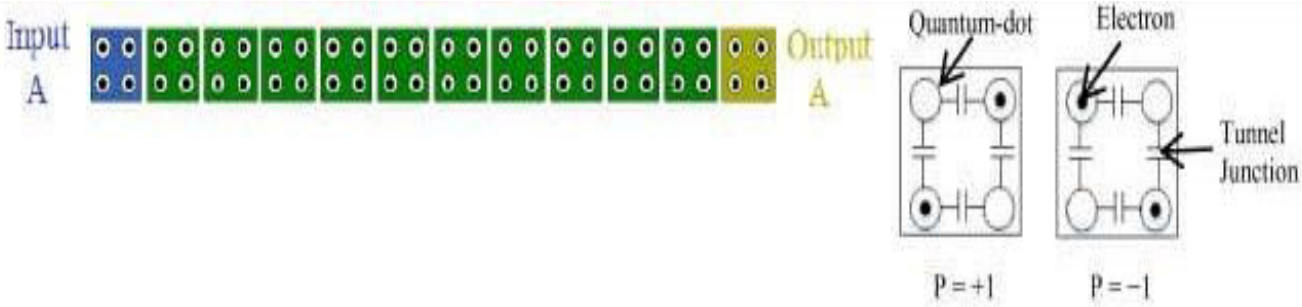

Figure 1 (i) QCA wire,1(ii)QCA cells

I.3 CLOCKING IN QCA:

To ensure accurate and synchronized operation of the circuit, proper clocking is essential in QCA. It aids in the regulation of state transition timing and sequencing, enabling accurate computing in QCA systems.

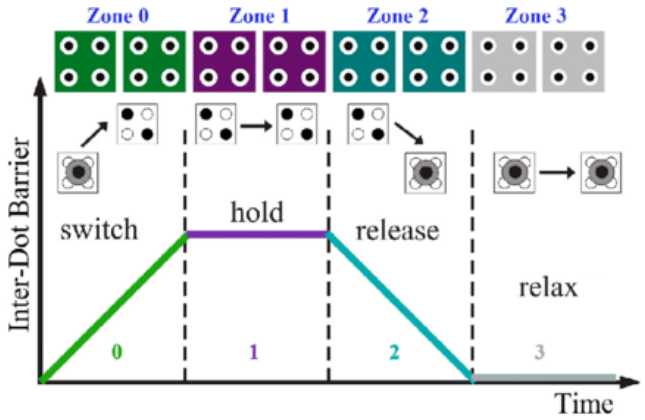

Fig2: QCA clocking scheme depicting different clock zones [2].

1.4 QUANTUM COST:

By multiplying the circuit's overall area by its latency, the quantum cost of the circuit is determined. These findings demonstrate the area and delay efficiency of a circuit. A circuit's QCA circuit cost is also determined by adding its quantum cost and clock cycle delay. The QCA circuit must have the lowest possible cost. Another crucial element for QCA reversible logic gate-based circuits is the calculation of the garbage output. The suggested circuit can produce up to two garbage outputs at a time. Thus, it is evident that the circuits were created to have the fewest possible garbage outputs.

II. PROPOSED ODD PARITY GENERATOR

A parity generator is a term for the combinational logic circuit in the transmitter that produces a parity bit. Its function is spot errors and alert the recipient to ask for retransmission of data or take the necessary action

In the current study, we put forward a new reversible odd parity generator in QCA technology that is implemented using two Feynman gates. Our technique turns multiple-output functions from irreversible to reversible. As a result, a reversible function has the following qualities:

i. Inputs and outputs must have a distinct mapping.
ii. Feedbacks are not acceptable.
iii. No Fan-out.

B1, B0, and d are the three input bits in this truth table, while o is the output(parity) bit. The output bit is calculated so that it is set to 1 if there are more odd input bits than even ones, and to 0 if there are more even bits than odd ones.

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Table1: Truth Table of Odd Parity Generator

B1	B0	d	output o
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Two 2-input majority gates make up the main logical figure for the QCA, as depicted in Figure 3[7], which is used to execute the reversible odd parity generator. This Feynman gate was modeled in the coplanar layer and constructed using QCA technology with 10 cells and 0.25 latency.

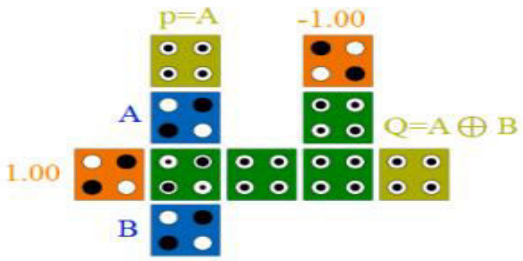

Fig3: Reversible Feynman gate in [7]

The newly introduced odd parity generator's diagram and the mapping of its inputs (B1, B0, and d) to its outputs (p=B1, q=B0, and o) are displayed in Figure 4 below.

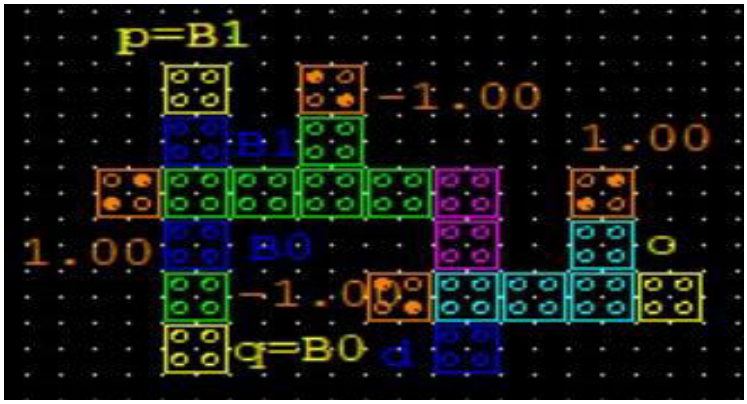

Fig4: 3-bit odd parity generator design with proposed reversibility.

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The newly suggested three-bit reversible odd parity generator's QCA design is shown in Figure 4. It executes across 3 clock zones, establishes garbage outputs p=B1 and q=B0 over the first clock zone, and generates the o output after three clock cycles (0.75 clock cycle delay).

III. SIMULATION RESULTS

V.I SIMULATION TOOLS:

This section uses the QCADesigner version 2.0.3 to simulate the suggested design. The designers' ease of use in simulating their designs with QCADesigner is a crucial component. There are four possible states for cells in the QCADesigner. Figure 8 presents the different modes.

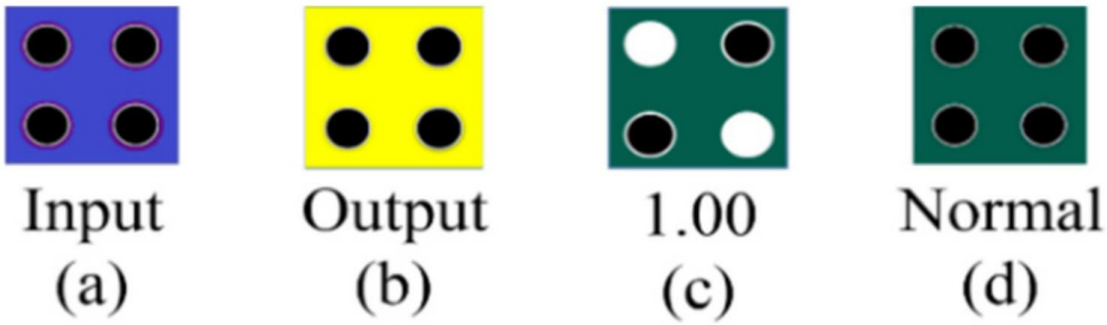

Fig5: Different cells available in QCA Designer (a)input cell, (b)output cell (c)fixed cell (d)normal cell[6]

V.2 SIMULATION PARAMETERS:

All of the simulation's parameters and calculations are currently set to their default setting. Quantum dots with a 5 nm diameter are used to regulate each cell's of 18×18 nm^2 size. Relative permittivity=12.9, convergence tolerance=0.001, 9.810-022 J clock high, layer spacing=11.5nm, and 100 iterations in each sample have been chosen as the parameters for the bistable approximation factors. For the "Bistable Approximation" engines, the defined parameters in Figure 6 were utilized. We employed "Bistable Approximation" which was the simulation engine's default setting in this study, to simulate the suggested circuit.

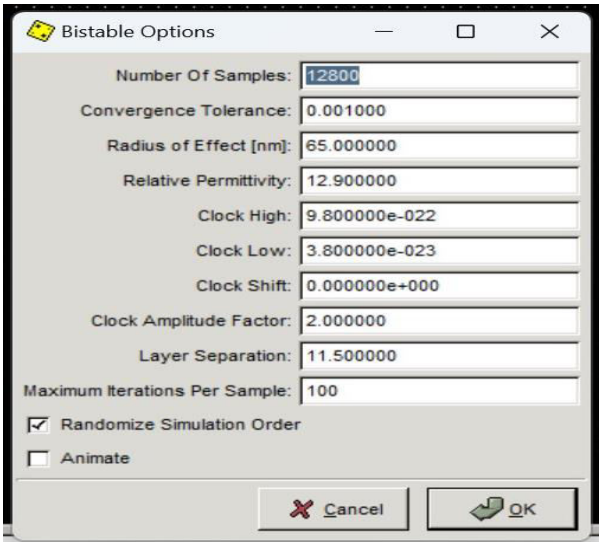

Fig 6: Default simulation parameters used in the proposed design

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V.3 SIMULATION ANALYSIS:

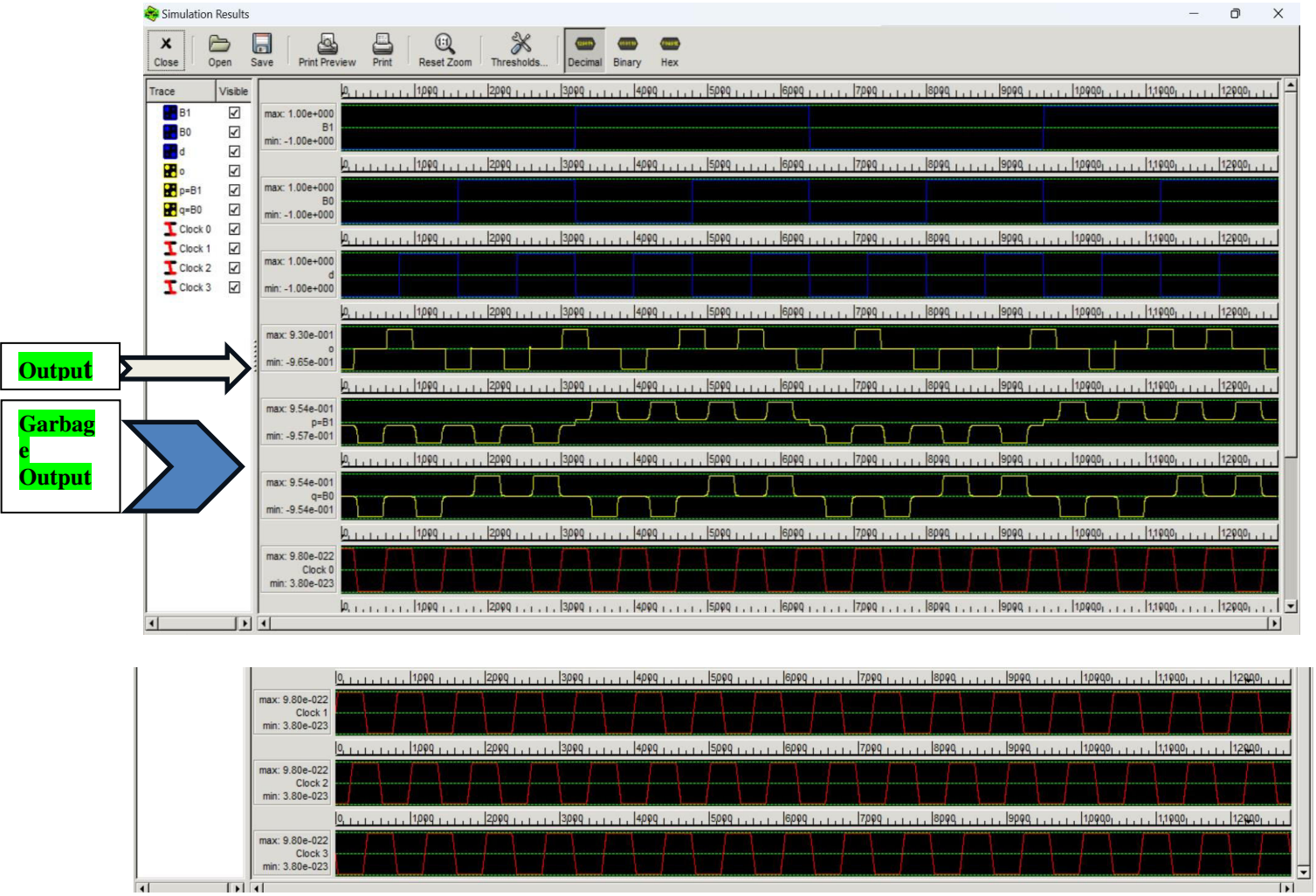

Fig7: Simulation results of proposed reversible odd parity generator

Figure 7 shows that after a 0.75 clock cycle delay, the output is accurately achieved. It is evident that the output exactly corresponds to the truth table of the reversible odd parity generator displayed in Table 2.

V. COMPARISONS

With regard to cell count and area, the suggested design clearly outperforms the earlier ones. The suggested layout consists of 22 QCA cells. For the suggested design, the minimum clock phase, or delay, is 0.75. The lesser area occupied by the circuit's design. The truth table supported the simulation findings for the innovative reversible parity generator circuit implemented with QCA, validating the operational effectiveness of the suggested novel design.

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TABLE 2: Comparative assessment of a 3-bit reversible odd parity generator

QCA REVERSIBLE ODD PARITY GENERATOR	CELL COUNT	AREA(in μm^2)	LATENCY
JC Das et al. [4]	43	0.038	0.75
Ali H Majeed [8]	24	0.035	0.75
Proposed design	22	0.022	0.75

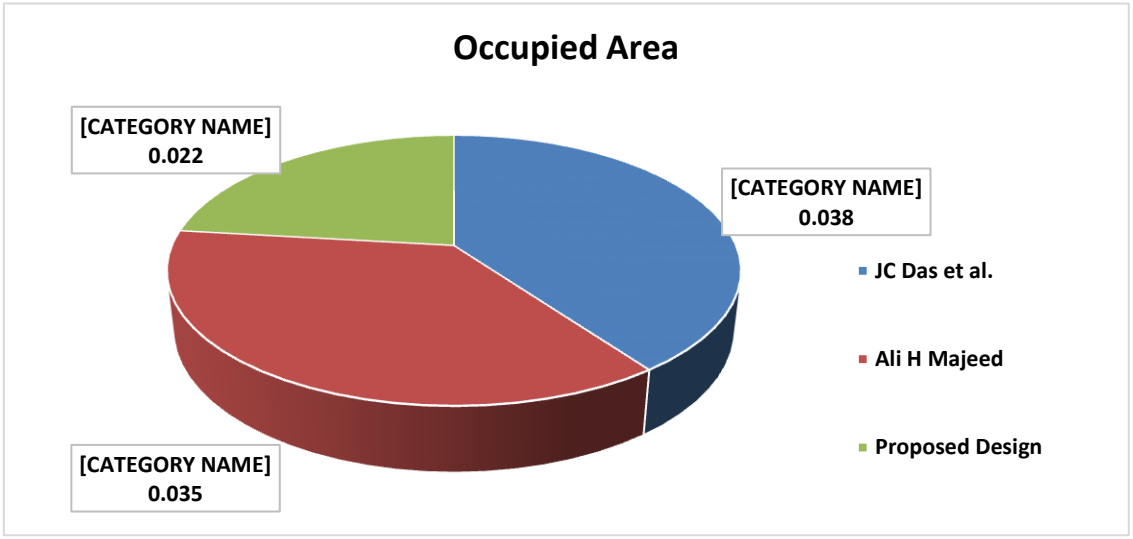

Fig8: Pie Chart depicting the area occupied by best-reported designs

Fig8 pie chart shows that our proposed reversible odd parity generator occupies the least area when compared to the best available designs. Less occupied area depicts reduced cost in embedding the circuit and higher efficiency and is 37% less than Ali H Majeed's design [8]

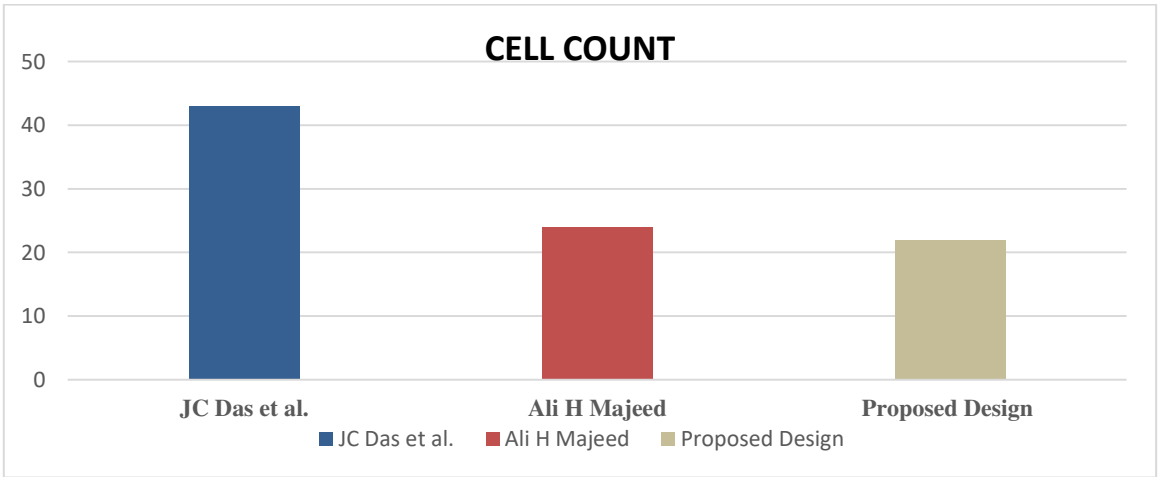

Fig9: Bar graph depicting the cell count of proposed and best-reported designs.

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According to the above bar chart, the suggested design has an 8% lower cell count than Ali H Majeed's design [8]

IV. CONCLUSION AND FUTURE WORK

The primary goals of nanotechnology are to minimize heat dissipation and circuit size so that they can be more readily integrated into an instrument. Reversible logic in conjunction with QCA technology may be the answer to ending these issues. In comparison to earlier works, the suggested 3-bit reversible parity generator used QCA and was optimized with decreased area and cell consumption. It could be useful in developing more advanced and complex reversible QCA designs in the future. When developing reversible circuits, it may also be utilised as a useful fundamental component for bigger units, such as communication systems, storage devices, and data transmission protocols. So, our work suggested low-cost solutions for reversible QCA-based nanoscale computing.

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