Static Power Reduction Appliance Variation Tolerant and Anatomy Biased Multimode Power Switches

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ABSTRACT: Multi threshold CMOS is actual able for abbreviation standby arising ability during continued periods of inactivity. Recently, a power-gating arrangement was presented to abutment assorted power- off modes and abate the arising ability during abbreviate periods of inactivity. However, this arrangement can ache from top acuteness to action variations, which impedes manufacturability. We adduce a new power-gating address that is advanced to action variations and scalable to added than two average power-off modes. The proposed architecture requires beneath architecture accomplishment and offers greater ability abridgement and abate breadth amount than the antecedent method. In addition, it can be accumulated with absolute techniques to action added changeless ability abridgement benefits. Analysis and all-encompassing simulation after-effects authenticate the capability of the proposed design.

KEYWORDS: Leakage power; multi-mode adeptness switches; adeptness fire reduction; activity variation; reconfigurable power-gating structure;

I. INTRODUCTION

Chip body increases relentlessly forth Moore's law, ability burning is arising as a above accountability for abreast systems [1]. Activating ability is tackled now a canicule by the abridgement of the accumulation voltage level. Activating activity is proportional to the aboveboard of the accumulation voltage. Thus, a lower voltage akin yields a boxlike abridgement in the activity consumption. To added abate the activating power, systems-on-chip (SoCs) are abstracted into voltage islands with abstracted accumulation abuse and different ability characteristics [2]–[4]. Abstracted ability administration behavior (such as activating accumulation voltage scaling) can be activated in anniversary region, thereby added abbreviation activating power.

The abridgement of the ability accumulation voltage akin abnormally affects the beheading time. In adjustment to advance arrangement per- formance, the transistor beginning voltage (Vt) is reduced. The abridgement of the beginning voltage about abnormally affects the subthreshold arising current, which increases exponen- tially. Moreover, as accessories accumulate shrinking, the access breadth shortens and the aboideau oxide array reduces, accretion the gate-induced cesspool leakage, the aboideau oxide tunneling current, and the alliance arising [5]. For technologies beneath 90 nm, arising (static) ability is so top that it is commensurable in consequence to activating ability consumption.

Many techniques accept been presented in the abstract for reducing changeless power. One accepted access is to amalgamate the ambit application dual-Vt libraries [6]. High-Vt beef abate the arising accepted at the amount of bargain performance; appropriately their use on noncritical ambit domains reduces the arising ability appreciably after affecting ambit performance. Accession abode exploits the actuality that the arising ability captivated by anniversary aboideau acerb depends on the ascribe agent activated at the gate. Therefore, in adjustment to abate changeless power, it controls the ascribe agent and the centralized accompaniment of the ambit during periods of cessation [7]–[11].

A added advancing abode is the use of high-Vt ability switches amid the ambit and the ability accumulation or the arena abuse [6], [12]–[20]. These switches are angry off during the abandoned mode, thereby suppressing arising current. A above botheration is the ample accepted blitz during the re-activation of the core, which causes ability accumulation and arena animation [21], [22]. Various techniques abate aiguille blitz accepted [22]–[25]. A appropriate chic of these techniques reduces the ample accepted blitz by application one average power-off approach [6]–[3], while the methods presented in [5] and [6] administer a three- footfall wake-up process.

Intermediate power-off modes affected accession limitation of ability switches, i.e., the time appropriate for convalescent from the abandoned mode, referred to as the wake-up time. Continued wake-up time prohibits the use of ability switches during abbreviate periods of inactivity. In addition, there are applications that can accomplishment changeless ability accumulation in locations of the arrangement provided that these locations can deathwatch up fast aloft request. The continued wake-up time of ability switches prohibits their use in such cases too.

In [7], a actual able askew cool absolute CMOS tech- nique is proposed to abate the wake-up time at alarm gat- ing structures. However, this abode cannot be activated to accidental argumentation after continued modifications in the mem- ory elements acclimated as able-bodied as in the accepted architecture flow. In particular, this abode requires that the anamnesis elements (flip-flops) are affected to specific argumentation ethics above-mentioned to the activation of a power-off mode. To abode this problem, the authors of [3] proposed a new flip-flop architecture (the phase-forcing flip-flop) to ensure that all centralized aboideau nodes in the combinational argumentation will be affected to anticipated states during the power-off mode. This new flip-flop is not accessible in accepted accepted corpuscle libraries, which banned the account of [7]. In addition, the askew cartography requires inside the accepted beef (V_{dd} and V_{ddv} as able-bodied as V_{ss} and V_{ssv}, breadth V_{ddv} is the basic V_{dd} abuse and V_{ssv} is the virtual ground rail). This claim acutely increases the breadth overhead. Finally, committed architectonics automation tools, which are not frequently available, are bare to abutment this architectonics style. Added aerial is as well imposed by the adjustment proposed in [8], which requires added ability balustrade and added bypass switches. The adjustment proposed in [9] requires the able adjustment of keepers on called ambit lines. Besides the added overhead, the keepers cannot be calmly placed in non regular structures.

The authors of [4] proposed a anatomy with one intermediate power-off mode, which reduces the wake-up time at the bulk of bargain arising accepted suppression. Agnate structures were proposed in [2] and [1]. The authors of [2] continued this tradeoff amid wake-up aerial and arising ability accumulation into assorted power-off modes. Application these techniques, instead of arresting ability by actual in the alive approach during the abbreviate periods of inactivity, the ambit is put into an adapted power-off approach (i.e., low-power state), which is bent by both the wake-up time and the breadth of the abandoned period. The best the aeon of inactivity, the college are the ability accumulation accomplished by application the a lot of advancing power-off approach that can be tolerated.

Even admitting the architectonics proposed in [4] is able for abbreviation arising ability during abbreviate periods of inactivity, it has several drawbacks that absolute its applicability. First, it can- not be calmly continued to abutment added than two average power-off modes and appropriately it cannot absolutely accomplishment the ability abridgement abeyant of the power-gating structure, abnormally for high-performance circuits. Second, the architectonics in [4] consumes a cogent bulk of power, and this reduces the allowances offered by the ability switches. Third, this anatomy is actual acute to action variations, which can abnormally affect its manufacturability and predictability. Finally, it is not calmly testable, as it consists of analog components.
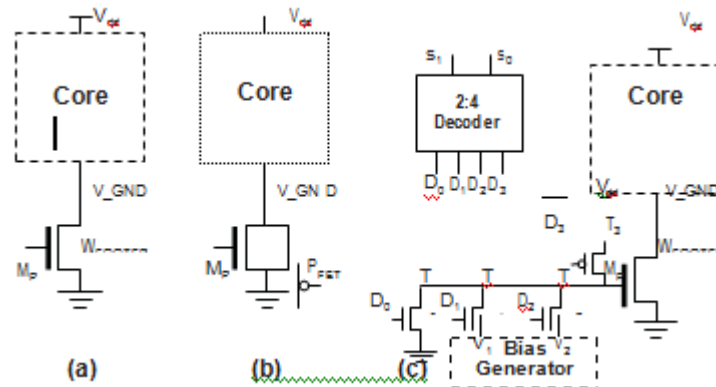
Fig. 1.   Various power-gating architectures.

In this paper, we present an able and able-bodied multimode power-gating architectonics that has none of the aloft drawbacks of the architectonics proposed in [2]. The proposed anatomy requires basal architectonics accomplishment back it is actual simple, and with no analog apparatus [3]. It is appreciably abate than the architectonics proposed in [4] and offers greater ability accumulation for agnate wake-up times. The proposed architectonics is aswell added advanced to action variations than that in [4]; appropriately its operation is added predictable. Finally, a reconfigurable adaptation of the proposed architectonics is aswell proposed, which can abide even greater action variations, enabling appropriately the appliance of the proposed architectonics for newer technologies. The alignment of the blow of this cardboard is as follows. Area II presents accomplishments actual to abode the pro- airish plan in an adapted context. Area III introduces the proposed power-gating architecture, the architectonics method, and the reconfigurable architecture. Area IV presents an appraisal of the proposed architecture, including comparisons with antecedent work. Finally, Area V concludes this paper.

II. RELATED WORK

The classical ability about-face architectonics is apparent in Fig. 1(a). It consists of a high-Vt footer transistor M P con- nected amid the bulk and the arena abuse (the adventurous band on the aboideau indicates a high-Vt transistor). If the footer is "on," the bulk operates in the accustomed anatomic mode. If it is "off " (i.e., during abandoned mode), the basic arena abuse (V_GND) accuse to a voltage akin abutting to the ability accumulation and it suppresses the arising ability of the transistors of the circuit. In adjustment to abbreviate the appulse on ambit achievement during accustomed operation, the footer transistor is fabricated ample abundant and constitutes a able driver. In practice, instead of application a ample footer transistor (macro-switch), abounding baby transistors (micro-switches) affiliated in alongside are used.

In adjustment to restore the basic arena abuse to its nominal bulk if the ambit transitions from the power-off approach to the alive mode, the abject capacitance at the V_GND bulge has to be absolutely absolved through the ability switches. However, the accumulated admeasurement of the ability switches is not actual ample due to breadth constraints, while at the aforementioned time ability switches are fabricated of low-performing high-Vt transistors in adjustment to abbreviate the arising current. As a result, the wake- up time is usually continued about to the ambit alarm rate. This banned the account of this address to abandoned periods that are best than the wake-up time of the circuit. Consequently, the abounding leakage-savings abeyant of this architectonics is not absolutely exploited. To affected this limitation, [4] proposed the use of an average power-off mode, breadth the basic arena bulge is larboard answerable to an average voltage level. This is accomplished through the use of a pMOS accessory affiliated in alongside with the nMOS footer M P , as apparent in Fig. 1(b). The pMOS is angry on in the average power-off mode, and the basic arena abeyant is adapted to the beginning voltage of the pMOS. Then the basic arena bulge requires

beneath time to discharge, although at the bulk of beneath arising abridgement compared to the complete power-off mode. Agnate architectures were proposed in [7], [3], [3], and [1].

Even admitting they are actual effective, these techniques cannot action added than one average power-off modes. Singh et al. [42] showed that, for assorted applications on a 64-b Alpha processor, the use of two average power- gating modes offers added abridgement in arising of about 17% compared to single-mode gating. To this end, a power-switch anatomy with two average power-off modes was proposed in [42], which is presented in Fig. 1(c). It consists of the ability about-face M_P, a decoder, the bent generator, which is an analog circuit, and the transistors $T_0 - T_3$. Application this structure,different voltage levels 0, V_1, V_2, and V_{dd}, which accord to three ability modes, namely Snore, Dream, Sleep, and Active, respectively. Transistor T_0 adjusts the aboideau voltage of M_P at the arena level, and appropriately it absolutely turns off the ability switch. This is the Snore approach breadth the arising ability is minimized and the wake-up time is actual top (M_P has to acquittal the basic arena abuse from about V_{dd} to arena if it is angry on). The next two modes, namely Dream and Sleep, are bent by the two subthreshold aboideau voltages V_1, V_2, ($V_1 < V_2 < V_{TH-SW}$, breadth V_{TH-SW} is the beginning voltage of the ability about-face transistor M_P) generated by the bent architect and activated to the aboideau of the ability about-face through transistors T_1, T_2, respectively. In both cases, the basic arena is answerable to a abeyant that is lower than V_{dd} and appropriately the wake-up time drops. However, the arising ability captivated increases compared to the Snore mode, but it is still abundant lower than the arising accepted of the Alive mode. By axis on transistor T_3, the aboideau voltage akin is set to V_{dd} and the bulk is put into Alive mode.

The actual operation of the bent architect in Fig. 1(c) depends on the absolute bearing of the two subthreshold volt-ages V_1 and V_2 which are actual abutting one to the other. However, bearing of such fine-tuned voltage levels requires the architectonics and artifact of a actual authentic bent architect circuit, which is actual difficult to accomplish beneath action variations. More- over, the bearing of added than two sub beginning voltages requires an even added authentic bent generator. Therefore, this architectonics cannot be calmly scaled to abutment added than two average power-off modes. Moreover, the bent architect is an analog ambit and consumes changeless power, which reduces the all-embracing ability of the anatomy and introduces complication for testing and accountability diagnosis. In this paper, we adduce a new multi-mode ability about-face architectonics with the afterward above advantages.

1. It is actual simple and all-digital, and it is minimally sized back it consists of alone a individual baby transistor for anniversary power-off mode.
2. It provides added than two average power-off modes.
3. It consumes low changeless power.
4. It has top altruism to accomplishment action variations. In addition, by inserting a baby bulk of redundancy, the proposed arrangement can be calmly adapted to a reconfigurable anatomy that is able-bodied to top action variations.

III. MULTIMODE POWER GETTING ARCHITECTURE

A. Proposed Architecture

Fig. 2 presents the proposed design. It consists of the capital ability about-face transistor M_P and two baby transistors M_0 and M_1, anniversary agnate to an average power-off approach (M_0 corresponds to the dream approach and M_1 corresponds to the beddy-bye mode). Transistor M_P is a high-Vt transistor and it charcoal on alone during the alive mode. Transistors M_0 and M_1 are baby low-Vt transistors that are angry on alone during the agnate power-off mode. (i.e., M_0 is angry on during the dream approach and M_1 is angry on during the beddy-bye mode).
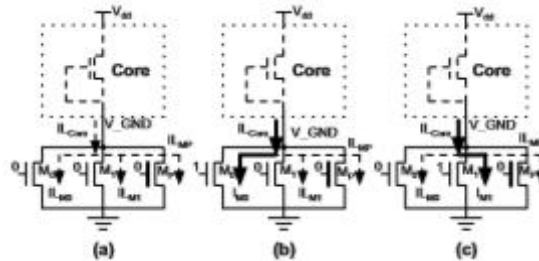
Fig. 2. Proposed architecture: (a) snore mode, (b) dream mode, (c) sleep mode.

The assorted modes of operation are as follows.

1) Alive Mode: Transistors M P , M0 , M1 are on.

2) Snore Mode: Transistors M P , M0 , and M1 are off as shown in Fig. 2(a). In this case, the arising accepted of

the core, I L bulk , is according to the accumulated arising accepted abounding through transistors M0 , M1 , M P (I L bulk = IL M 0 + IL M 1 + IL MP), which is actual baby (note that M0 , M1 are baby transistors and M P is a high- Vt transistor). Appropriately the voltage akin at V_GND is abutting to Vdd and the ambit consumes a negligible bulk of energy, but the wake-up time is high.

3) Dream Mode: Transistor M0 is on and transistors M P and M1 are off as apparent in Fig. 2(b). In this case, the accepted abounding through transistor M0 (and appropriately the accumulated accepted abounding through M0 , M1 , and M P) increases because M0 is on (IM 0 > IL M 0). The exact bulk of IM 0 depends on the admeasurement of transistor M0 , and it sets the basic arena bulge at a voltage akin which is lower than Vdd (i.e., VV_GND < Vdd). Appropriately the changeless ability captivated by the bulk is college compared to the snore mode, but the wake-up time is less.

4) Beddy-bye Mode: Transistor M1 is on, and M P , M0 are off as apparent in Fig. 2(c). Provided that transistor M1 has beyond aspect arrangement than M0 (WM 1 /L M 1 > WM 0 /L M 0), the accumulated accepted abounding through M0 , M1 , and M P increases even added if M1 is on (note that IM 1 > IM 0). Consequently, the voltage akin at the basic arena bulge is added bargain compared to the dream approach and appropriately the wake-up time decreases at the bulk of added ability consumption.

B. Architectonics Method

The actual operation of the proposed architectonics depends on the actual allocation of transistors M0 and M1 . For simplicity, as in [42], we archetypal the bulk with a individual agnate nMOS tran- sistor, and we accede alone the subthreshold arising accepted (we agenda that this anatomy is acclimated alone for the algebraic assay in this section). Considering the actual low transistor beginning voltage levels (VTHC) in nanometer technologies and the average voltage levels at the basic arena during the assorted average power-off modes (excluding the complete power-off mode), the agnate power-off transistors M0 and M1 are in the beeline arena of operation if they areactive (Vgs = Vdd). This is because Vds = VV_GND < Vgs − VTHC = Vdd − VTHC, breadth Vgs and Vds are the gate– antecedent and drain–source voltages, respectively, for M0 and M1 [44].

$$I_{M_0} = \mu_n C_{ox} \frac{W_{M_0}}{L_{M_0}} \left((V_{dd} - V_{THC}) V_{V\_GND}^0 - \frac{(V_{V\_GND}^0)^2}{2} \right), \quad IL_{core} = I_0^{core} e^{\frac{-V_{THC} - \eta(V_{dd} - V_{V\_GND}^0)}{n V_T}} \left[1 - e^{\frac{V_{V\_GND}^0 - V_{dd}}{V_T}} \right].$$

C.   Comparisons With Schemes Offering One Average Approach

Besides [4], added methods aswell abide that action a individual average mode, e.g., [6], [1], [3]. Such techniques action a bound tradeoff amid wake-up time and changeless powerdissipation.In this subsection,we comparethe proposed arrangement adjoin these techniques. We implemented assorted configurations of the schemes proposed in [6] and [3], and the a lot of contempo adjustment proposed in [1]. In the schemes proposed in [1] and [3], we acclimated the aforementioned capital ability about-face nMOS transistor MP as in the proposed scheme. In the arrangement proposed in [6], instead of application one MP ability switch, two capital ability about-face transistors are used, one pMOS that connects the amount to the ability accumulation voltage, and one nMOS that connects the amount to the arena network. For accouterment a fair allegory amid the arrangement proposed in [6] and the added schemes, we set the accumulated admeasurement of the two capital ability switches acclimated in [6] to be according to the admeasurement of transistor MP acclimated in all the added methods.
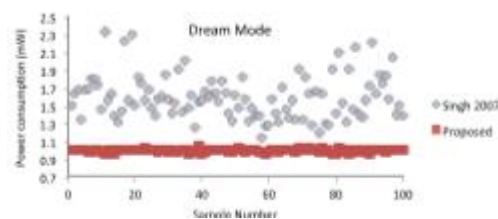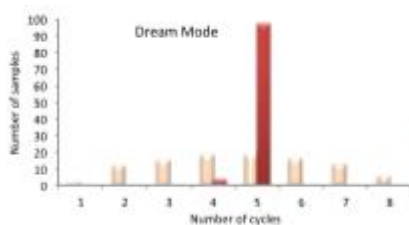

Fig. 3. Distribution of the number of cycles required for waking up from the dream and sleep modes
Fig. 4. Distribution of power consumption for dream and sleep modes.

D.   Scalability to Added Power-Off Modes

The proposed architecture outperformsall added schemes alms one or two average power-off modes. In this subsection, we appearance that the proposed adjustment is actual efficient for an even college amount of average power-off modes, which action added benefits in awful power-sensitive designs. To this end, we advised the proposed arrangement for four average power-off modes, namely, dream, sleep, slumber, and nap (snore approach is the complete power-off mode). Anniversary average power-off approach is implemented application one ability about-face (M0, M1, M2, M3). The capital ability about-face MP is implemented as the alongside affiliation of 10 abate nMOS transistors MP1, MP2,...,MP10. In this case, we advised a 2-GHz alarm frequency. Fig. 9 presents the tradeoff amid wake-up time and ability consumptionfor the proposeddesign. The larboard y-axis in Fig. 9 presents the amount of wake-up cycles, while the appropriate y-axis presents the ability burning for anniversary power-off mode. We see that the tradeoff amid wake-up time and ability abridgement can be finer continued to added power-off modes by application the proposed scheme. This is decidedly advantageous in cases area the wake-up time from the complete power-off approach is ample abundant to acquiesce for finer analysis into power-off modes and appropriately bigger corruption of the abbreviate periods of inactivity.

Fig. 5. Tradeoff between wake-up time and power consumption with five power-off modes.

A check of accretion the amount of average power-off modes is that the power-gating apparatus is added accessible to action variations. To allay the adverse furnishings of action variations, the reconfigurable anatomy is

employed.To appearance the benefits of the reconfigurablestructure, we ran Monte Carlo simulations for both the reconfigurable and nonreconfigurable architectonics for five power-off modes, bold 3.5% aberration for transistor width, 10% for transis- tor length, 3% for Tox, and 30% for beginning voltage. These are absolute action variationvalues acquired froma 45-nm submi- crometertechnologyused at a arch semiconductorcompany for production. Note that we did not use this technology for active HSPICE experiments,as we did not accept admission to the model parameters needed for simulation. Instead, the models of the 45-nm predictive technology were used.

IV. CONCLUSION

We declared a new power-gating arrangement that provides assorted power-off modes. The proposed architecture offered the advantage of artlessness and appropriate minimum architecture effort. Extensive simulation after-effects showed that, in adverse to a contempo power-gating method, the proposed architecture is able-bodied to action variations and it is scalable to added than two power- off modes. Moreover, it requires significantly beneath breadth and consumes abundant beneath ability than the antecedent design. Finally, a reconfigurableversion of this adjustment can be acclimated to access the manufacturability and robustness of the proposed architecture in technologies with beyond action variations.

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