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Design of Multiple Full Adders Using XOR and XNOR Gates for Power Minimization and High Speed

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ABSTRACT: In recent trends, Power Optimization and Speed Improvement played a key role in the VLSI design circuits. This project presents an advanced hybrid full adder. Rather than using conventional gates, we use XOR and XNOR gates which are built using high threshold voltage (HVT) MOS transistors. Adders have a powerful impact on the overall performance of the system. The modern design is correlated with some actual designs for average power, delay. The power utilization increased at a slow rate in contrast to other adders with the increase in frequency. The simulations are drifting out on Cadence Virtuoso at 100nm. By correlating with the previous FA designs, the present operation was found to offer a powerful improvement in terms of speed and power.

KEYWORDS: HVT, Average Power, Delay, Cadence Virtuoso, VLSI.

I. INTRODUCTION

As the technology advances day by day the demand of low power and high-speed operating devices is increasing. Power consumption can be reduced by two factors. By surmount the supply voltage and changing the operating frequency. But these factors may increase the propagation delay of the system and driving capability may be reduced. Full adders are the fundamental block of any digital circuit. Therefore, by increasing the efficiency of full adders increases the performance of overall system. VLSI devices contains a greater number of gates within a single package. Large memory arrays and complex microcomputer chips come under VLSI. CMOS technologies combine both PMOS and NMOS transistor (Rabaey, Chandrakasan, & Nikolic, 2002) [7] devices on the same silicon. Both the transistors require two different substrates, that is NMOS transistor requires a p- substrate and the PMOS transistor requires an n-type substrate. Each electronic circuit requires a certain amount of power to operate. The average power is a parameter that is measured in Milliwatts (mW). It represents the average power of the overall circuit. The sum of the entire average power in all gates, circuits or IC's in the design is considered as the overall average power consumed by the system. Propagation delay is the most important factor to measure the performance of the circuit. Time taken to propagate a signal from the input to the output of the gate is called the propagation setback of the gate.

II. LITERATURE SURVEY

Many of the previous researchers are concentrated on power utilization, speed improvement and efficiency of the system. In general, there are three constituting modules for full adder design (Zimmermann &Fichtner, 1997). And given the performance analysis of low power 1-bit CMOS full adder cells. By combining the different modules, there are twenty different full adder design is implemented. Every design has several benefits itself like power consumptions, speed, area and delay, device count. (Vesterbacka, 1999; Radhakrishnan, 2001) had explained the low- voltage low power CMOS full adder. In general, the design circuits use k-maps and pass network theorems are explained and six-transistor XOR- XNOR cell is implemented with the aid of standard rules. The standard method has not affected the voltage drop in transistors (Radhakrishnan, 2001). That does not affect from the threshold voltage drop in MOS transistors, but at the same time fewer transistors are used compared to existing designs. However, more design effort is required for the sizing of the

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transistors explained the design of robust, energy-efficient 1-bit full adders (Shams, Darwish, &Bayoumi, 2002) for deep sub micrometer design using hybrid-CMOS logic style. Novel 1-bit full adder which uses the hybrid logic is presented here for low Power consumptions. Proposed design is carried out with low power voltage levels. (Sudsakorn, Tooprakai, &Dejhan, 2012; Goel, Elgamel, &Bayoumi, 2003) asserted that a low- power high- speed CMOS full adder for embedded system. Generally, the power utilization is considered as an important factor but high speed is also one of the main factors for the appropriate design (Goel, Kumar, &Bayoumi, 2006; Chang, GU, & Zhang, 2005). Improving the driving capability, with just low power by using a new XOR gates (Tung, Hung, Shieh, & Huang, 2007; Aranda, Báez, & Diaz, 2010; Wairya, Singh, Nagaria, & Tiwari, 2011), the full adder is integrated in a System on Chip (SoC). Many design circuits faced power dissipation issue due to leakage currents of the whole static and dynamic cases (Deb & Majumder, 2016; Pattnaik et al., 2017) and its analysis. The minimization of the leakage power consumptions under certain circuit timing constraints is presented (Shin & Kim, 2004). The special functions gates have to satisfy the universal and basic gates principles, to reduce the component count.

III.PROPOSED WORK

A. *FULL ADDER*

An Adder is designed by using conventional methods by using only transistors. The Chang adder design is performed with 26 transistors and its modified low power XOR and XNOR circuit in Figure 2. By the addition of a greater number of transistors, the delay problem is solved, but these designs lead to the higher power utilizations. So, in order to decrease the power, we use HVT Transistors. Aguirre adder performed with parallel pass transistor logic style to find the balanced paths based on multiplexing of the Boolean functions. Full swing balance output is generated by the Goel adder with XOR- XNOR circuit. These circuit are used for the high-speed applications because of its cross coupling. Complementary pass transistor logic is evaluated by the Agarwal adders to determine the full fluctuation output voltage. This adder has a generated SUM and CARRY-OUT signals. Truth table has mentioned in Table 1.

The 1-bit Full Adder Transistor sizes are for p-MOS we use l=100nm and w=400nm, for n-MOS we use l=100nm and w=200nm respectively. This logic design style involves the division of larger circuit into smaller sub-circuits and each sub circuit is optimized using various logic design style. The design methodology for a full adder circuit is shown in Figure 2. The Figure 1 that the full adder circuit is split into 3 sections and these sections are designed using different design styles to exploit the advantages of the different design styles and essence the desired performance. Module 1 produceXNOR and XOR behavior of the inputs A and B. The Module1 can be either XNOR based or XOR based depending on the primary output generated within the module the primary output is utilized as input to another module to get the other output using an inverter. Module 2 and Module 3 comprises of the circuitry to produce the required sum and carry outputs of the full adder by appropriate the intermediate outputs achieved by module1 circuit

A	B	C_{in}	SUM (S)	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1: Truth Table of Full Adder

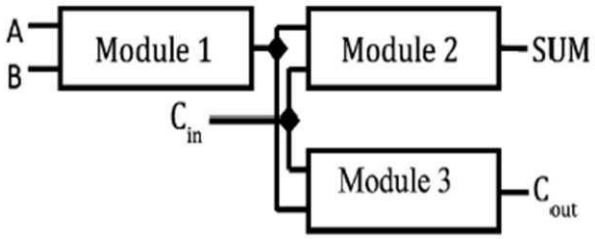

Figure 1. Schematic Diagram of Hybrid Full Adder

B. *MODIFIED XNOR MODULE*

XNOR module consumes more power in the proposed adder design. Power can be reduced to best desirable extent by optimizing the XNOR module by using HVT Transistors and designing the circuit. It also wards off the possibility of voltage degradation. Figure 2 represents Modified XNOR circuit.

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C. *CARRY PROPAGATION MODULE*

The schematic of this module is given in Figure 3. The transistors Mp7, Mn7, Mp8 and Mn8 are accomplished in order to get the required carry out signal. Here the input carry signal (Cin) propagates through only one transmission gate, i.e., Mn7and Mp7. Hence it reduces path required for carry propagation. Large channel width transistors are used for transmission gates. Here Mn7, Mp7, Mn8 and Mp8 form the transmission gates. Hence it results in reducing the power consumption and delay for some extent. The Figure 6 and Figure 7 represents the simulation results of the 1bit full adder and 4-bit ripple carry adder. Here x-axis time and y-axis voltage level of the input and output signals. Here the voltage levels are varying from 0V to 1 V.

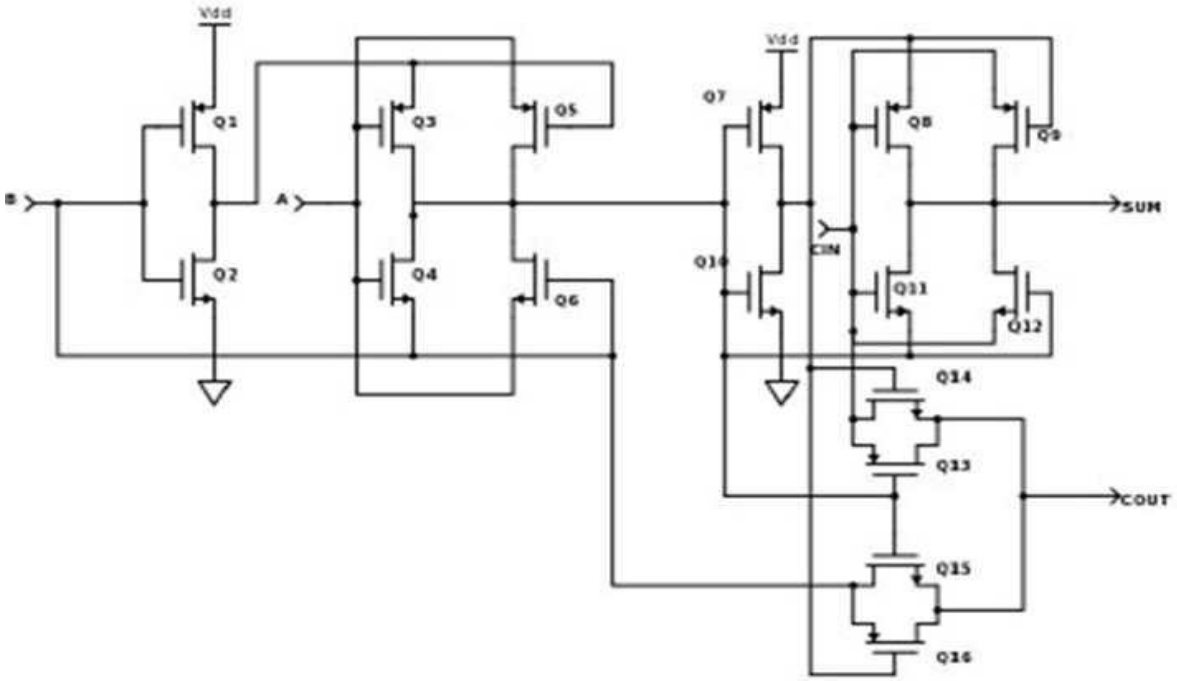

Figure 2. Proposed Full Adder Circuit

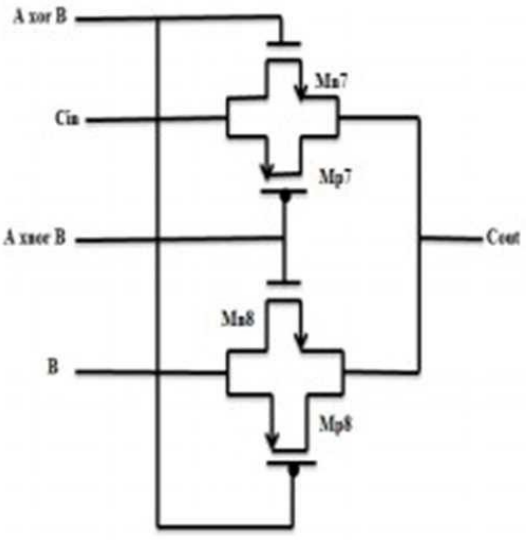

Figure 3. Carry Generation Module

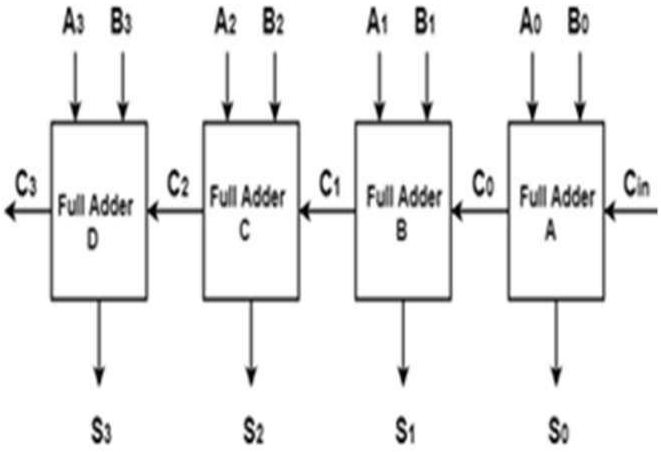

Figure 4. Ripple Carry Adder using Proposed Full Adder

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D. RIPPLE CARRY ADDER

Numerous full adder circuits can be cascaded in coordinating to add an N-bit number. For an N- bit parallel adder or Ripple Carry Adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit is shown in which the carry-out of each full adder is the carry in of the consecutive next most significant full adder. Each carry bit gets rippled into the next stage that is simply we call it as ripple carry adder. Any Half adder sum and carry out bits in the ripple carry adder is not accurate until the carry in of that stage appears. The reason behind this is propagation delays exist inside the logic circuit. The time required between the input and corresponding generated output. i.e. propagation delay. The inverter gate principle is for the given input is "0" then it produces output is "1" and vice versa. The propagation delay in the inverter gate or any gate decided by changing the states transition period. Similarly, the carry propagation delay is the time taken for the corresponding carry-in to the occurrence of the carry- out value and also, we have taken into consideration of delay value from each input to each output and tabulated them in the table. Circuit diagram of a 4-bit ripple carry adder is shown below Figure 4.

IV. RESULT AND ANALYSIS

The proposed designs of 1-bit full adder circuit with CMOS technology have been simulated by using Cadence tool. The schematic result of proposed 1-bit full adder are shown in Figure 5. Synthesis result of 1-bit full adder circuit is presented. Synthesis result of power for 1-bit full adder and output waveform of power for 1-bit full adder are shown in Figure 5.
The 4-bit ripple carry adder schematic representation is shown in below Figure 6. The RCA is having 4 bits of data from A0-A3 and similarly data B0-B3. In adder circuit initial carry bit Cin=0. Here we used the table 2 for the validation of the circuit. The simulation results are verified using the Cadence tool, Figure 7 shows the simulated wave forms of the ripple carry adder. power dissipation & delay comparison are shown in Table 3

	A				B				Sum				Carry
Cin	A3	A2	A1	A0	B3	B2	B1	B0	S3	S2	S1	S0	Cout
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	1	0	0	1	0	0
0	0	0	1	0	0	0	1	0	0	1	0	0	0
0	0	0	1	1	0	0	1	1	0	1	1	0	0
0	0	1	0	0	0	1	0	0	1	0	0	0	0
0	0	1	0	1	0	1	0	1	1	0	1	0	0
0	0	1	1	0	0	1	1	0	1	1	0	0	0
0	0	1	1	1	0	1	1	1	1	1	1	0	0
0	1	0	0	0	1	0	0	0	0	0	0	0	1
0	1	0	0	1	1	0	0	1	0	0	1	0	1
0	1	0	1	0	1	0	1	0	0	1	0	0	1
0	1	0	1	1	1	0	1	1	0	1	1	0	1
0	1	1	0	0	1	1	0	0	1	0	0	0	1
0	1	1	0	1	1	1	0	1	1	0	1	0	1
0	1	1	1	0	1	1	1	0	1	1	0	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 2: Truth table of 4-bit Ripple Carry Adder

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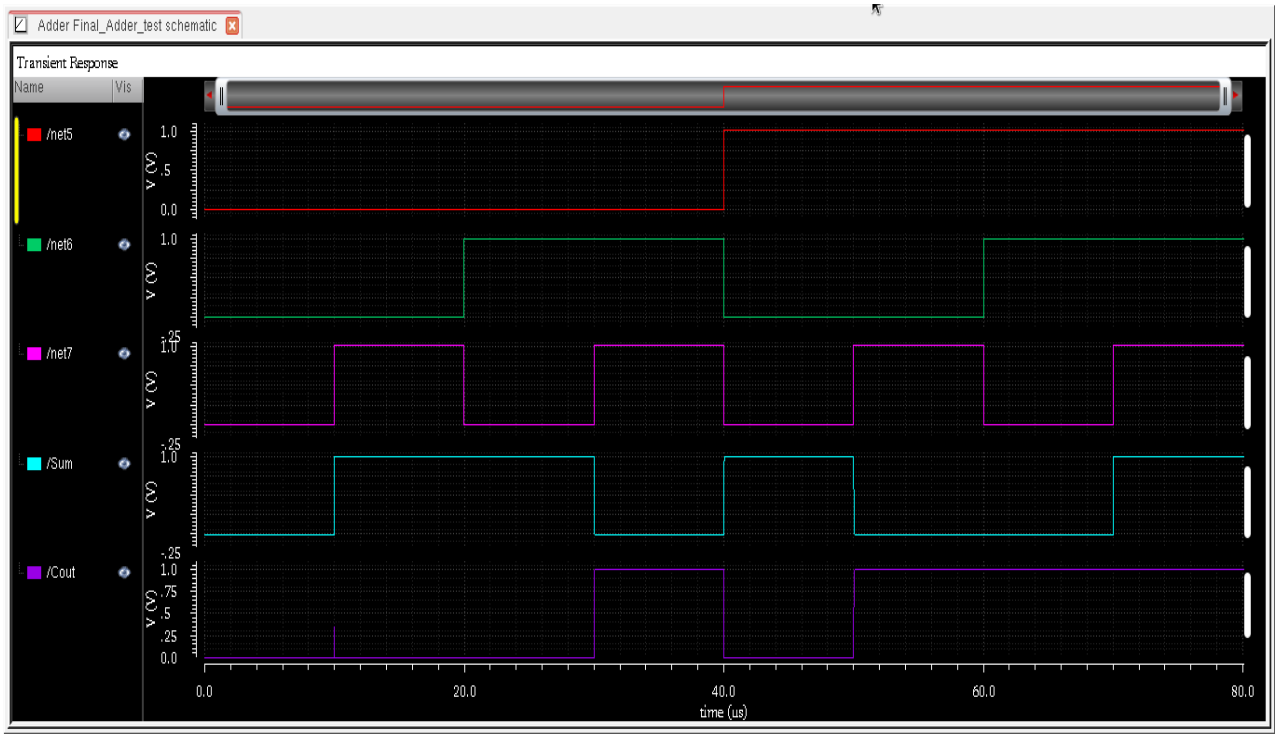

Figure 5. Waveforms of 1-bit Full Adder

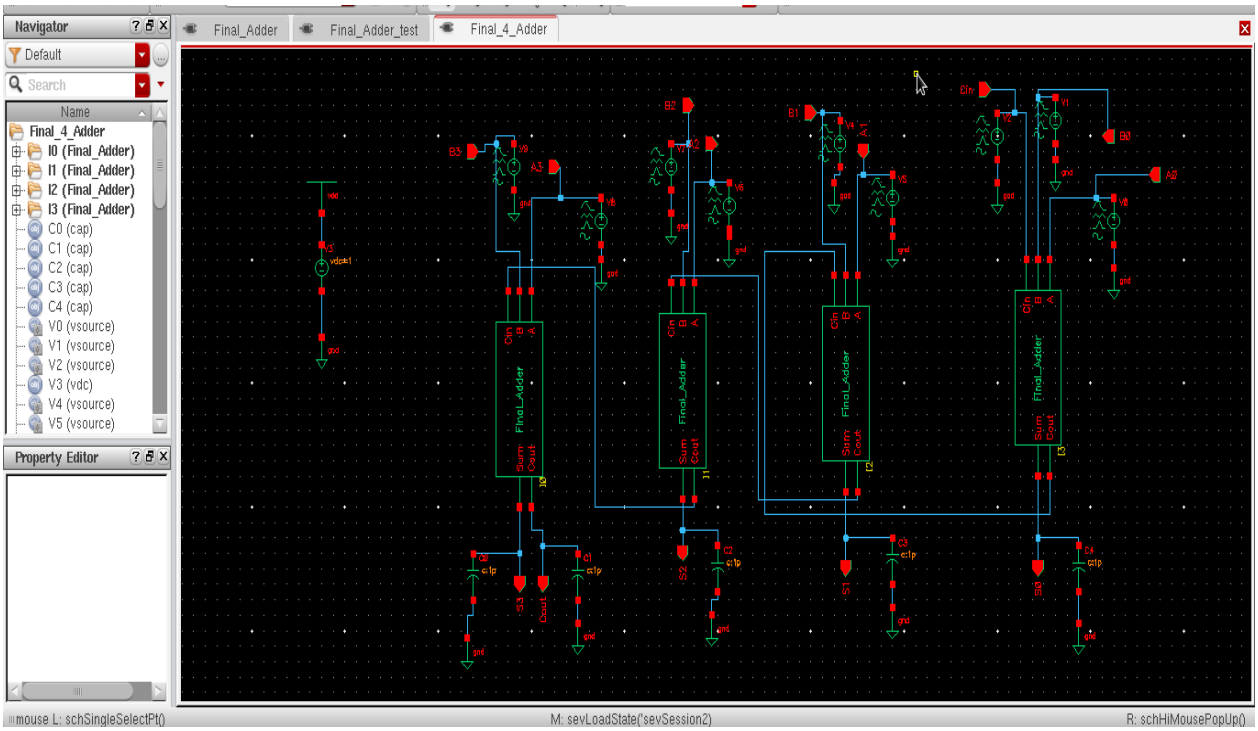

Figure 6: Schematic Representation of Ripple Carry Adder

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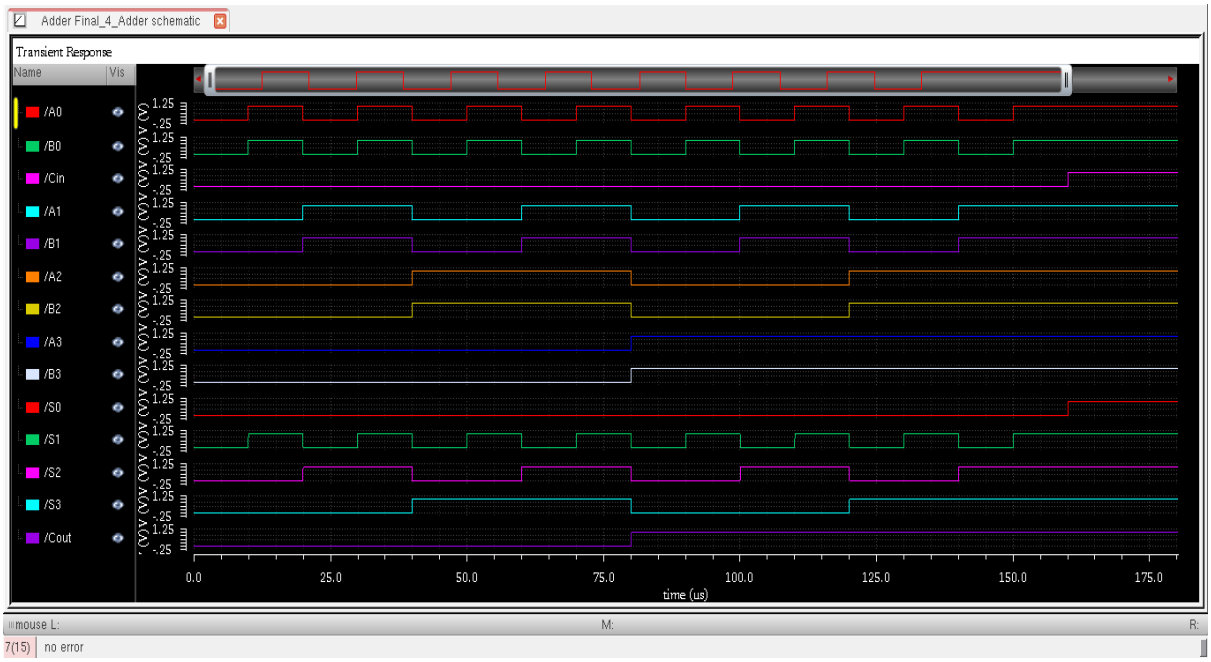

Figure 7: Waveforms of 4-bit Ripple Carry Adder

Table 3: Average Power and Delay Comparison

Technique	Average Power	Delay
Existing 1-bit Full adder	79.12nw	79.999811us
Proposed 1-bit Full Adder	56.38nw	79.995850us
Existing 4-bit Ripple Carry Adder	192.7nw	439.98098us
Proposed 4-bit Ripple Carry Adder	78.05nw	439.86834us

V. CONCLUSION AND FUTURE WORK

To detraction the power and setback time in the VLSI designs biggest challenge issue to overcome those issues, my proposed idea is one of the best techniques while compared with the other existed conventional works. Based on these inputs one can develop the superior full adder with the help of LECTOR and Junction Less Transistors. The suggested techniques are the best methods to improve the performance by minimizing the power and delay.

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