ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2016

Low Phase Noise, Current Starved Ring VCO with Wide Tuning Range and Improved Linearity

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ABSTRACT: This paper presents the design of a low phase noise voltage controlled ring oscillator (VCO) with wide tuning range. The circuit consists of a chain of current starved inverter with transmission gates. The proposed circuit is implemented in a 0.18μm CMOS technology. By varying the control voltage of VCO from 0.5 to 2.5V, the tuning range from 30 MHz to 1.13 GHz is attained.The Phase Noise at 1MHz offset frequency is -99.70dBc/Hz.

KEYWORDS:Current Starved VCO, Transmission gate, Tuning range, Phase noise.

I. INTRODUCTION

Phase Locked Loop (PLL) plays a crucial role in many electronic communication systems which consists of phasedetector, low pass filter (LPF), voltagecontrolled oscillator (VCO) and a divider circuit [1],[2].VCO is one of a major block of PLL system operates athigh frequency. Low power VCO design is important for PLLdesign to reduce power consumption. There are two types ofVCO which is widely used in nature: LC oscillator and ringoscillator or current starved VCO. LC oscillator shows betterphase noise performance but occupies large area due to on spiral inductor winding which is undesirable for design costand also the tuning range is less or limited for LC-VCO. On the other handfor CS-VCO, the phase noise performance is not too good as compared to LC-VCO but the tuning range is much large and also the area occupied by CS-VCO is very less. The wide tuning range of CSVCO is helpful toovercome the variation in the process. The main motivation behind the design of such kind of CSVCO is toreduce the power consumption, area occupied by the PLL and to reduce the phase noise performance for PLL circuit as well. VCO isan important part for many RF transceivers for frequencyselection and signal generation.

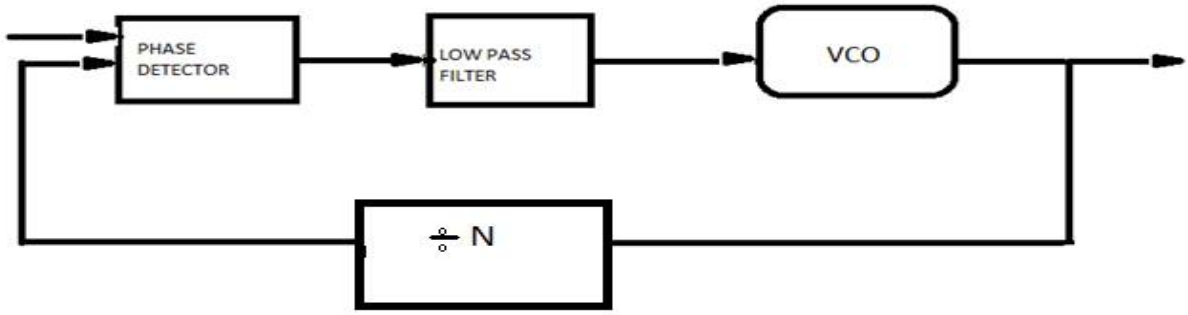

Fig.1 Block diagram of Phase Locked Loop (PLL)

The whole paper is divided into five sections where Section II contains the related work done, section III gives the outline of proposed 3 stage CSVCO, Section IV mark outsthe simulation results and the gist of the paper is concluded in Section V.

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II. RELATED WORK

In [3] design of a voltage controlled ring oscillator is proposed. The proposed design allows an implernentation of a low frequency ring oscillator using relatively small device and less number of stages. In this work authors have increased the delay of the circuit by adding a controllable resistance at an input of each inverting stage. A tuning range from 40Hz to 380MHz was achieved using the proposed circuit which enables output voltage to swing faster than the conventional one. Here the resistances of the MOS transistors are controlled by their gate voltages.

To achieve variable oscillation frequency in VCO three control methods were implemented [4]. However, capacitance controlled method is less widely used because the capacitance of the dummy transistors cannot be changed sufficiently to get a wide range of the oscillation frequency. And at the same time large capacitance area is required for very low frequency.

This paper [6] compares the performance of two VCO's for PLLviz a current starved VCO and a source coupled VCO. The result depicts that a RC based current starved VCO is superior to source coupled VCO in respect of chip area, power consumption and tunable frequency range.

The paper [7] mainly concentrates on design of current starved voltage controlled ring oscillator for ultra-low power applications. The performance comparison is done with respect to frequency stability and power consumption. In this paper dynamic threshold MOSFET technique was optimized to have ultra- low power with enhanced speed.Here, Current Starved DTMOS connection of VCO shows 48% higher speed at the cost of 18.9% increase in power consumption over conventional VCO at 0.4 V.

Reference paper [8] depicts a comparative study of different topologies of CSVCO. The analysis shows that 7-stage current starved VCO has better phase noise performance as compared to 3-stage VCO and 5-stage VCO's, while the power dissipation of 3 stage VCO is less as compared to 5-stage and 7-stage VCO. So it was concluded that as the number of stages increases the phase noise reduces at the same time frequency gets affected and also the power dissipation increases.

Conventional Current Starved Stages:

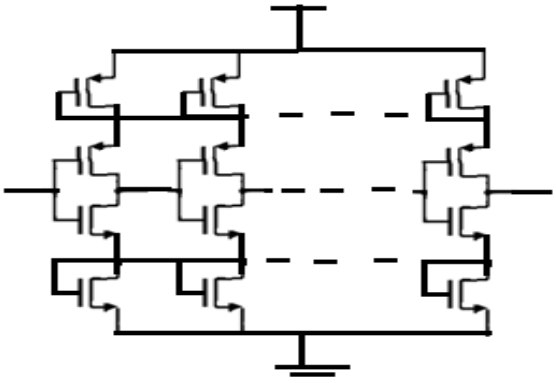

Fig.2. Current Starved Stages

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III. PROPOSED CSVCO

The phase noise is a very important parameter of VCO, the main objective of proposed design presented in fig.5 is mainly to reduce phase noise of oscillator with wide tuning range.

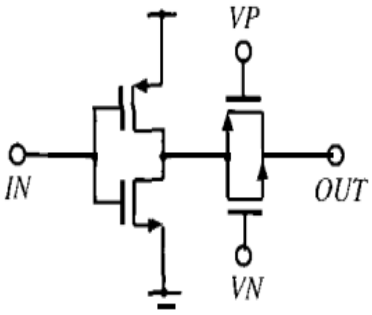

Fig.3 Inverter with transmission gate

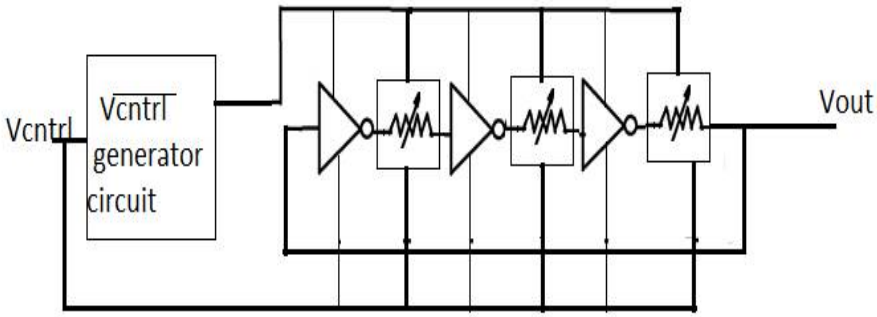

Fig.4 Proposed Ring VCO

In figure 3 inverter with simple CMOS transmission gate is presented. Here transmission gate used as a resistive delay element.

The VCO demonstrated in this work is shown in figure 4. This circuit is composed of current starved inverter chain with transmission gate connected at output of each inverter stage. The control voltage is applied to transmission gate of PMOS and NMOS transistors through $\overline{\text{Vcntrl}}$ generator circuit [9]. A full swing between the power supplies is enabled using transmission gates. The resistance of a transmission gate can be controlled by its voltages V_P and V_N. The current starved MOS used limits the current available to inverter and hence reduces the power consumption. In this circuit, the product of resistance of present stage and input capacitance of next stage gives the delay of present stage. Here the Oscillation frequency can be varied by varying the control voltage.

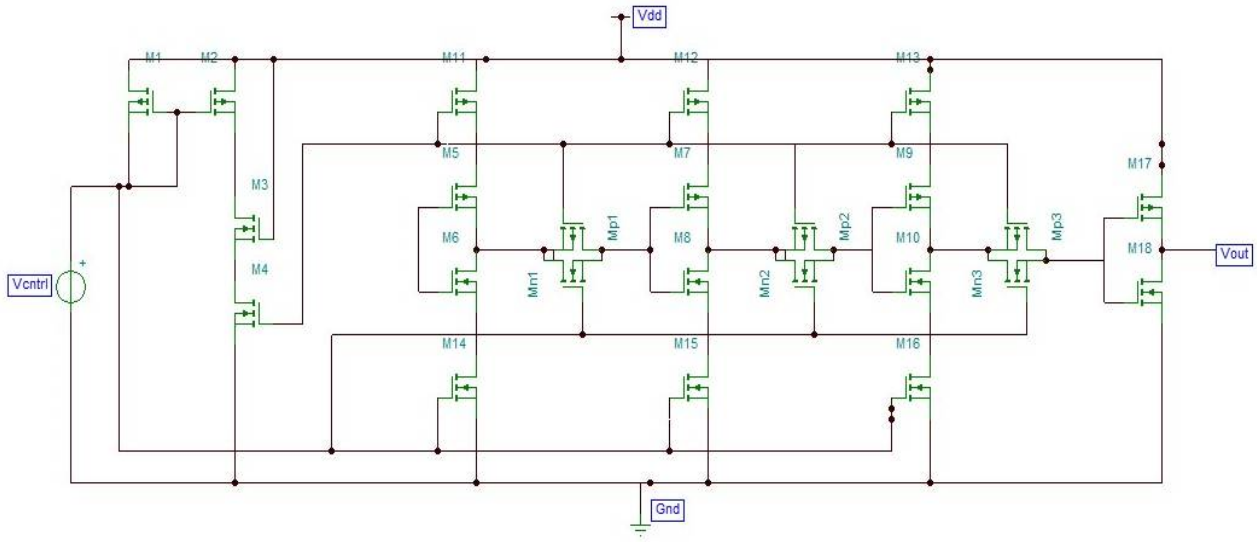

Fig.5 Proposed CSVCO based on transmission gates

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The oscillation frequency for conventional ring VCO with N odd number of stages can be given as:

$$\mathbf{F_{osc}} = \frac{1}{2NT_p} \quad (1)$$

Where T_p is the delay of one Stage

In the proposed circuit, the variable resistance $R_C$is added at the output terminal of each inverter stage. Since the MOS transistor in each inverter can be assumed as switches so it can be replaced by a resistance $1/G_M$. If the trans-conductance G_M and parasitic capacitance C_G of NMOS and PMOS transistors are equal, then the delay of each stage T_p will be approximately given as:

$$T_p = \frac{C_G(1+G_M R_C)}{G_M} \quad (2)$$

The oscillation frequency can be given as

$$\mathbf{F_{osc}} = \frac{G_M}{2N\, C_G(1+G_M R_C)} \quad (3)$$

From equation 3, it can be seen that the oscillation frequency is inversely proportional to the number of stages. So by using less number of inverter stages, high oscillation frequency can be achieved.

IV. SIMULATION RESULTS

(a) Transient Response :

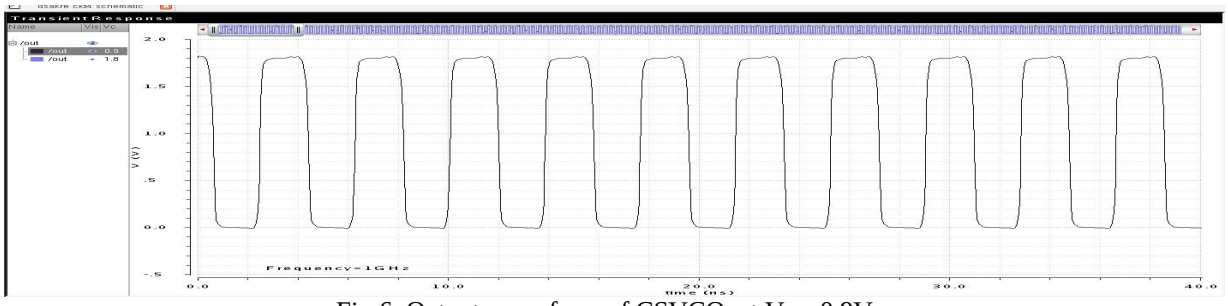

Fig.6. Output waveform of CSVCO at V_c = 0.9V

The figure6shows the output wavform of VCOat control voltage V_C =0.9 V

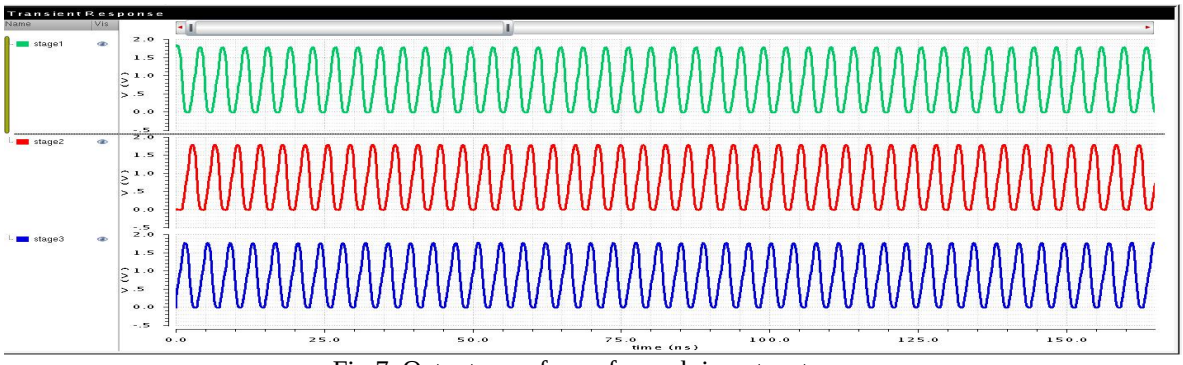

Fig.7. Output waveforms for each inverter stage

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The above fig.7 depicts the output waveforms for each inverter stage at a constant control voltage of 1.8V.

(b). Frequency Variation with Control Voltage:

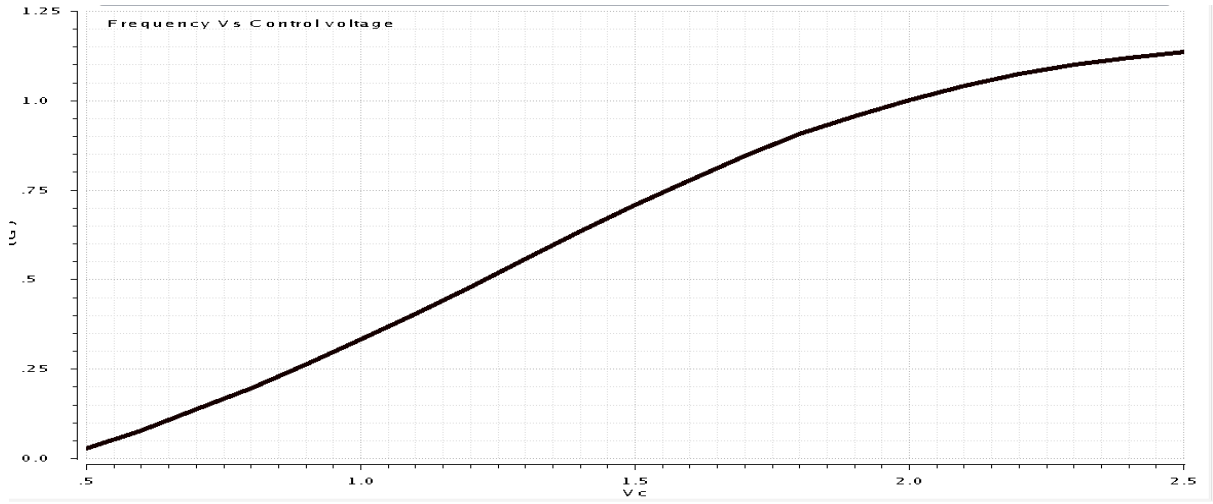

Fig.8. Oscillation frequency V_s Control voltage

Fig.8 depicts the control voltage versus frequency curve it shows linearity for wide tuning voltage. When the control voltage is varied from 0.5V to 2.5V, the resistance produced by transmission gates and the current of starving transistors (source and sink respectively)varies. Hence, the oscillation frequency of designed VCO ranges from 30MHz to 1.13 GHz.

(C). Phase Noise Response:

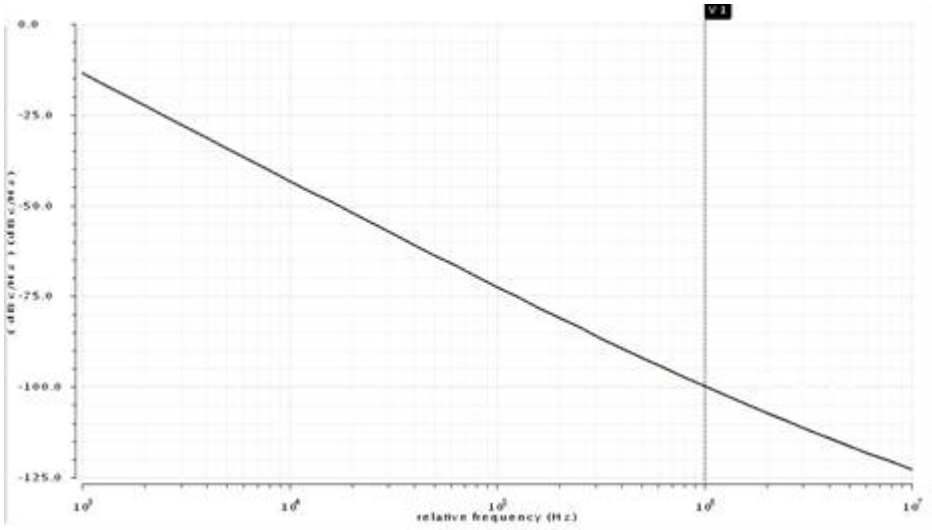

Fig.9. Oscillator phase noise at 1 MHz offset frequency

The above fig.9 shows the periodic noise response of proposed VCO which shows that the oscillator phase noise at 1 MHz offset frequency is -99.70dBc/Hz.

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TABLE.1.PERFORMANCE COMPARISON OF VCOs

	Ref.[3]	Ref.[4]	Ref[10]	Ref. [8]	This work
Technology	**0.6µm CMOS**	**0.8µm**	**90nm CMOS**	**0.18µm CMOS**	**0.18µm CMOS**
Supply Voltage (V)	**3**	**1.8**	**1.2**	**1.8**	**1.8**
Tuning Range /Oscillation Frequency	**40Hz -380MHz**	**13Hz –407MHz**	**2.00642GHz**	**1.0229 - 3.995GHz**	**30MHz - 1.13GHz**
Phase Noise (dBc/Hz)	**-**	**-**	**-87.71dBc/Hz @1MHz**	**-80.17 dBc/Hz @1MHz**	**-99.70dBc/Hz @ 1 MHz**
Power Consumption	**-**	**29.2mW**	**765.641µW**	**7.49mW**	**361.7µW**

The Table 1 shows the performance comparison of recent VCO designs. The comparison is done on the basis of frequency range, phase noise and power consumption. The proposed VCO gives better noise performance with less power consumption.

V. CONCLUSION AND FUTURE WORK

The performance of the circuit is validated by carrying out simulations for transient and noise analysis in Cadence Environment. Here CSVCO is designed in 0.18µm CMOS technology. In this proposed design, a wide tuning range with improved linearity as compared to conventional VCO is achieved usinga negative control voltage generator circuit and transmission gates as variable resistor. Apart from this a less power consumption is maintained due to current starving transistors. The tunable range from 30 MHz to 1.131 GHz is obtained with variations incontrol signal from 0.5V to 2.5V. The Phase Noise at 1MHz offset frequency is -99.70dBc/Hz and average transient power is 361.7µW.

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