Low Power and High Performance Shift Registers Using Pulsed Latch Technique

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ABSTRACT: This work presents an elegant methodology using pulsed latch instead of flip-flop without altering the existing design style. Pulsed-latch technique retain the advantages of both latches and flip-flops and thus one can achieve both high speed and lower power consumption simultaneously. In this work, pulsed latch technique has been used to reduce the delay of various shift registers without increasing any power consumption. In very high speed VLSI circuits due to heavy pipelining there is requirement of low power edge triggered flip-flops. However, for low power consumption in these very high speed VLSI circuits, the migration from flip-flop to pulsed latch technique has become a great success. In the proposed work, non-overlapped delayed pulse clock has been used in pulse latch technique to eliminate the timing problem between the pulsed latches. All the proposed shift registers have been designed in 180 nm CMOS technology and their functionality have been verified using Cadence Virtuoso. From this work, it has been concluded that, the pulse latch technique reduces the power consumption significantly in the designed registers and overall there is an improvement in power delay product. Further, it is pertinent to mention that the proposed registers require less number of transistors for their implementation as compared to conventional versions.

I. INTRODUCTION

Recently, many methodologies have been introduced for reducing dynamic power for systems – on - chip (SoCs). These methodologies, however, impose restrictive physical constraints which have schedule impact or which are heavily dependent on logic functions such as clock gating. Dynamic power is consumed across all elements of a chip. The clock network is one of the large consumers of dynamic power. Therefore, reducing power in the clock network can impact the overall dynamic power significantly. Designers already use a variety of techniques to reduce the clock power using smaller clock buffers, reducing the overall wiring capacitance, employing clock gating to reduce the dynamic power, and de cloning to move the clock buffers at higher levels of hierarchy. Even with these techniques, the dynamic power of clock network can be large since registers are used as state elements in the design. In general, a flip - flop is used as the register or you can say sequential circuits

II. PULSED LATCH CONCEPT

Flip-flops and latches are some of the most frequently used elements in digital VLSI. In synchronous systems, they are the starting and ending points of signal delay paths, which decide the maximum speed of the systems. As they are clocked at the system operating frequency, hence they consume a large amount of power. Careful design of the flip-flop and latch circuits is important to a low power VLSI system to reduce this dynamic power consumption. The clock power of a high-performance processor dominates the total power dissipation. In a commercial RISC CPU running at 200MHz, the clock power represents about 40% of the total power consumption. A large portion of the clock power is used to drive sequential elements such as flip-flops and latches. An important technique for the total chip power conservation is by reducing the clock power dissipation of flip-flops and latches. The energy dissipation of a flip-flop can be divided into two components:

1. Clock energy

2. Data energy

Oscillator Circuit for Clock Generation

Some chips contain on-chip clock generation circuits using crystal oscillator devices. The simplest oscillator circuit is shown in Figure 1 ,The inverter I0 serves as a gain amplifier for the feedback oscillator and the inverter I1 reshape the waveform to obtain a proper digital clock signal. To minimize power dissipation of tcircuit, several trade-off decisions have to be considered. For good stability of oscillation, we like to set a large gain on the inverter I0, However, a large gain results in large voltage swing and short-circuit current that increase the power dissipation. Thus, it is important to tune the transistor sizes of the inverters to achieve a proper trade-off between the "quality" of oscillation and the power dissipation of the circuit.
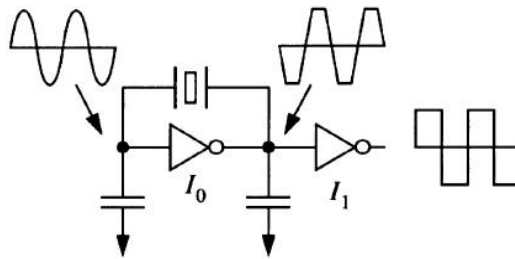

Fig. 1 An on-chip crystal oscillator circuit

PULSED LATCH ISSUES AND OPTIMIZATION

If pulse generators and pulsed latches are not placed properly, timing violations might occur. A pulse generator generates a brief clock signal to each connected latch, after receiving the clock waveform from the clock source. Latches can share the same generator with the same pulse width. A pulse generator is a combinational circuit itself. The output load capacitance would also affect the delay and driving capability of a pulse generator [8]. If a pulse generator and latches are not placed properly, the wire length might become too long and thus make the generated pulse width distorted causing serious timing violations. In Figure 4.1, load capacitance and the pulse width are inversely proportional to each other. Therefore, after circuit placement, the pulse-width degradation might cause timing constraint violations, e.g., setup/hold time violations. A multilevel pulsed latch prevents pulse width degradation.
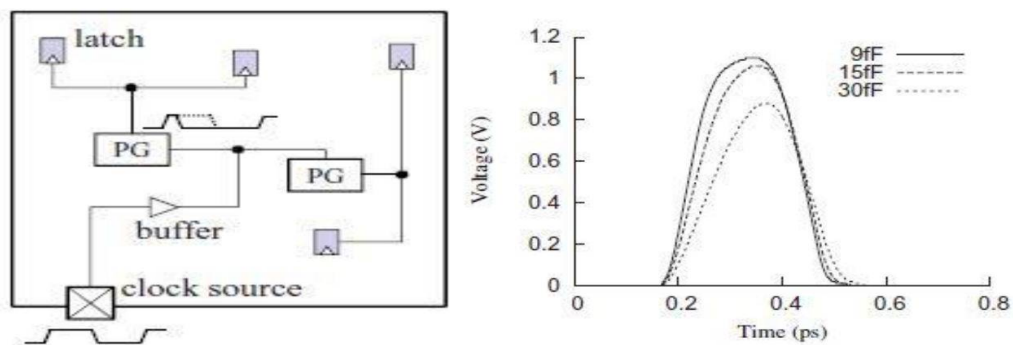

Fig. 2 Multilevel PL & Pulse width distorts as CL increases

III. PROPOSED APPLICATIONS OF PULSED LATCH

There are wide range of applications for pulsed latches. Pulsed latches could be used in portable devices where low power consumptions is necessary like the applications where flip-flops could be replaced with pulse latches i.e. in pipelining or as sequencing element or as register.

Shift Registers

A sequential logic block made up of flip-flops that allows parallel or serial loading and series or parallel outputs as well as shifting bit-by-bit is called Shift Register. It is the basic building block in a VLSI circuit. They are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register. A 16-megapixel CMOS image sensor uses a 45K-bit shift register. The area and power consumption of the shift register become important design considerations as the word length of the shifter register increases.

IV. SIMULATION RESULTS

Figure shows the schematic of D flip-flop and figure 6.2 working of flip-flop can be verified by waveform. Output follows the input and first waveform provides average power dissipation in flip-flop.
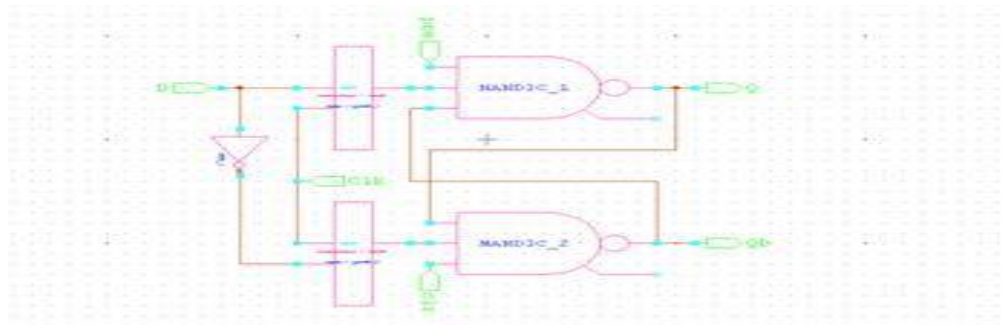

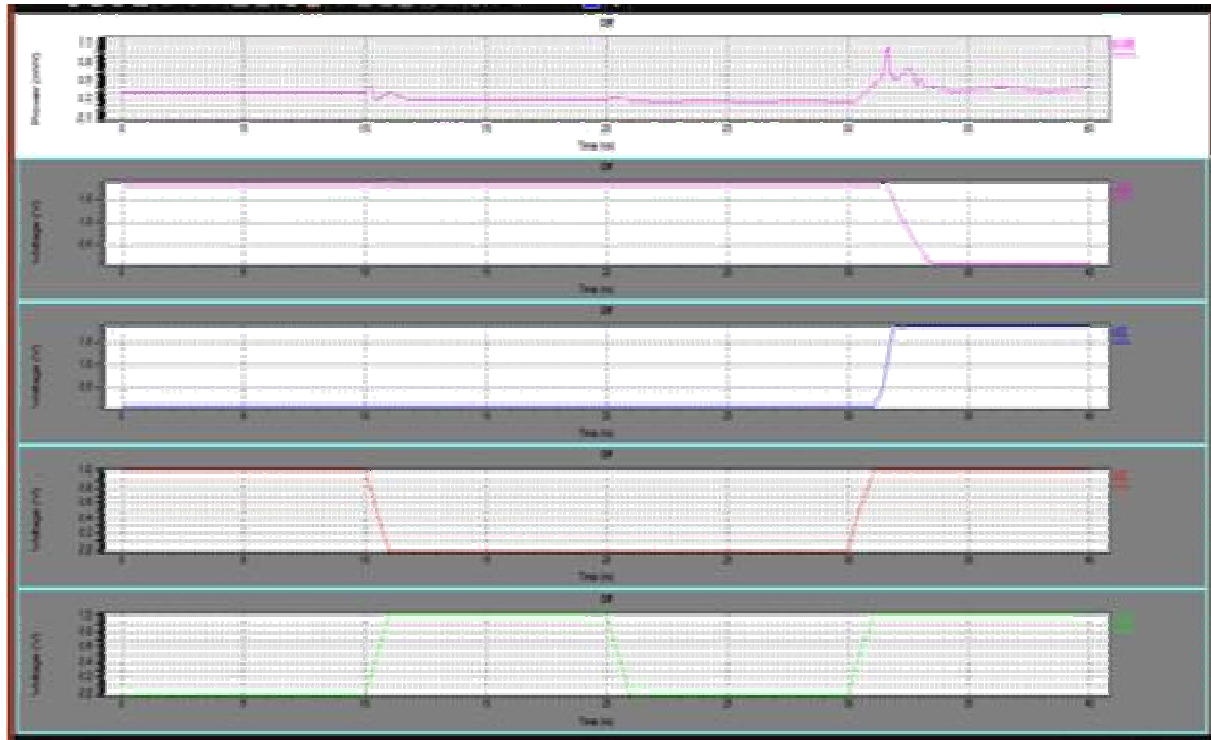Fig. 3 Schematic of D flip-flop

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Fig. 4 D flip-flop using NAND gate waveform

V. CONCLUSIONS

The requirement of replacement element for flip-flops in recent trend, led to migration from flip-flops to the pulsed latch for low power consumption, less area and delay applications. In this thesis, we have proposed different applications of pulsed latch using 180nm technology in Tanner tool v 14.1 and performance is compared with application using flip-flop. The number of transistors utilized in pulsed latch is less than that of flip-flop, hence area is significantly reduced. Pulsed latch circuit saves power consumption and power delay product in comparison with flip-flop circuit hence it can be inferred from the results that the circuits using the pulsed latches can be used instead of flip-flop for low power, less area and high speed applications. It also eliminates one latch per cycle and doesn't require clock complement. Other advantages include minimised sequencing overhead, easier timing verification, lower delay and time borrowing capability. The trading towards applications using pulsed latches from conventional flip-flop circuits in heavy pipelining, mobile devices or in low power ASIC circuits is immense achievement in field of VLSI designing.

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