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# Optical Solutions for Manycore Inter/Intra-Chip Interconnects

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**ABSTRACT:** Manycore processor system is turning into a stunning platform for applications seeking each high performance and high energy saving. Throughput, power consumption, signal integrity, pin count and routing complexness square measure all more and more vital interconnect problems that the system designer should trot out. Recent advances in integrated optical devices might deliver various interconnect solutions enabling drastically increased performance. This paper begins by outlining a number of the additional pressing problems in interconnect design, and goes on to explain system-level optical interconnect for inter- and intra-chip applications. Every section is often utilized severally to spice up performance in addition as cut back energy consumption. Simulation results show that our network can do higher outturn with lower power consumption than various styles underneath most of synthetic traffics and real applications.

**KEYWORDS**: Interconnect technology, optical interconnect, Optical network-on-chip (ONoC)

## I. INTRODUCTION

Due to frequently shrinking feature sizes, higher clock frequencies, and the synchronic growth in complexness, the role of interconnect as a dominant aspect in determinative circuit performance is growing in importance. Table 1, drawn from the 2001 ITRS (International Technology Roadmap for Semiconductors), shows that by 2010, high performance integrated circuits can count up to two billion transistors per chip and work with clock frequencies of the order of 10GHz. Coping with electrical interconnects underneath these conditions are a formidable task.

| | 2004 | 2007 | 2010 | 2016 |
|---|---|---|---|---|
| Local wiring pitch (nm) | 210 | 150 | 105 | 50 |
| Chip size at production ($mm^2$) | 310 | 310 | 310 | 310 |
| Total interconnect length ($m/cm^2$) | 6879 | 11169 | 16063 | 33508 |
| On-chip local clock (GHz) | 3.990 | 6.739 | 11.511 | 28.751 |
| Number of metal levels | 9 | 10 | 10 | 11 |
| Maximum power (W) | 160 | 190 | 218 | 288 |
| Package pin-count (high-performance) | 2263 | 3012 | 4009 | 7100 |

Table 1: Trends in some integrated circuit parameters

Manycore processor is changing into stunning platform delivering high performance with restricted power budget. It's projected that a whole bunch or perhaps thousands of cores are integrated on the chip. During a manycore processor system with such a big amount of cores, the communication demand are thus massive that standard electrical interconnects might not be able to fulfill it owing to the bandwidth density and energy consumption constraints. The limitation of the communication system can confine the manycore processor performance severely. Another limitation to the longer term manycore processor is that the power density. It is estimated that over five hundredth cores on the chip 8 nm won't be utilized owing to the ability constraint. The method yield will confine the chip space and therefore the measurability of future manycore processor. Breaking an oversized manycore processor into several smaller processors could decrease the ability density further as increase the yield. However, it needs enormous inter-chip information measure, birthing the burdens on the off-chip interconnects, that is already the bottleneck of the system

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performance. The 3-D technology may be wont to stack the chips and support low-latency inter-chip communication. However, the ability density becomes even higher.

With the recent progress in element photonics, optical interconnects may be adopted to deal with these problems effectively. Optical interconnects promise ultrahigh bandwidth, low latency, and low energy consumption. They will address each the intra-chip and inter-chip communication needs with limited power budget. As an example, an element wave guide on the chip will support an information rate of 10 Gb/s for every light-weight wavelength and multiple wavelengths are often multiplexed into the single wave guide to realize extraordinarily high information measure. The wave guide may also be connected with off-chip wave guide passively to support ultrahigh off-chip information measure.

Optical network-on-chip (ONoC) exploits optical interconnects has been suggests to interchange electronic NoC by several studies. These works chiefly focus on the intra-chip communication. In this paper a new inter/intra-chip optical network (I2CON), that supports both intra-chip and inter-chip communication. It includes multiple intra-chip sub networks, where the intra-chip and inter-chip sub networks are co designed to balance the bandwidths and also the resources likewise. Both intra-chip and inter-chip interconnects are depend on silicon photonic devices as well as modulator, photo detector, and conductor.

We compared our network with two different styles including point-to-point network and limited point-to-point network. The simulation results show that our network will achieve higher outturn with lower power consumption under most of synthetic traffics and real applications. For instance, beneath all transpose traffics, the outturn of I2CON is quite six fold over point-to-point network and more than 70%over restricted point-to-point network. The energy comparison shows that beneath uniform traffic, I2CON saves 52% and 58% of energy examination with point-to-point and restricted point-to-point networks, severally. The rest of this paper is organized as follows. 1st reviewed interconnect categorization then on-chip and off-chip optical networks and mentioned the variations between our work and connected work. Section II shows the overview of the total design. After that, design methodology in section III, the simulation and analysis are conducted in Section III. Finally, Section IV concludes this paper.

## II. RELATED WORK

Based on the silicon photonic technologies, different on-chip network architectures are projected. Kirman et al. [13] bestowed an opto-electrical hierarchic bus for future manycore processors with cache-coherence supported. Xu et al. [14] projected a hierarchic optical network and a composite cache coherence protocol, trying to acquire each benefit in snoopy and directory-based protocols. Pasricha and Dutt [15] projected an optical ring conductor to switch international pipelined electrical interconnects whereas protective the interface with bus protocol standards. O'Connor [3] bestowed a full connected ONoC based on the special λ-router with WDM technology. Shacham et al. [5] projected a hybrid ONoC combining an optical circuit-switched network with an electrical packetswitched network. Joshi et al. [16] bestowed a photonic network within which long electrical links between routers are replaced by optical ones. The projected network provides additional uniform latency and better output compared with mesh network. Cianchetti et al. [4] projected a packet-switched optical network. The packet might tolerate multiple routers without being buffered as long as no collision happens. Li et al. [17] projected a hybrid network within which optical network is employed to broadcast latency-critical messages and electrical network is employed to transfer high bandwidth traffic. Ouyang et al. [18] projected an ONoC supported freespace optical interconnects to cut back power consumption. Psota et al. [19] used WDM technology to create contentionfree network that expedited new programming model. Koohi et al. [20] projected hierarchic optical rings, where local rings are used for intranode communication and international rings are to attach the nodes. All told these styles, only one chip is taken into account, and also the networks are projected to deal with the intra-chip communication necessities. In I2CON, we also use an optical intra-chip sub network to support the on-chip communication; but a lot of significantly, we use an inter-chip network, that is very correlative with on-chip network to deal with the communication among chips. The on-chip sub network in I2CON is an optical crossbar network with ring topology. Similar topologies are proposed in [2], [6], and [21]–[23]. In crossbar style with large network resources, link sharing is vital to cut back the resource necessities. For instance, Vantrease et al. [2] proposed a crossbar, within which a conductor for information transfer is shared by multiple writers and one reader. On the opposite hand, Pan et al. [21] projected a style that a conductor is shared by single author and multiple readers. In [6], a waveguide will be any shared by multiple writers and multiple readers (MWMRs). Xu et al. [23] projected a channel

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borrowing technology to boost the channel utilization and also scale back the ability consumption. All told these styles, a waveguide is unifacial, and at any time, there may be no more than one dealing with same wavelengths in an exceedingly single waveguide. In I2CON, bidirectional transmission is supported, and we any improve the resource sharing by permitting concurrent transmissions with same wavelengths on one waveguide. Le Beux et al. [22] bestowed an optical ring operative for each 2-D and 3-D architectures. In their style, a wavelength will be reused in an exceedingly wave guide specified it may support multiple transactions to boost the performance as our I2CON. The wavelength is statically allotted supported the property requirements. Within the I2CON, one wave guide supports multiple transactions dynamically supported the arbitration. Also, bidirectional transmission is supported for constant link. Morris et al. [24] projected an optical network with 3-D stacking technology. An oversized crossbar is rotten into multiple little crossbars on completely different layers to cut back the power. the concept of rotten an extended link into some shorter links is additionally adopted in our I2CON, however we want not physically break the channel and only 1 optical layer is needed. Datta et al. [25] projected divided optical bus. Buses are segmented to cut back power consumption and that they are interconnected by electrical routers. I2CON segments the bus in additional depth and also the turnout is higher with economical arbitration and additional freelance segments. No electrical switch is required, that consumes giant power and space. The optical power is additionally lower as a result of the light can solely pass the active parts of the link. Optical interconnects for chip level communication have been projected for over a decade. Polymer waveguides on board [26], fiber [27], and free area [28] are proposed as mediums for light transmission. Among these techniques, the polymer wave guide made-up on PCB is particularly favored for its compatibility with PCB style method. Comparing with the fiber, wave guide will have smaller pitch width and so higher bandwidth density. Another feature of waveguide is that the chance to integrate splitters and combiners, which are helpful for bus-like structures [29]. In I2CON, polymer waveguides are used for inter-chip communication. Koka et al. [8], [30] projected a brand new approach to interconnect the chips along.

## III. INTERCONNECT CATEGORIZATION

Two networks, particularly point-to-point network and limited point-to-point networks, had been identified because the two most promising styles in terms of performance and power.

A) Point-To-Point Network

The basic plan behind exploitation point-to-point optical links consists of substitution electrical international links with optical ones. Analysis has been applied on analyzing the advantages of introducing optical interconnect in crucial data-intensive links, like CPU-memory buses in processor architectures. These analyses showed that point to purpose links don't confer a sufficiently high performance gain to warrant their widespread use in future technologies. In essence, the bandwidth/power quantitative relation for point-to-point optical links is beyond the electrical counterpart, however not high enough, when interface circuit power is taken into thought. Instead, it is preferable to use discipline modifications so as to change bottlenecks to be overcome, even at the expense of larger semiconductor area and power. Hence, for optical interconnect to be accepted as a real various to metallic interconnect, performance gains of at least one order of magnitude should be incontestable through circuit and device analysis advances, additionally as through application targeting.

B) Limited Point-To-Point Network

In the limited point-to-point network, the dies within the same row/column are still connected in a very point-to- point fashion, however every die is related to associate electrical router such a die will communicate with a die not within the same row/column. With associate electrical router on the trail, the flexibility is enhanced however it's at the value of additional OE/EO conversion power and conjointly the electrical change power.

C) Optical Interconnect Technology

The logical vision of I2CON is shown in Fig. 1. It is composed of associate degree inter-chip network and multiple intra-chip networks. Every intra-chip network is to interconnect all cores on identical chip plane. And therefore the inter-chip network is to string the cores in an exceedingly dimension, that is perpendicular to the chip plane. During this manner, the chips are nearly stacked sort of a 3-D chip. Optical signals will tolerate for much longer distance than electrical signals, only if an extended distance won't introduce abundant power, throughput, and latency overheads.

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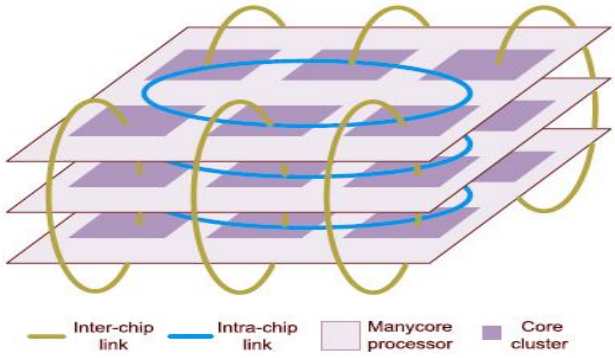


Fig 1: Logical view of I2CON

## 1. INTER-CHIP NETWORK

Inter-chip network addresses the communication needs among the chips. The necessities, like massive bandwidth density, low latency, and low power consumption, are troublesome to be consummated by the standard electrical wires. By exploiting the inherent properties of optical links, we place the chips removed from one another to scale back the ability density but still give high performance and high energy efficiency communication structure. The inter-chip network consists of data channels and the related dominance materials. There are N data channels, which are parallel to every alternative with an equivalent style. They connect the core-clusters in numerous chips. Payload data are transmitted between clusters on completely different chips. The dominance fabric consists of the dominant channels associate degree an arbiter chip. Before accessing the data channel, the clusters are needed to send requests to the arbiter chip through the dominant channels. The arbiter chip can create the arbitration and conjointly set up the data channels by causing out dominant info to the data channels.

(i) Inter-Chip data Channel

The inter-chip data channels are homogenized and parallel to each alternative in the absence of wave guide crossings. The channel consists of closed-loop with optical transceivers hooked up to them. The on-chip optical transceivers act with the semiconductor waveguides to urge the light out of the information channel or inject the light into the channel. Every closed-loop waveguide is constructed by bridging semiconductor wave guides on chip and the polymer waveguides on board. Previous works shows that the coupling between semiconductor and polymer waveguides can be created with terribly tiny loss. The coupling is achieved by adiabatic mode transformation. In a coupling with loss around 0.8 dB has been fabricated. Besides the couplers, there are no OE/EO conversions at the chip IO, saving important power consumption.

*Optical Transceiver:*

The optical transceiver consists of VCSELs, waveguides, photo detectors, and microresonators (MRs). The VCSELs function the on-chip laser sources, and arrays of VCSELs will be guaranteed on prime of the chip Compared with off-chip laser supply, the on-chip laser supply owns the potential of well reducing the static power. The on-chip laser will be powered OFF once there's no information transfer. This may considerably scale back the power consumption if the application load isn't high. Another advantage of on-chip laser is that we are able to dynamically organize the output power supported the trail loss. The disadvantage of on-chip laser is that it'll be thermally stricken by the chip. The power efficiency of the laser can drop with heat. However, these overheads are going to be well salaried by saved power that is verified in our analysis. Once VCSELs are guaranteed on the chip, the output lights are vertically with respect to the chip. To couple the vertical light to in-plane silicon waveguides, grating technology will be used. The MR is wavelength selective, and multiple MRs are used for multiple wavelengths. The performance of the optical transceiver is predicated on the coordination of the lasers, MRs, and photodetectors. The laser injects modulated light into the waveguide, the MRs switch the light from one conductor to another, finally the photo detector receives the light from the conductor

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*Duplex Transmission:*

In standard design, each link is single directional and two links are needed to support the communication between the two communication nodes. Due to the imbalance property of actual traffics, it's usually the case that one simplex link is busy with serious traffic burden whereas the alternative link is idle with no data transmission, wasting the network resources. This flexibility in direction will well handle the heterogeneous real traffics.

*Channel demarcation:*

Another feature of the channel is that, the channel is nearly divided into multiple sections, and these sections will work severally and at the same time. This can effectively improve the link utilization. The segmentation feature may be any expedited by the two-way feature in rising the resource utilization. Since the channel could be a circle, an extended link utilized by a group of action may be replaced by a compact one in opposite direction such the unused long link may be used by other transactions. This can't be achieved if bidirectional transmission isn't supported.

*Crosstalk Noise Evaluation:*

Crosstalk is often a threat to the network performance and measurability. During this section, we'll show our network is proof against such threat. As shown in Fig. 2(a), when the optical signal is switched by MR from one conductor to another conductor, some residual power are going to be left within the original conductor with an extinction quantitative relation KON. On the opposite hand, once the optical signal bypasses an OFF-state MR, some fraction power are going to be switched to a different conductor, and the extinction quantitative relation is KOFF The causeless discharge power can be the noise to alternative transactions. However, the discharge power is thus little that it'd not hurt the signal till the noise is accumulated. Luckily, after we have multiple concurrent transactions on constant channel, the noise cannot accumulate as a result of a group action that makes noise can absorb the noise created by others. As shown in Fig. 2(c), although CC(0, 1) is causing information and therefore making noise to alternative downstream clusters on the channel, it's removing noise from upstream transactions.

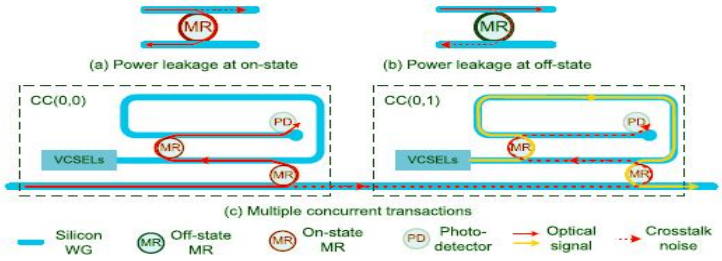


Fig 2. Crosstalk noise illustration

(ii) Control Subsystem

Before accessing the data conductor, the cluster can send letter of invitation to its management unit with the information, as well as destination ID, request ID, and packet size. Destination ID is employed to spot the receiver cluster. The request ID is hooked up for every request in order that the cluster will send multiple requests out before receiving grant info This will facilitate to boost the output of the system through pipelining, particularly once the trip delay is large. Variable packet size for every group action is supported and therefore the dimensions info is needed. After receiving the request, the management unit can check the channel states, try and reserve a channel section for this request and finally send the grant packet back to the cluster. At the same time, the management unit also will send the grant info to the destination cluster, telling it to configure the receiver to detect the incoming information. Once receiving the grants, the source cluster can send information out on the allotted channel whereas the destination cluster can configure the MRs to observe the approaching signals. Credit-based flow management is employed in I2CON, which is facilitated by the management units. Every management unit has the initial number of tokens equivalent to variety of buffer slots of each receiver. It counts down the tokens on every occasion a packet is sent. On the opposite hand, the receiver cluster can send the new tokens back to the management unit via the optical link if the buffer slots are empty. If no token is left, the requests cannot be processed by the management unit.

*Control Unit:*

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Each management unit is to operate the arbitration for all the requests on identical information channel. It is optically connected to the clusters via on-board waveguides. Since the cluster can send each requests and buffer tokens to the agent, two kinds of packets are needed. One bit is enough to identify the differentiation. From the agent to the cluster, there are also two kinds of information: 1) the grants responsive the request and 2) the grants informing the receiver that new packets area unit coming back.

## 2. INTRA-CHIP NETWORK

In I2CON, multiple homogeneous chips are used. All the core-clusters are interconnected with one another by the parallel closed-loop channels. The cluster accesses the channels with optical switch box. The communications among the cores are coordinated by the management scheme. Within the management scheme, each cluster is appointed with a cluster agent (CA). All agents are located at the chip center they are interconnected with short local electrical wires, whereas every cluster agent is connected to the corresponding cluster with dedicated optical waveguides. This approach utilizes the benefits of optical interconnects in long distance communication and electrical interconnects in short distance.

*Data Channel Design:*
On-chip data channels are composed of multiple parallel waveguides that are aligned as closed loops and pass through all clusters on the chip. Every cluster accesses all channels with optical switch box. The switch box includes several optical transceivers and they are designed within the same manner because the inter-chip ones. For on-chip network, we tend to conjointly pack W wavelengths into the waveguide for every dealing. At the supply, W MRs are used to multiplex all wavelengths into single conductor, which is not shown within the figure for simplicity. W MRs also are used at every change stage and there are W photodetectors for each receiver. An entire information channel may be a conductor with all transceivers attached that is comparable to inter-chip channel style. The sole distinction is that, the inter-chip channel is built by connecting silicon waveguides and on-board polymer waveguides, whereas the on-chip channel may be a single closed-loop silicon conductor. The similarity between on-chip and inter-chip channel design implies that on-chip channel conjointly owns two vital properties: 1) duplex transmission and 2) channel segmentation.

*Control Subsystem:*
Each dealing needs path setup before payload data transmission. Every cluster is appointed with a cluster agent that is answerable for process the requests from this cluster. A cluster agent wants discuss with alternative agents to create sure the channel is idle and destination buffer isn't full. Therefore, we tend to place all agents close with one another within the chip center. They impart victimization short local electrical wires. The comparatively massive distance between the agent and cluster is offset by the dedicated optical links that provides low communication delay. The affiliation between every agent and the corresponding cluster consists of two simplex waveguides: one for sending requests from the cluster to the agent, and also the alternative one for grant data from the agent to the cluster. The latency between cluster and agent is within one clock cycle. Before accessing the info channel, the cluster can send a request to its agent (called supply agent) with the data, including destination ID, request ID, and packet size. After receiving the request, the supply agent can discuss with the other agents, attempt to reserve a channel section for this request and finally send the grant packet containing the channel ID back to the cluster. At constant time, the destination cluster's agent (called destination agent) will send the grant data to the destination cluster. Once receiving the grants, the supply cluster can send information out on the appointed channel (identified by the channel ID) whereas the destination cluster can open the receivers to discover the info. Similar credit-based flow management is adopted to prevent buffer overflowing.

## IV. DESIGN METHODOLOGY

In order to be able to evaluate and optimize link performance criteria properly, prognostic models and style methodologies are required. Regarding the ability aspects, the aim is to ascertain the overall power dissipation for an optical link at a given rate and BER. The calculation is basically conditioned by the receiver, since the BER defines the lower limit for the received optical power. This lower limit will then be wont to calculate the specified power coupled into waveguides by optical sources, the specified detector efficiency and acceptable transmission losses. Power will then be calculable from supply bias current and photoreceiver front-end style methodologies. For integration density

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aspects, supply and detector sizes should be taken under consideration, whereas the dimension, pitch and needed bend radius of waveguides is key to estimating the dimensions of the photonic layer. On the circuit layer, the extra surface attributable to optical interconnect is within the driver and receiver circuits, additionally because the depassivated link to the photonic layer. The circuit layout downside is combined by the requirement of victimization clean provide lines to cut back noise. The data rate is basically ruled by the bandwidth of the photoreceiver: high modulation speed at the supply is usually more simply come-at-able than similar detection speed at the receiver. This is basically attributable to the photodiode parasitic capacitance at the input of the transimpedance amplifier. In an optical link there are two main sources of power dissipation: (i) power dissipated by the optical receiver(s) and (ii) energy required by the optical source(s) to produce the desired optical output power.

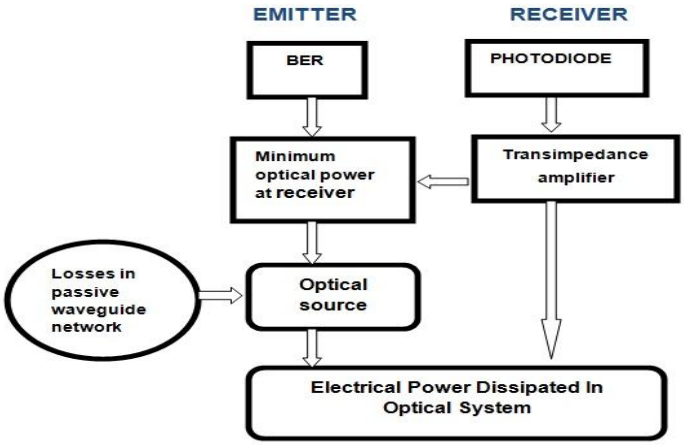


Fig 3: Methodology used to estimate the electrical power dissipation

To estimate the power dissipated within the system we have a tendency to develop the methodology shown in fig.3. First, supported the given photodiode parameters (Cd, R, Idark), is used for the planning of the transimpedance amplifier. Next, for a given system performance (BER) and for the noise signal related to the photodiode and transimpedance circuit we have a tendency to calculate the minimum optical power needed by the receiver to control at the given error likelihood, using the Morikuni formula within the preamplifier noise calculations. To estimate the optical power emitted by the supply we have a tendency to take into account the antecedently calculated nominal needed signal by the receiver and therefore the losses incurred throughout the passive optical waveguide structure. The power dissipated within the optical. Link is that the total of the power dissipated by the quantity of optical receivers and the energy required by the supply to produce the desired optical power. The power dissipated by the receivers will be extracted from transistor-level simulations. To estimate the energy needed by the optical supply, we have a tendency to use the optical device light-current.

*Design Technology Issues:*

The introduction of optical interconnect technology as an above- IC technique for normal CMOS has immense technological challenges, but the importance of EDA tools and models can't be overestimated since these are equally necessary to assist introduce the technology into existing style flows and methodologies. In an exceedingly shell, the main issue with style technology for integrated optical interconnects (and for that matter the other non-electronic technology) is that specific non-electronic tools are required however should be compatible with existing EDA flows.

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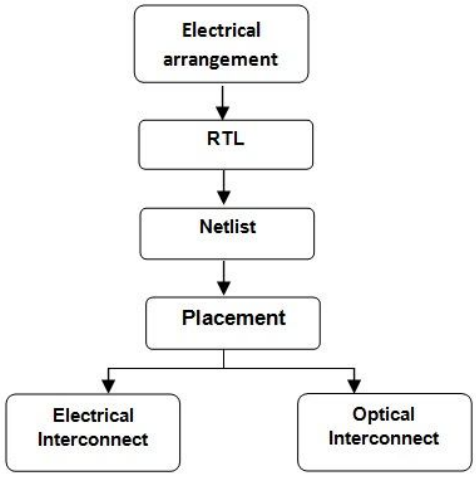


Fig 4: Design flow modifications for integrated optical interconnect

Figure 4 shows the modification of a typical style flow to include the utilization of optical interconnects. basically the choice of whether or not to use optical interconnect or not is predicated on the distance between two points to be connected and therefore the rate of the signals between the points. Of course, this info is not noted before final placement, however early constraints before system refinement are helpful to avoid repetitive style loops. These constraints are often generated early within the style cycle through the definition of fixed-complexity (constant variety of gates) zones, where ideally intra-zone links are metallic and inter-zone links are optical. This suggests that solely distance info is taken into account that is why a posteriori correction ought to be administered after final placement. This section describes the ways that are usually utilized in the optical domain and so details however such tools are often integrated into customary EDA surroundings. We are aiming at remaining compatible with top-down and bottom-up methodologies characteristic of IC style, sanctioning informatics apply. This basically needs a definition of gradable description levels for all parts, with short simulation time at system level and high simulation accuracy at device level.

## V. SIMULATION RESULTS AND FUTURE WORK

In this section, we tend to measure the performance and power efficiency of I2CON and compare it with the associated works. Two networks, particularly point-to-point network and limited point-to-point networks, had been known because the two most promising styles in terms of performance and power. In each point-to-point and limited point-to-point networks, the processor dies are placed as a 2-D array on an oversized SoI substrate. Every processor die could be a cluster with four process cores. Within the point-to-point network, each die communicates with all alternative dies with dedicated channels. There is no routing stage or arbitration needed for every channel, however it's at the prices of flexibility and measurability. The waveguides are aligned horizontally or vertically, and each point-to-point channel uses two wavelengths for data transmission. Within the limited point-to-point network, the dies within the same row/column are still connected in a very point-to-point fashion, however every die is related to an electrical router such a die will communicate with a die not within the same row/column. With an electrical router on the trail, the flexibility is raised however it's at the value of additional OE/EO conversion power and conjointly the electrical change power.

The resource comparison outline is given in Table II. In all three styles, the clock frequency is assumed as 5 GHz and therefore the data rate of every wavelength altogether three designs is assumed to be 10 Gb/s. Higher bit rate will be achieved by raising the modulation speed at the supply and detective work frequency at the receiver with the value of upper power consumption. We will explore the impact of upper WDM channel count and higher bit rate in our future work

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NETWORK RESOURCES

| | $I^2CON$ | point-to-point | limited point-to-pint |
|---|---|---|---|
| Core | 256 | 256 | 256 |
| Cluster | 64 | 64 | 64 |
| Tx/cluster | 120 | 126 | 112 |
| Rx/cluster | 264 | 126 | 112 |

Table II: Resource comparison

**Synthetic Traffics**

In performance analysis, we have a tendency to use each synthetic and real traffic. For the synthetic traffic, six traffic patterns, including uniform, Gaussian, transpose, tornado, bit complement, and neighbor traffics. The throughput comparison is shown in Fig 5. I2CON outperforms the opposite two styles below most of traffic patterns apart from uniform traffic. I2CON has lower division bandwidth and so achieves lower throughput below the uniform traffic. Uniform traffic specially favors point-to- point network as a result of all channels will be absolutely utilized. Under uniform traffic, every cluster can send data to any or all other clusters with a similar chance, and therefore the data will be transferred through the dedicated channels connecting to every cluster.

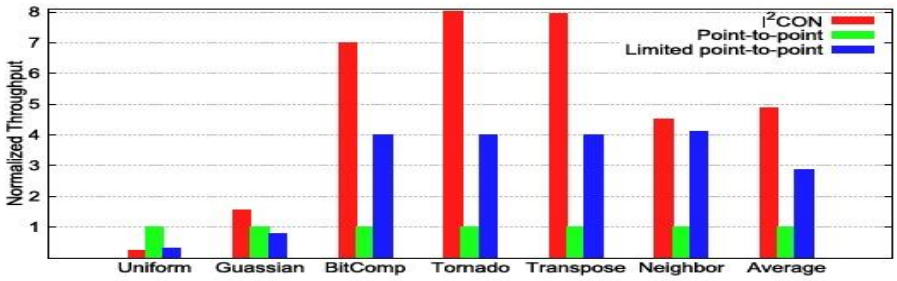


Fig 5 Maximum throughputs of three designs

I2CON achieves terribly stable throughput underneath every kind of traffic, implying that the network will well accommodate different traffic patterns. Particularly, the throughputs under permutation traffics keep high compared with the opposite two styles. Underneath bit-complement traffic, the throughput of I2CON is six fold over point-to-point network and 74% over limited point-to-point network. Under both tornado and transpose traffics, the throughput of I2CON is eight times of that of the point-to-point network, and double of the limited point-to-point network. For Gaussian traffic, we set the standard deviation to be four, implying that around 68% of traffic is destined to the neighboring eight clusters. Under this traffic, each point-to-point network and limited point-to-point network achieves lower throughout than them underneath uniform traffic. The explanation is that every cluster can solely send information to some however not all different clusters, effort several channels unused. In distinction, I2CON achieves even higher turnout under Gaussian traffic than underneath uniform traffic, showing that I2CON favors vicinity within the traffic.

## VI. CONCLUSION

The Integrated optical interconnect is one potential technological results to alleviate a lot of problems concerned in moving volumes of information between circuit blocks on integrated circuits. The advances in nanophotonics have motivated us to use the benefits of optical interconnects for future manycore processor with an outsized range of cores. During this paper, we propose an inter/intra-chip optical network known as I2CON which supports high-throughput and low-latency communication for the multichip system the properties to spice up performance as well as scale back energy consumption. The comparison with the alternatives shows that I2CON achieves promising throughput with smart energy potency. A lot of work is needed for system-level optical interconnect prediction to explore new solutions that take pleasure in advances both at the architectural and at the technological level.

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