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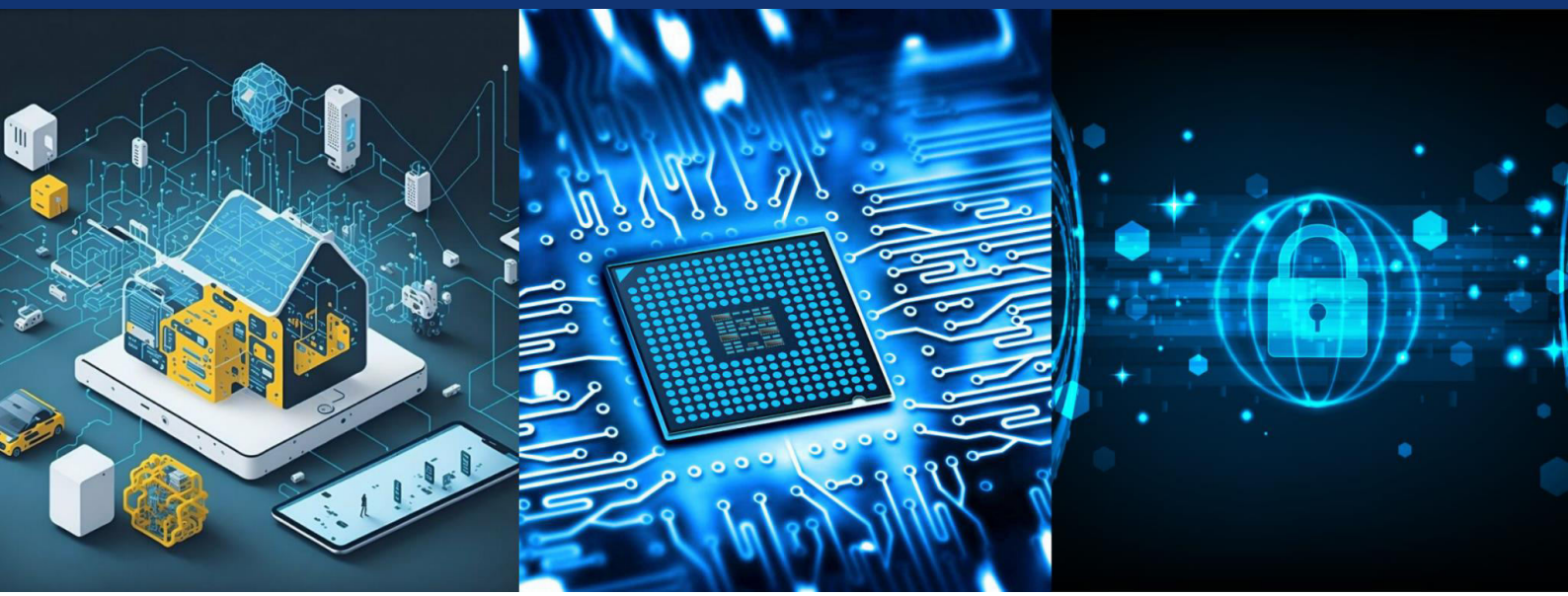

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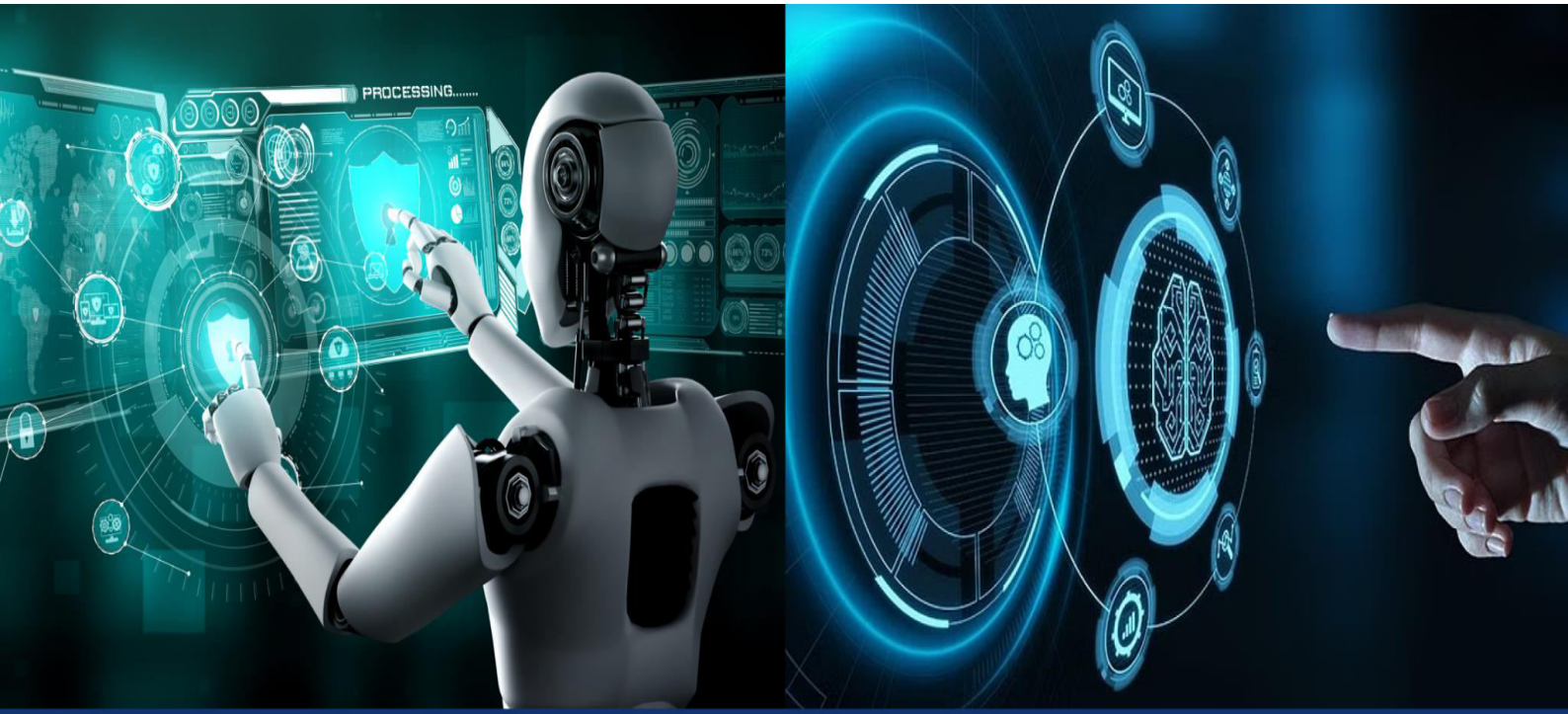

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Implementation of I/Q Generator of A 6-18 GHZ 6bit Full- 360 Degrees Vector-Sum Phase Shifter in 90nm CMOS

Goka Divya[1], Byri Rohini[2], Bushi Rajesh[3], Dronamaraju Karthikeya [4],P.V. Murali Krishna[5]

B. Tech Student, Department of ECE, GMR Institute of Technology, Rajam,

Andhra Pradesh, India[1-4]

Assistant Professor, Department of ECE, GMR Institute of Technology, Rajam, Andhra Pradesh, India[5]

ABSTRACT: This paper discusses the design and implementation of an In-phase/Quadrature (I/Q) signal generator as a key building block in a 6–18 GHz, 6-bit full-360° vector-sum phase shifter, in standard 90nm CMOS technology. Vectorsum phase shifters are ubiquitous in contemporary phased-array transceivers, radar systems, and beamforming networks, providing the ability to precisely control the phase of the signal without affecting the amplitude significantly. Among the different phase shifting methods, the vector-sum method provides better linearity, resolution, and low insertion loss across a broad frequency range. One of the most important requirements of this architecture is the generation of precise and broadband I and Q signals, which are utilized to synthesize the desired output phase by vector summation of weighted base components. The suggested I/Q generator has a broad frequency coverage from 6 GHz to 18 GHz with high-resolution phase control and digital tuning capability up to 6 bits, representing a minimum phase step size of 5.625°.

The circuit design utilizes wideband quadrature hybrid structures and broadband buffer amplifiers to facilitate good amplitude and phase balance throughout the operating band. The design is optimized for low mismatch and small quadrature phase error, which are important for phase accuracy in vector summation. The system also provides isolation between I and Q paths to eliminate LO leakage and spurious mixing products.

KEYWORDS: I/Q generator, vector-sum phase shifter, 6-bit resolution, 6–18 GHz, CMOS, quadrature signal generation

I. INTRODUCTION

As wireless communication systems evolve at a fast pace, there is increasing need for RF front-end components that are high-speed, high-frequency, and reconfigurable. Phased-array antenna systems, where electronic beam steering can be achieved without mechanical movement, have emerged as a fundamental element in cutting-edge radar, satellite communications, and 5G millimeter-wave systems. A central building block in such systems is the phase shifter, which modulates the phase of RF signals to steer the radiated beam in a specific direction.Among several phase shifting methods, vector-sum phase shifters have become popular because of their linearity, bandwidth, and digital programmability benefits. In contrast to switched-line or loaded-line structures, the vector-sum method synthesizes the target output phase by adding two orthogonal components—In-phase (I) and Quadrature (Q)—each weighted by digitally programmable gain stages. The method offers fine phase resolution and complete 360° coverage with little distortion and insertion loss.Central to the vector-sum architecture is the I/Q generator, which generates two equal-amplitude signals with a fixed 90° phase difference over the desired frequency range. Developing a broadband I/Q generator with phase and amplitude balance over a wide operating range—6 to 18 GHz here—is a difficult technical challenge, particularly in low-cost CMOS technology. CMOS, although it benefits in integration and power efficiency, contains limitations at high frequencies like greater parasitics and lower gain. This project is aimed at the design and realization of the I/Q generator block for a 6-bit full-360° vector-sum phase shifter in 90nm CMOS technology. It aims for broadband performance with high precision in phase and amplitude balance, low power consumption, and small chip area. The I/Q generator features quadrature hybrid structures and differential buffer stages, designed for minimum mismatch and wideband

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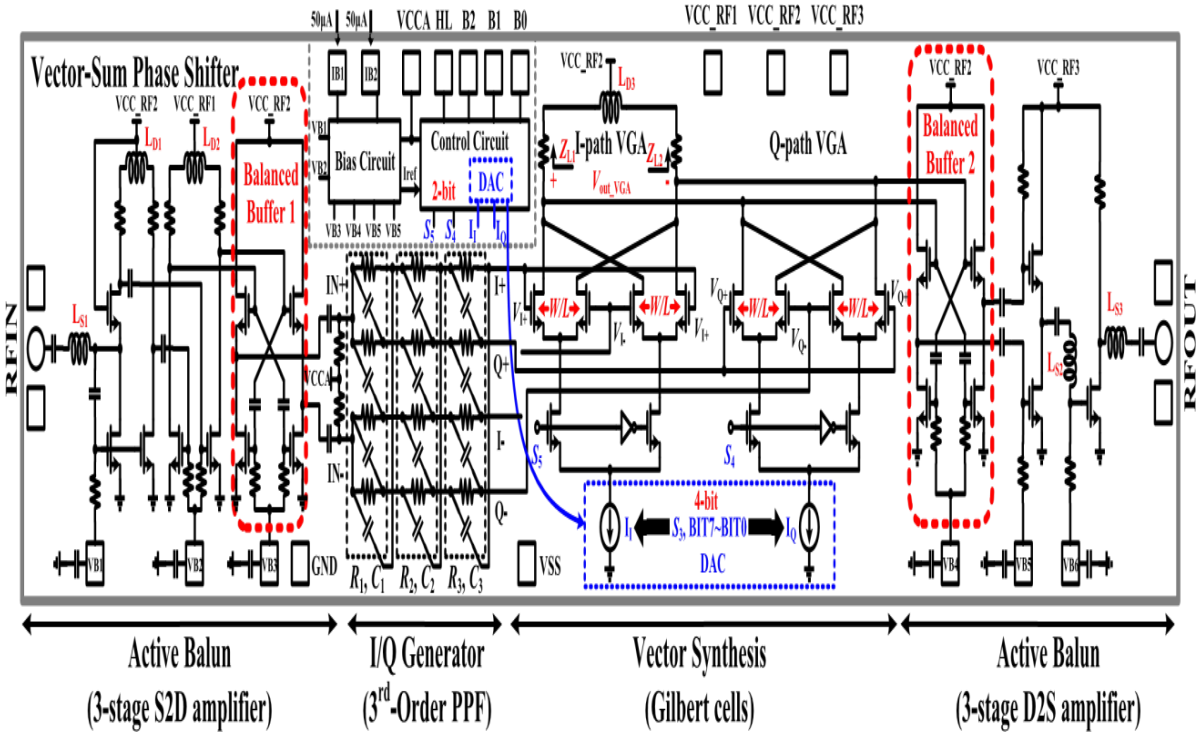
operation. The 6-bit resolution is equivalent to 64 phase steps, each 5.625°, allowing for fine-grained beam steering.By this project, the design issues of wideband quadrature generation in deep-submicron CMOS are solved, helping to develop integrated, digitally controlled phase shifters for scalable and reconfigurable RF front-end modules. Simulation verification confirms the operation of the I/Q generator and makes it an effective solution to next-generation beamforming applicationsThe I/Q generator is realised with broadband coupler structures in the form of Lange couplers or lumped-element hybrids as well as with wideband buffer stages to buffer subsequent signal tracesSome major design challenges catered to during this project include:



•Obtaining precise 90° phase difference over 3:1 bandwidth.
•Maintaining amplitude balance between I and Q paths.
•Minimizing phase error and insertion loss.
•Ensuring robustness against process-voltage-temperature (PVT) variations.
•Reducing power consumption and area for integration into compact systems.

II. METHODOLOGY

Input Active Balun: It receives one single input signal and divides it into two opposite-phased signals (referred to as differential signals). These signals are required to be used for the subsequent processes. The design of active balun is being employed here as it can drive a wider variety of frequencies and can also support amplification to minimize signal loss.

I/Q Signals Generator: This component produces two sets of signals – an "in-phase" (I) pair and a "quadrature" (Q) pair, which are 90 degrees out of phase with one another. This configuration is critical to providing precise phase corrections. The third-order RC circuit is used in the I/Q generator due to its small size and suitability over a wide range of frequencies, though it does result in a little signal loss.

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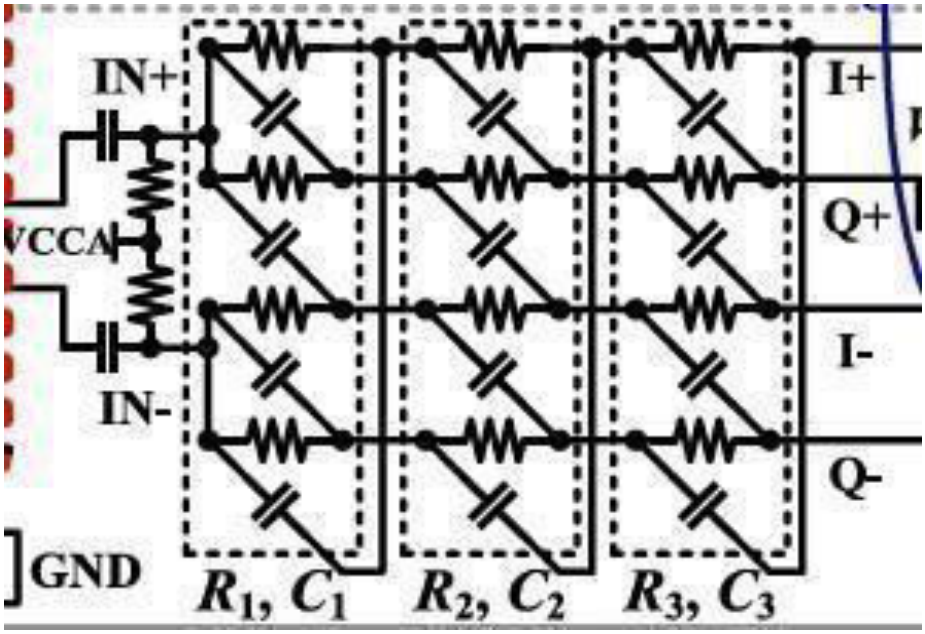
Vector-Synthesis Block: This is where the phase shifting actually occurs. The circuit regulates the I and Q signal strengths with adjustable amplifiers, which are regulated by a digitaltoanalog converter (DAC). By altering the current (the signal strength of each), the system can adjust the phase to get the desired shift.

Control and Bias Circuits: The control circuit enables the system to select particular configurations by a digital code. It picks the desired settings to obtain the precise phase shift required. The bias circuit offers stable reference currents and voltages, which ensure that the PS functions

Output Active Balun: Following the phase shift, this section accepts the two differential signals and reunites them as a single output signal. The phase of the output is determined by the strength of the I and Q signals, esulting in the desired total phase shift.



The online I/Q signals generator converts the differential input signals into the mutually orthogonal signals in two(I/Q) paths, which plays an important role in the errors and bandwidth of PS and is also the most important module of the active vector-sum PS. Currently LC quadrature all-pass filter (QAF) structure, transformer-based structure and RCPPF structure are widely used. In comparison to the other two configurations, in RC-PPF configuration, no inductor exists, with resultant small mismatches due to parasitic elements at the cost of large insertion loss. In accurate broadband quadrature signals, an RC-PPF structure is used. Two common second-order RCPPF structures. For type-I RCPPF, it may be calculated as follows:

$$V1=-V3= 1/(1+sR1C1) V0$$
$$V2=-V4=sR1C1/(1+sR1C1)$$

These are the output voltages of a first-order RC polyphase filter (PPF) stage in I/Q signal generation.They indicate how the input signal is divided into quadrature components with certain amplitude and phase relationshipsThe phase difference of the quadrature signals at the first-stage output(V1–V4) is 90◦ throughout the entire frequency band, whereas the gain is identical just at ω1=1/R1C1.At the second-stage output, it can be similarly concluded that

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$$VI+= 1-s2R1R2C1C2/((1+sR1C1)(1+sR2C2))V0$$
$$VI-=- 1-s2R1R2C1C2 /((1+sR1C1)(1+sR2C2))V0$$
$$VQ+= s(R1C1+R2C2)/((1+sR1C1)(1+sR2C2))V0$$
$$VQ-=- s(R1C1+R2C2) /((1+sR1C1)(1+sR2C2))V0$$

The second-order output quadrature signals also have a phase differenceof90◦ in the full band, and a new frequency point ω2=1/R2C2 with equal gain is introduced. Therefore, the second-order PPF can produce quadrature signals with more accuracy than the first-order one in a specific bandwidth. Similarly, it can be computed in type-IIRCPPF that

$$VI+= (1-s2R1R2C1C2 -s(R1C1+R2C2)/((1+sR1C1)(1+sR2C2))V0$$
$$VI-=-(1-s2R1R2C1C2-s(R1C1+R2C2)/((1+sR1C1)(1+sR2C2))V0$$
$$VQ+=(1-s2R1R2C1C2+s(R1C1+R2C2)/((1+sR1C1)(1+sR2C2))V0$$
$$VQ-=(- 1-s2R1R2C1C2 +s(R1C1+R2C2)/ ((1+sR1C1)(1+sR2C2))V0$$

The second order type-II RCPPF output quadrature signals gain are equal throughout the full frequency range,while phase differences are exactly 90◦ at justatω1=1/R1C1 andω2=1/R2C2. In view of the fact that phase shift precision of the PS in the four statesof90◦, 180◦, 270◦, and360◦ is very sensitive to the accuracy of the I/Q signal gain, which is the bottle neck to constrain optimization of phase shift precision, the type- IIRCPPF is better than type-I RC PPF. As f1 =(ω1/2π≈5.47GHz), f2= (ω2/2π≈20.74GHz), f3 = (ω3/2π≈13.86GHz) are spread around 4–24GHz, a wider operating bandwidth can be obtained.

Analog Behavioral Example is performed for this project under cadence virtuoso environment based on 90nm CMOS Technology

The 90nm CMOS technology node is an established, mainstream semiconductor process with a fair balance between performance, power and manufacturing cost.

It has been widely applied in RF, analog, and mixed-signal integrated circuit design, such as high-frequency applications like phase shifters, LNAs, mixers, and oscillators. With feature sizes that are small enough to support high-speed operation while having good analog properties like gain and matching, the 90nm node is still very much relevant for prototyping and research work in RFIC development. Cadence Virtuoso is a industry standard Electronic Design Automation (EDA) platform applied for custom IC design, such as schematic capture, layout, simulation, and verification. Within 90nm CMOS, Virtuoso enables access to an established PDK (Process Design Kit) composed of transistor models, standard cells, and technology rules tuned up for this node.

The Virtuoso Analog Design Environment (ADE) facilitates exact simulation of circuit performance with Spectre or other simulators, enabling designers to examine important parameters like gain, phase shift, bandwidth, noise figure, and power consumption. For layout, the tools in Virtuoso support the development of DRC/LVS-clean layouts, parasitic extraction, and post-layout simulation, guaranteeing design accuracy and manufacturability. 90nm CMOS technology was selected in this project because it can run effectively in the GHz range and can be used in wideband phase shifter design. Cadence Virtuoso was used to implement, simulate, and validate the schematic and layout of the phase shifter for performance at different operating conditions such as process, voltage, and temperature variations. To do transient analysis in Cadence Virtuoso based on CMOS 90nm technology, the initial process is to start the Virtuoso platform and open a new design library that is related to the 90nm technology file (PDK), e.g., gpdk090. This library is the working area for all circuit elements and the simulation conditions.In this library, an instance of a new cell view is opened to construct the schematic of the target circuit—such as a phase shifter, amplifier, or mixer—based on in-built components like MOSFETs (nmos/pmos), resistors, capacitors, current mirrors, and signal sourceThe circuit is then correctly connected, and pins are allocated for inputs, outputs, power, and ground. Once the schematic is verified to pass the design checks, a symbol can be created for easier reuse and hierarchical testbench configuration. A new testbench cell is then defined where the symbol of the circuit under testis instantiated, including voltage sources (VDC, VPULSE, or VSIN), input signal generators, and measurement probes. This testbench enables controlled simulation in realistic conditions. The testbench is placed into the Analog Design Environment (ADE L or ADE XL), and the designer picks the simulator (most likely Spectre) and configures transient analysis. In the transient analysis window, simulation settings like total simulation time (stop time), largest

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Before simulating, model libraries are checked or installed to guarantee correct 90nm transistor behavior. Designers also choose individual nodes or outputs in the schematic to be graphed following simulation—for instance, output voltage, I/Q signal waveforms, or bias points. After everything is configured, the simulation is run, and results are viewed in the waveform viewer (ViVA or Wavescan), where designers can examine signal transitions, delays, rise/fall times, and phase differences. This step is essential to confirm circuit performance in the time domain and assists in guaranteeing performance targets such as speed, linearity, and transient stability in analog and RF designs. Transient analysis specifically gives information not observable in DC or AC analysis, like signal distortion, settling time, and switching behavior, which makes transient analysis an indispensable step in designing and verifying circuits implemented in CMOS 90nm technology. Once the transient analysis is done, the designer can go on to perform other simulations like AC, DC sweep, noise analysis, and parametric variations to thoroughly analyze circuit behavior in various operating scenarios. These simulations assist in determining frequency response behavior, bias stability, power dissipation, and noise or mismatch susceptibility. Also, post-layout simulations may be done by reading parasitics out from the layout view to make sure real-world effects like routing capacitance and substrate coupling do not compromise circuit performance. This phase is particularly crucial in high-frequency designs such as the I/Q generator where minor layout mismatches can create considerable phase and amplitude imbalances.The design and simulation process of the I/Q generator circuit using 90nm CMOS technology was successfully carried out in Cadence Virtuoso, following a structured flow from schematic creation to transient simulation.

In the first step, a new schematic file was created under the library named generator with the cell name iq_generator. This setup was done through the New File dialog box in Virtuoso, where the design view and type were selected as schematic, and the application was set to open with Schematic Editor L. This forms the foundation of the design process, allowing the user to proceed with circuit-level development.

The second stage involved the schematic design of the I/Q generator, where a quadrature phase-splitting circuit was implemented using CMOS components. The schematic included a sinusoidal voltage input source, multiple resistor-capacitor (RC) networks, and matched transistor stages to generate four output signals with phase differences of 0°,

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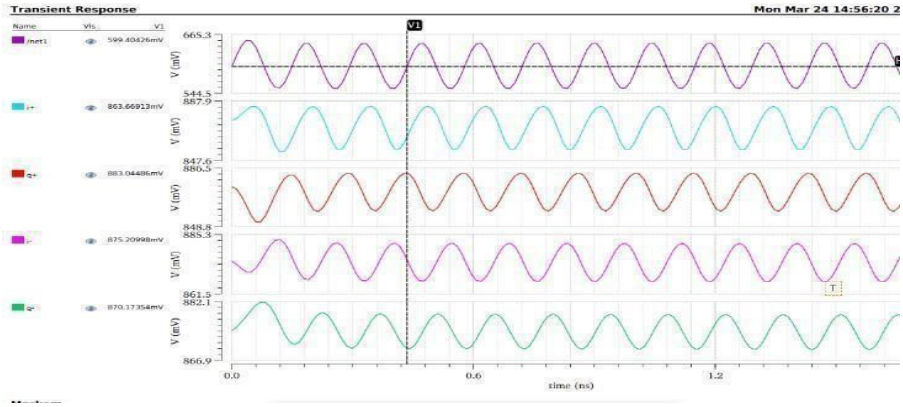
90°, 180°, and 270°. These outputs are essential for various applications in RF communication, including vector modulation and phased-array beamforming. The circuit was carefully designed to ensure symmetry and accurate phase shifts.

In the final stage, transient analysis was performed using the Analog Design Environment (ADE L) in Cadence. Simulation parameters such as stop time and step size were configured, and key signal nodes were selected for output observation. The Spectre simulator was used to run the simulation, and the logs indicated successful completion with generated .psf files for waveform viewing. This step validated the time-domain performance of the circuit and confirmed the proper generation of quadrature signals.

Overall, the entire design and simulation flow demonstrates a robust implementation of an I/Q generator suitable for frequency applications, leveraging the capabilities of Cadence tools and the 90nm CMOS process.



III. RESULTS AND DISCUSSION

The I/Q generator circuit was successfully developed and simulated. The circuit consisted of a polyphase filter optimized to generate two output signals in quadrature phase difference (i.e., having a 90° phase difference). Major findings observed:

The stimulation was a sinusoidal waveform introduced at a predefined frequency (in most cases the center frequency of interest).

The I (In-phase) and Q (Quadrature-phase) outputs were seen at the nodes as designed, with a 90- degree phase difference between them as expected.

I and Q channel amplitude balance was kept within reasonable values, proving the utility of the polyphase filter network.

The phase difference between the I and Q outputs, simulated using transient and AC analysis, was found to be verified, and it ensured that the circuit was retaining the phase accuracy over the required bandwidth

IV. CONCLUSION

The main aim of this project was to develop and integrate an I/Q generator as one of the essential functional building blocks of a 6–18 GHz 6-bit full-360° vector-sum phase shifter, based on 90nm CMOS technology under the Cadence Virtuoso design environment. The I/Q generator plays an important role in RF front-end systems, specifically in beamforming and phased-array systems, where the control over phase and amplitude is of primary importance to achieve signal direction and integrity.

In this paper, a quadrature signal generator that can provide four equally phased phase outputs (0°, 90°, 180°, and 270°) was achieved. The process entailed combining passive RC phase shift networks with current-steering logic based on CMOS devices to provide linearity, phase accuracy, and stability across a broad frequency range. Particular attention was paid to component sizing, symmetry, and layout-aware design principles to minimize mismatch,

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parasitic effects, and phase error, key in high-frequency applications. The schematic was created by employing the schematic editor within Cadence, and the circuit was thoroughly simulated employing Spectre transient analysis in ADE L. Simulation outputs confirmed the generation of quadrature outputs with proper phase spacing and waveform integrity. Performance of the I/Q generator was tested for output amplitude balance, phase shift accuracy, and time-domain signal quality to ensure it can be a dependable sub-block in vector modulators or phase shifters.

The project is able to prove the feasibility of employing 90nm CMOS technology in designing low-power and area-efficient high-frequency analog/RF circuits. The successful implementation and simulation results not only confirm the design methodology but also emphasize the applicability of such architectures in contemporary wireless communication systems, such as millimeter-wave 5G, radar systems, satellite communications, and phased-array antennas.

In summary, this work provides a solid ground for the future development of more sophisticated RF integrated circuits with phase control and vector modulation. It demonstrates the practicality and effectiveness of CMOS-based approaches to high-speed signal processing and provides additional prospectives for system-level optimization and integration in cutting-edge communications technology.

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