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# Design of CMOS Operational Amplifier in 180nm Technology

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**ABSTRACT:** In this paper we have presented a method for designing a Two Stage CMOS Operational Amplifier using Cadence Virtuoso 180nm CMOS Technology. Complementary metal oxide semiconductor technology is used for constructing integrated circuits. This technology is preferred to design opamp as CMOS devices are high noise immune and consume low static power. An operational amplifier is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output. Operational amplifiers used to perform mathematical operations in many linear, non-linear and frequency-dependent circuits. Op-amp is widely used as a building block in integrated circuits is due to its versatility. Different operational parameters are discussed in this paper. The trade-off curves are computed between various characteristics such as Gain, Phase Margin, Gain Bandwidth, Common Mode Rejection Ratio, Power dissipation etc.

**KEYWORDS**: Operational amplifier, Bandwidth, Gain, Power dissipation, CMMR

## I. INTRODUCTION

The operational amplifier is one of the most useful devices in analog electronic circuitry. Operational Amplifiers more commonly known as, Op-amps are built with different levels of complexity to be used to realize functions ranging from a simple dc bias generation to high speed amplifications or filtering. With only a handful of external components, it can perform a wide variety of analog signal processing tasks. Op-amps, are among the most widely used building blocks in Analog Electronic Circuits and are most widely used in consumer, electrical and scientific devices. They have wide applications in many analog circuit including square wave generators, switched capacitor filters, sigma delta A/D converter, sample and hold amplifiers etc.

The trend towards low power, low voltage silicon chip systems has been growing due to the increasing demand of smaller size and longer battery life for portable applications in all marketing segments including telecommunications, medical, computers and consumer electronics. Op-amps are linear devices which has nearly all the properties required for not only ideal DC amplification but is used extensively for signal conditioning, filtering and for performing mathematical operations such as logarithm, addition, subtraction, integration, differentiation etc .

### A. TWO STAGE AMPLIFIER TOPOLOGY

Two stage operational amplifiers consist of a differential amplifier in the first stage followed by a Common Source Amplifier in the second stage. Differential Amplifier stage ensures high gain and Common Source Amplifier stage further increases the gain and also provides high output voltage swing. The block diagram of a two stage operational amplifier is shown in Figure .1.

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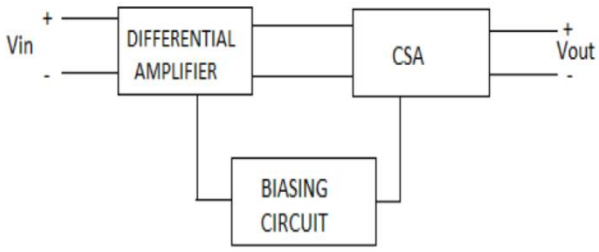


Figure 1: General block diagram of two stage Operational Amplifier [2]

The first block is a differential amplifier. It has two inputs, an inverting input and non inverting input. It provides a differential voltage or single ended voltage, depending on the configuration at the output which depends on differential input voltage. Single ended output degrades the output swing of the amplifier. As the symmetry of the circuit is lost, the Common Mode Rejection Ratio degrades.

In circuits where the gain provided by the differential amplifier stage is not enough, additional amplification required is provided by the second stage, i.e. the common source amplifier, driven by the output of the first stage. The biasing circuit provides the proper operating point to each transistor in its saturation region. An output buffer stage can be attached at the end to provide the low output impedance and larger output current needed to drive the load. For a small capacitive load output buffer is not required. When the output buffer stage is not used, the circuit acts as an Operational Trans-conductance amplifier or OTA.

## II. DESIGN METHODOLOGY OF OP-AMP

### A. SCHEMATIC OF OP-AMP

The basic 2 stage operational amplifier consists of three sections [5] :

- **Dual input Differential Amplifier**: In Fig. 2, the transistors nm0, nm1, pm0 and pm1 form the first stage i.e. differential stage of the operational amplifier.nm0 and nm1 are nmos transistors whose gate acts as the differential input node. Gate of nmos nm0 is the inverting input and the gate of nmos nm1 is the non-inverting input. In this stage current is mirrored from nm0 by pm1 and pm0 and subtracted from the current through nm1.This current mirror topology is used for converting the differential input signal to single ended output signal.

- **Output Buffer**: The Output buffer, more commonly known as Second Gain Stage, comprises of transistor nm0 and pm0 in Fig. 2. It is a common source amplifier which provides an additional gain to the amplifier. The output of the differential input stage acts as the input for this stage. The gain provided by this stage is the product of trans- conductance of pm0 and the effective load resistance i.e. the output resistance of nm0 and pm0.

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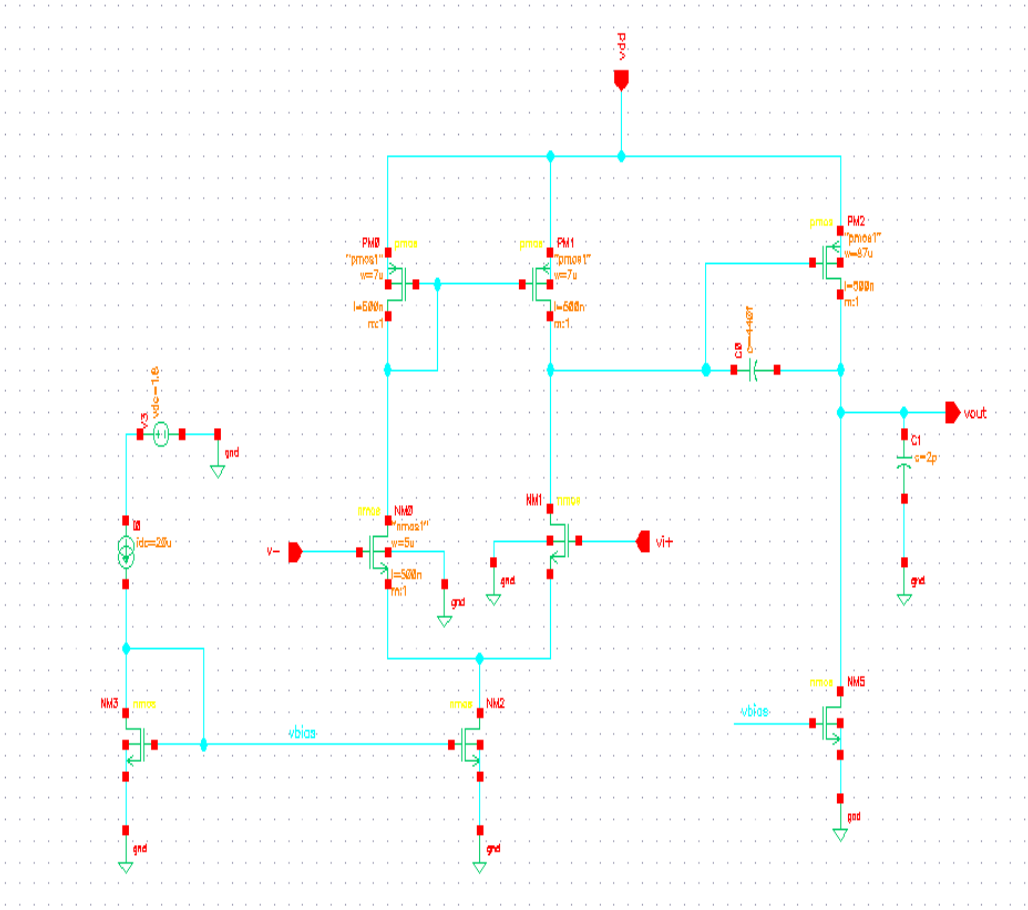


Figure 2: Operational Amplifier using 180nm technology [4]

## III.CHARACTERISTIC FEATURES OF OP-AMP[3]

- **Open loop gain:** The ratio of change in output voltage to the change in voltage across the input terminals is known as open loop gain of the op-amp. It is also known as differential mode voltage amplification.

- **Common mode gain**: The ratio of output voltage to the input voltage when both the terminals of the op-amp are supplied same potential is known as common mode gain of op-amp. It is also known as common-mode voltage amplification.

- **Common mode rejection ratio:** The ratio of differential voltage amplification to common-mode voltage amplification is known as common mode rejection ratio (CMRR). Ideally this ratio would be infinite with common mode voltages being totally rejected.

- **Slew rate:** The rate at which the output changes with respect to the time required for a step change in the input is known as slew rate of the op-amp. It is generally expressed in the units of V/ μ sec.

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- **Input common mode voltage range:** The range of common-mode input voltage that may cause the operational amplifier to cease functioning properly if the input voltage goes beyond this range is known as input common mode voltage range.

- **Unity gain bandwidth**: The range of frequencies within which the open-loop voltage amplification is greater that unity is referred as the unity gain bandwidth of the op-amp.

- **Total power dissipation:** The total dc power supplied to the device less any power delivered from the device to a load is known as total power dissipation of the op-amp. At no load, PD = VDD * I.

### A. RELATIONSHIPS DESCRIBING THE OP-AMP PERFORMANCE[1]:

1) The design procedure begins by choosing a device length to be used throughout the circuit.

2) The minimum value for the compensation capacitor $C_c$ should be 0.22 times more than $C_L$ to get phase margin 60°.

3) Based on slew rate requirements the value of tail current I0 is determined.

$$Slew\ rate\ SR = \frac{Io}{Cc}$$

4) The negative input common mode ratio range is given by

$$ICMR(-) = [\sqrt{\frac{2ID1}{\beta 1}} + Vt_1]_{max} + V_{dsat}$$

5) The positive input common mode ratio range is given by

$$ICMR(+) = [VDD - \sqrt{\frac{2Io}{\beta 3}} + |Vt_3|]_{min} + Vt_{1min}$$

6) To calculate the saturation voltage negative input common mode ratio range is used by equation .

$$V_{dsat} \geq ICMR(-) - [\sqrt{\frac{2ID1}{\beta 1}} + Vt_1]_{max}$$

7) The total amplifier gain against the specifications is given by

First - stage gain $Av_1 = \frac{gm1}{gds1 + gds4}$

Second-stage $Av_2 = \frac{gm6}{gds6 + gds7}$

8) The gain bandwidth product is given by

Gain bandwidth $GB = \frac{gm1}{Cc}$

## IV. SIMULATION RESULTS AND WAVEFORMS

### A. AC ANALYSIS

The AC analysis is used to figure out the change in the output when input is supplied with AC signals. AC analysis to figure out the frequency response of the circuit.

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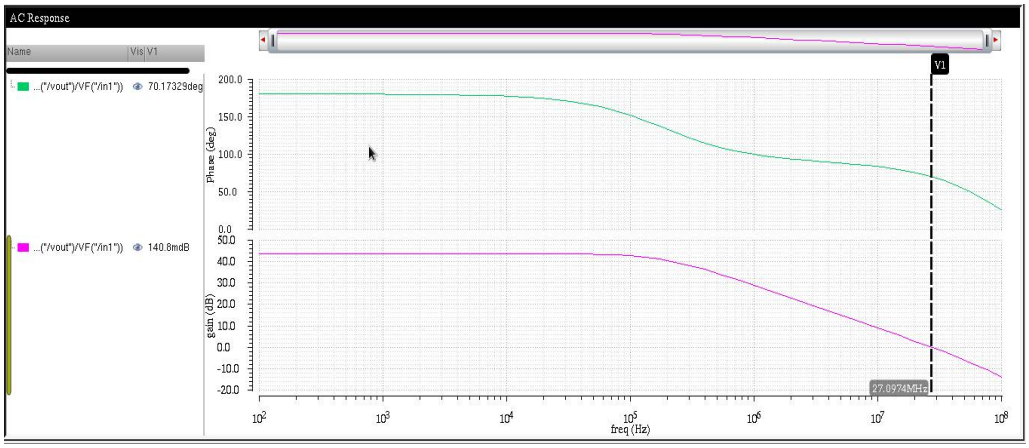


Figure 3.1:- AC gain and phase for CM 1.6 op-amp in 180nm technology

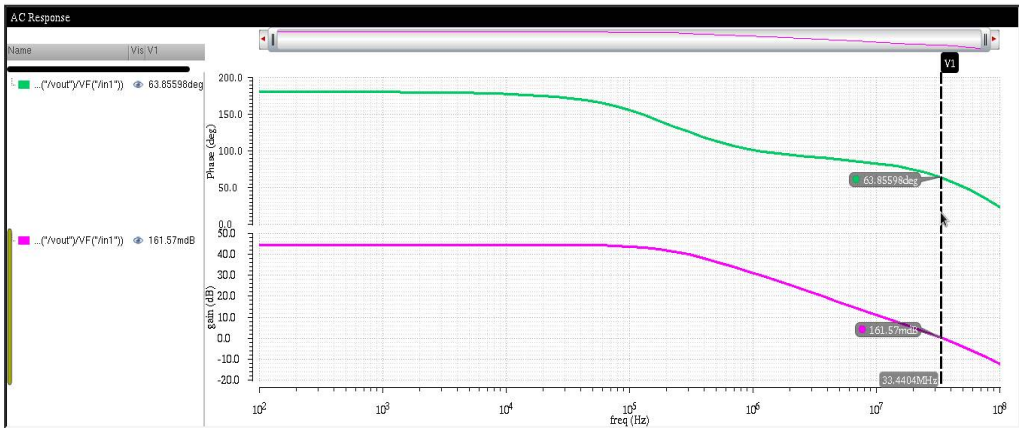


Figure 3.2:- AC gain and phase for CM 0.8 op-amp in 180nm technology

| **Parameters** | **Values** |
|---|---|
| Power supply(V) | 1.8 |
| Bias current(µA) | 20 |
| Cc(fF) | 440 |
| Cl(pF) | 2 |
| Open loop gain(dB) | 44.98 |
| Phase margin(deg) | 63.85 |
| Gain Bandwidth Product (Mhz) | 33.4 |
| Slew rate(v/µs) | 5 |
| ICMR(+)(V) | 1.6 |
| ICMR(-)(V) | 0.8 |
| Power consumption (µW) | 276 for CM 0.8V<br>300 for CM 1.6V |

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## V. CONCLUSION

CMOS two stage op-amp is simulated and analyzed in 180nm. Suitable effort is made to improve the open loop gain, phase margin, gain bandwidth product. The 180nm CMOS two stage op-amp is giving performance parameters with gain 44.98 dB, phase margin 63.85 deg, Gain Bandwidth Product 33.4 MHz, power consumption 276µW which are the basic characteristics of operational amplifier to be suitable for commercial use.

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