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Implementing an I2C Master Bus Controller in a FPGA

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ABSTRACT*:* In this paper we are implementing a I2C protocol using FPGA. The communication forms between the master control bus and slave. To implement this we have used a FPGA board which works as a master and a RTC (real time clock). This concept is widely applicable from any high speed device or low speed device to any low speed device or high speed device. When it is connected to RTC it works as slave where-as at a same time it works as a master when connected to microcontroller. In second case microcontroller acts as a slave.

KEYWORDS*:* FPGA, I2C, RTC, VHDL, Xilinx.

I. INTRODUCTION

These days the coordination of various inserted electronic modules incorporate probably a portion of these functions: digital and analog I/O ports, general purpose circuits, intelligent control, non-volatile memories (EEPROM, FLASH), volatile memories (RAM), ADC, real time clocks, among others. The coordination is conceivable in view of the improvement of various sort of wired and remote interchanges. The incorporated circuit peripherals take into consideration the cooperation among electronic devices for trading data, either the coordinated circuit plays out the default association undertakings or must be actualized by programming. The I2C (Inter-IC Communication) bus has turned into a modern true standard for short-separate correspondence among ICs since its presentation in the mid 1980s. The I2C bus utilizes two bidirectional open-channel wires with pull-up resistors. There is no strict baud rate necessity similarly as with other correspondence models. The genuine multi-ace bus permits insurance of data debasement if various bosses start data exchange in the meantime. These, and numerous different highlights of the I2C bus, give effective and adaptable intends to control works that don't require rapid data exchange, and for applications that require a little measure of data trades. Actualizing the I2C bus ace in a FPGA adds the well known correspondence interface to parts that don't have I2C interface coordinated on chip. In the meantime, the FPGA opens up the on-board microcontroller for heavier undertakings in the framework.

There are numerous purposes behind utilizing sequential interface structure a lot progressively vital applications incorporates sequential correspondence like sensors correspondence with PC. Numerous regular embedded framework peripherals, for example, ADC or DAC, LCDs, serial interfaces and temperature sensors. Serial interface enable processors to impart without the requirement for shared memory and the issues they can create. Inter-Integrated Circuit, abridged as I2C is a sequential bus short separation protocol designed by Philips Semiconductor to exchange data among ICs. On account of points of interest in straight forwardness and low assembling expense, I2C is these days a standout amongst the most prevalent sequential bus correspondence protocols in the market together with other serial bus communication protocols, for example, SPI, UART, CAN, USB, etc. There are numerous devices, which have I/O I2C interface and speak with different devices following the I2C protocol. Instances of I2C good devices are Analog to Digital Converter, Digital to Analog Converter, EEPROM, Real Time Clock, Real Time Calendar, Temperature Sensor, LCD interactive media shading contact board from Teras IC, etc.

In the realm of serial data communication, there are protocols/ protocols like RS-232, RS-422, RS-485, SPI (Serial peripheral interface), Micro wire for interfacing rapid and low speed peripherals. These protocols require more stick association in the IC(Integrated Circuit) for serial data communication to occur, as the physical size of IC have diminished throughout the years, we require less measure of stick association for serial data transfer. USB/SPI/Micro wire and for the most part UARTs are on the whole only 'one point to one point' data exchange bus frameworks. They

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use multiplexing of the data way and sending of messages to support numerous devices. To conquer this issue, the I2C protocol was presented by Phillips which requires just two lines for correspondence with at least two chips and can control a system of device chips with only a two GPIO pins while, different bus protocols require more sticks and flags to interface devices.

In the world of numerous application based item it is particularly an obligatory to have various devices connected with a framework, this incorporates peripherals following diverse correspondence protocols also. These prerequisites offer ascent to the requirement for a middle of the road framework which can go about as an extension between 2 devices following diverse correspondence protocols. This is the place I2C master controller configuration is exceptionally helpful. Today a framework is connected with various devices and makes the correspondence smooth and quick, I2C protocol is considered as one of the absolute best. The EEPROM, ADC and RTC will require an interface for correspondence between them. So I2C bus is utilized as an interface between them. It is utilized to limit framework level interconnect. This rearranges the framework level structure and the plan of the motherboard and related chip-sheets. Additionally transmitting data over the I2C bus will enhance framework execution since the transmission of computerized data is considerably less helpless to impedance from ecological clamor sources. I2C Bus gives great help to correspondence with different moderate, on-board fringe devices that are gotten to discontinuously, while being very unobtrusive in its hardware asset needs. It is a low-data transfer capacity, short-separate protocol. Most accessible I2C devices work at rates up to 400 Kbps, with some wandering up into the low MHz extend. The I2C bus has turned into the accepted world standard that is currently utilized in various coordinated circuits ICs. By utilizing the I2C protocol in a plan, a significant part of the helper bolster hardware, for example, address decoders and standard logic entryways required for other specialized strategies can be dispensed with. In an I2C bus, there is no focal server to determine data clashes. The crashes are averted utilizing the wired-and designs of the serial data (SDA) line and the serial clock (SCL), and data misfortune is forestalled by the way that each byte on the SDA line needs to pursue by a recognize . The model can be utilized as an master or as a slave or both.

II. NEED OF I2C

The on-chip RAM (EEPROM), Oscillator (RTC), ADC and I2C Interface will be coordinated for the reason to Communicate between them. The contiguity of a RTC and an on chip RAM presents a quick requirement for an data correspondence between the chip and a host PC to send data on the RAM. To limit the framework level interconnect, proposed to transmit the substance of the RAM putting away the outcomes back to a host PC by means of a sequential bus , the I2C Interface. This extraordinarily rearranges the framework level plan and specifically the structure of the mother-board and related chip-boards. Besides, putting away data in a computerized organization on-chip before transmittal to a host PC over the I2C Interface will result in an enhanced framework execution since the transmission of advanced data is considerably less vulnerable to obstruction from sources of environmental noise.

III. PROBLEM STATEMENT

In this dissertation implementing I^2C bus protocol for interfacing low speed peripheral devices on FPGA. It is also the best bus for the control applications, where devices may have to be added or removed from the system. To perform communication between various circuit boards in system I^2C protocol is used without or with cable which depends on distance and data transfer speed. With the help of I^2C bus communication between master and slave is done where master controller is used to send and receive data to and from the slave. The low speed peripheral is interfaced with I^2C master bus and synthesized on SPARTAN 3ANBoard.

IV. LITERATURE SURVEY

[1] Prof. Jai Karan Singh, “Design and Implementation of I2C master controller on FPGA using VHDL,” IJET, Vol. No. 4, Aug-Sep 2012.The focus of this paper is on I2C protocol following master controller. This controller is connected toa microprocessor or computer and reads 8 bit instructions following I2C protocol. The instructions are then processed and converted to instructions which follow SPI protocol. 32 bit register is designed to send data serially as per SPI instructions. The complete module is designed in VHDL and simulated in ModelSIM. The design is also

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synthesized in Xilinx XST 12.1 and optimized for area and power. This concept is widely applicable where a microprocessor wants to communicate with SPI device. This module acts as a slave for the microprocessor at the same time acts like a master for the SPI device which can be considered as a slave. This design is customized for slowing the data rate according to SPI device, which assures no data loss.

[2] Trupti D. Shingare, R. T. Patil, "SPI Implementation on FPGA," International Journal of Innovative Technology and Exploring Engineering (IJITEE), Volume-2, Issue-2, January 2013.The SPI is a full-duplex, synchronous, serial data link that enables communication between a host processor and peripherals. Based upon Motorola's SPI-bus specifications, version V03.06, release February 2003, the designs are general purpose solutions offering viable ways to controlling SPI-bus, and highly flexible to suit any particular needs. However, Field programmable gate array devices offer a quicker and more customizable solution. This paper provides a full description of an up to date SPI Master/Slave FPGA implementations, In conformity with design-reuse methodology.

[3]ArvindSahu,Ravi Shankar Mishra,PuranGour, "Design and Interfacing of High speed model of FPGA using I2C protocol," Int. J. Comp. Tech. Appl., Vol 2 (3), 531-536.Once the I2C protocol is being designed for interfacing the devices with each other (i.e. FPGA with OV7620) over a serial data line for getting high speed without data loss, as compare to any other communication methodology. The main purpose for developing the protocol is not only high speed communication but keep control on the each register inside the devices as well as the data that can be saved on registers, through this we are able to control more than 100 parameters of the devices, few are discuss in this paper. The design is use in surveillance system to make the overall system more efficient and accurate. The design methods are developed in VHDL and simulate on ModelSIM and implemented on FPGA board.

[4] Pankaj Kumar Mehto, PragyaMishra ,SonuLal, "Design and Implementation for Interfacing Two Integrated Device Using I2C Bus, " International Journal of Innovative Research in Computer and Communication Engineering, Vol. 2, Issue 3, March 2013. In this paper we focus on the design of I2C bus controller and the interface between the two integrated devices i.e.microcontroller and EEPROM like as a master controller and a slave for serial communication in embedded system. The components of the I2C bus controller is consist of only a bidirectional two wires and standard protocol which communicate between two integrated circuit or device. First one is serial data (SDA) line and second is serial clock (SCL) line. The I2C protocol was given by Philips Semiconductors for faster devices to communicate with slower devices and each other without data loss. The complete module is designed in VHDL and simulated in ModelSIM. The design is also synthesized in Xilinx XST 14.1

[5] J. J Patel, B. H. Soni, "Design and Implementation of I2c Bus Controller Using Verilog," Journal of Data, Knowledge and Research in Electronics and Communication Engineering Nov 12 To Oct 13, Vol. 02, Issue – 02, page no. 520-522.The I2C protocol was given by Philips Semiconductors in order to allow faster devices to communicate with slower devices and also allow devices to communicate with each other over a serial data bus without data loss. I2C enabled microcontrollers like PIC18F452 from Atmel and TMS470 from Texas Instruments requires a lot of programming and knowledge of the register structures for configuring it. Hence they are not portable. We here present a model of I2C bus controller.

V. SYSTEM ARCHITECTURE

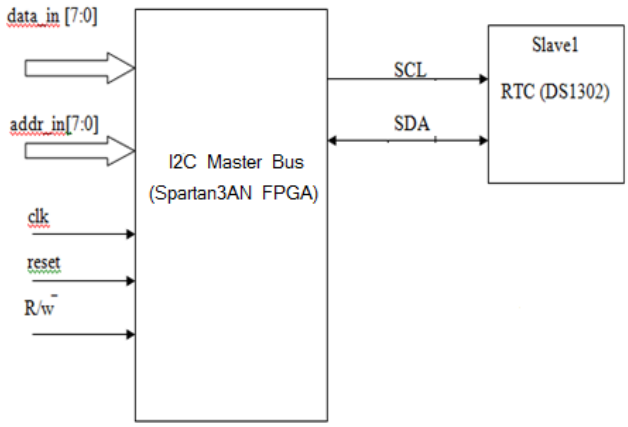

Figure1: Block Diagram

This dissertation deals with the implementation of serial data communication using I2C master bus controller using FPGA. The I2C master bus controller is interfaced with no. of slaves. This dissertation is aimed at designing of a Master controller for I2C bus using VHDL. This core, however, supports solely single master operations, in which the core is the master.

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The use of VHDL has many advantages:

• Designs can be defined at very intellectual level with the help of HDL. Designer will write his style description while not selecting any specific fabrication technology. If a brand new technology emerges, designers do not need to redesign the circuit. He simply input the design program to the logic synthesis tool and creates a new gate level net list using the new fabrication technology. The logic synthesis tool can optimize the circuit in space and temporal order for the new technology.

• By labeling the design in HDL, practical authentication of the design is done primary in the design cycle. Since designers work on the high level language, they will optimize and modify the planning module till it meets the specified practicality. Most of the design bugs are eliminated at this point.

I2C is a two wire, bidirectional sequential bus that gives successful data correspondence between two device. In Figure 5.1 data_in and addr_in are the 8 bit location given as an info. Clk and reset are the data lines used to start the bus controller process. The R/w flag is given as a contribution to show whether master or slave goes about as a transmitter in the data transmission. The I2C bus is worked around a two-wire sequential bus, SDA and SCL. Every device is perceived by a one of a kind location, and can work either as a transmitter or an as a recipient. The I2C master is the devices that starts an exchange and produces the clock for the equivalent. Any master tended to by the master is the slave.

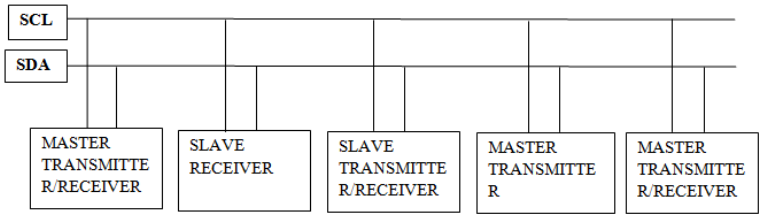

Figure2: I2C Bus Configuration using Masters and Slaves

The Interconnect Integrated Circuit or I2C interface was initially created by Philips Semiconductors Company for data exchange among ICs at the Printed Circuit Board (PCB) level in mid 1980s. All I2C-bus good devices have an interface enabling them to discuss specifically with one another by means of the I2C-bus. The idea gives a fantastic answer for issues in numerous interfacing in computerized plan. I2C is currently extensively embraced by many driving chip configuration organizations like Intel, Texas Instrument, Analog Devices, and so on. In I2C, just two bi-directional lines are required to convey data between device s, a Serial Data (SDA) line and a Serial Clock (SCL) line. Each device can be recognized by a unique 7 or 10 bits address. Only a single master can transfer data at a time though I2C is multi-master.

In fig2., there is one Master; the other devices are all Slaves. When a Master needs to initiate a communication, it problems a “START” condition. At that point, all devices, together with the opposite Masters, got to hear the bus for incoming knowledge. When the “START” is issued, the Master sends the “ADDRESS” of the Slave that it needs to speak with along-side a small amount to point the direction of the information transfer (either scan or write). All Slaves can then compare their addresses with the address received on the bus.

VI. METHODOLOGY

The proposed system aims to implementing I^2C bus protocol for interfacing low speed peripheral devices on FPGA. FPGA is reconfigurable hardware architecture. It has a flexible architecture, parallel processing maximizes data throughput, support any level of parallelism, optimal performance/cost tradeoff. FPGAs also support serial processing. I^2C protocol can also be used for communication between multiple circuit boards in hardwares with or without using a shielded cable depending on the distance and speed of data transfer. I^2C bus is a medium for communication where master controller is used to send and receive data to and from the slave. The I^2C master bus controller was interfaced

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with slave devices (RTC). This module would be designed in VHDL and the design would be synthesized using Xilinx ISE 14.7.

VII. CONCLUSIONS

This dissertation has the results of hardware implementation of I2C communication protocol on Spartan3AN FPGA interfaced with slaves RTC (DS1302). I2C bus is used in a small area network connecting ICs and other electronic systems. With help of I2C devices, any devices like microcontroller, FPGA can exchange information without special interface. I2C provides a low cost but powerful chip to chip communication link between slow speed devices with high bitrate mode to send large amount of information. Because of many merits, I2C bus remains as a one of the best serial interface to communicate integrated circuits on board.

REFERENCES

[1]BollamEswari, N.Ponmagal, K.Preethi, S.G.Sreejeesh , " Implementation of I^2C Master Bus Controller on FPGA," International Conference on Communication and Signal Processing, India, April 3-5, 2013, pp. 678-681.
[2] Prof. Jai Karan Singh, "Design and Implementation of I2C master controller on FPGA using VHDL," IJET, Vol. No. 4, Aug-Sep 2012.
[3] Philips Semiconductor, "I2C Bus Specification" version 2.1, January 2000.
[4] ArvindSahu,Ravi Shankar Mishra,PuranGour, "Design and Interfacing of High speed model of FPGA using I2C protocol," Int. J. Comp. Tech. Appl., Vol 2 (3), 531-536.
[5] Trupti D. Shingare, R. T. Patil, "SPI Implementation on FPGA," International Journal of Innovative Technology and Exploring Engineering (IJITEE), Volume-2, Issue-2, January 2013.
[6] Pankaj Kumar Mehto, PragyaMishra ,SonuLal, "Design and Implementation for Interfacing Two Integrated Device Using I2C Bus, " International Journal of Innovative Research in Computer and Communication Engineering, Vol. 2, Issue 3, March 2013.
[7] J. J Patel, B. H. Soni, "Design and Implementation of I2c Bus Controller Using Verilog," Journal of Data, Knowledge and Research in Electronics and Communication Engineering Nov 12 To Oct 13, Vol. 02, Issue – 02, page no. 520-522.
[8] Philips Semiconductor, "I2C Manual" March 24, 2003
[9] Philips I2C specifications
http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf
[10] A VHDL Primer, J. Bhasker, Prentice Hall.
[11] Data sheet for the Maxim DS3232 real-time clock,
http://datasheets.maxim-ic.com/en/ds/DS3232.pdf
[12] Perry D., "VHDL," 3rd Edition, Tata McGraw Hill Publications, 2001.
[13] J. Bhasker, "Verilog HDL Primer," BSP Publishers, 2003.
[14] "VHDL Reference Manual", IEEE standard, 1993
[15] http://www.xilinx.com/products/design-tools/ise-design-suite/ise-webpack.html