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A Hardware Efficient Fast Sign Detection Algorithm for RNS Moduli Set

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ABSTRACT: The Residue Number System (RNS) is a non-weighted system that is very efficient in digit a signal processing and communicational applications. Here fast sign detection algorithm for RNS special moduli set introduced . The special moduli set is $\{2^{n+1}-1, 2^n-1, 2^n\}$, this moduli set based algorithm used. This unit of implementation contains CSA, comparator unit, carry generation unit and post processing unit. The experimental gives the proposed unit minimizes area and delay in case RNS sign detection using pipelined architecture.

KEYWORDS*:* Residue Number System (RNS),Chinese Reminder Theorem (CRT),Moduli Set $\{2^{n+1}-1, 2^n-1,2^n\}$.

I. INTRODUCTION

Residue Number System is an unconventional system. In this system, an integer X is represented by its reminder modulo a number of different bases. The Residue Number System (*RNS*) is a non-positional number system that has been invented in order to decompose certain operations on large integers into sets of operations on small numbers. The simplicity of such *RNS* operations as addition, subtraction and multiplication is offset by the difficult realization of scaling, division, sign detection, magnitude comparison and overflow detection. Hence the *RNS* can be advantageous for the realization of these algorithms where the operations of the first group dominate. To such algorithms belong those of the digital signal processing such as the Finite Impulse Response (*FIR*) and the Fast Fourier Transform (*FFT*).

Here examining sign of the residue number system. This sign detection problem has been investigated by many researchers, and derived general theorem for sign detection of RNS[2]. Selected class of sign detection carried as a sum modulo 2of digits in associated mixed radix system(MRS) in [3] .The modulo operations of sign detection bounded by size $\sqrt{M}$. Here sign detection algorithm is presented for restricted moduli set $\{2^{n+1}-1,2^n-1,2^n\}$.

First sign algorithm for only modulo 2^n in the RNS. Our new sign detection consist of carry save adder, comparator and carry generation unit. The new chinese reminder theorem used to sign detected here[5].This algorithm uses nth mixed radix conversion (MRC) for sign detection[6].This sign detection method only applicable for moduli set, $\{2^{n+1}-1,2^n-1,2^n\}$.

The proposed method sign detection better than on area and delay by comparing existing methods .Section II describes existing method of sign detection. Section III describes the proposed method sign detection, and section IV describes performance evaluation.

II. RELATED WORK

The standard RNS case positive integers in the range [0,M).Implicit signed number system split positive half of range and negative half of the range.

A. RNS representation

An RNS is defined by a set of relatively prime integers called the *moduli*. The moduli-set is denoted as $\{m_1,m_2,...m_n\}$ where m_i is the i^{th}modulus. Each integer X can be represented as a set of smaller integers called the

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residues. The residue-set is denoted as { $r_1,r_2....r_n$}where $r_i$is the i^{th}residue. The residue r_i is defined as the least positive remainder when X is divided by the modulus m_i. This relation can be notationally written based on the congruence:

$$X \bmod m_i = r_i \quad (1)$$

The same congruence can be written in an alternative notation as:

$$|X|_{mi} = r_i \quad (2)$$

The RNS is capable of uniquely representing all integers that lie in its *dynamic range*. The dynamic range is determined by the moduli-set { $m_1,m_2...m_n$} and denoted as M where:

$$M=\prod_{i=1}^{n} mi \quad (3)$$

The RNS provides unique representation for all integers in the range between 0 and M-1 . If the integer X is greater than M-1 , the RNS representation repeats itself. Therefore, more thanone integer might have the same residue representation. It is important to emphasize that the moduli have to be relatively prime to be able to exploit the full dynamic range . Converting from residue to weighted number, X in the interval [0,M/2) carries implicit representation of the sign of the actual result Y,

$$Y = \begin{cases} X, if\ 0 \le X \frac{M}{2} \\ X - m, if \frac{M}{2} \le X < M \end{cases} \quad (4)$$

Theorem I: Given { m1, m2, ….., mn}, the magnitude of the residue number x = (x1,x2,…..,Xn) is calculated as follows:

$$X = \sum_{j=1}^{N-2}(\alpha_{j+1}\prod_{i=1}^{j+1} mi)_{+}\alpha 1m1 + \alpha 0 \quad (5)$$

Whereα_{j+1}=$|(\sum_{i=1}^{j+2}\gamma ixi / \prod_{i=2}^{j+1} mi)|m_{j+2}$, $\alpha 1 = |\gamma 1x1 + \gamma 2x2|m2, \alpha 0 = x1, N1, \gamma 1 = (N_1 |N_1^{-1}|m_1 -1 /m_1$, γ_i = M $|N_i^{-1}| m_i/m_1m_i$, M = m_1m_2…. M_N, N_i = M/ m_i, and the multiplicative inverse $|N_i^{-1}|_{mi}$ defined by $|\,|N_i^{-1}|_{mi} N_i|_{mi}$ =1, for i = 1, 2, 3,……., N. Above theorem provides ,Here modulo m_i operation only required for convert residue to weighted numbers .Fully parallel manner mixed radix coefficients calculated.

Theorem II : For the moduli set {*m1 , m2, ……, m_N =2^n}*, the value of $\alpha_{N-1}$is equal to $2^{n-1}$when the integer *X* is *M*/2, α_{N-1} (M/2) is denoted as the value of α_{N-1} for X = M/2 and it has

$$\alpha_{N-1}\ (M/2) = 2^{n-1} \quad (6)$$

Theorem III: :In the moduli set {m_1, m_2,m_3……., m_{N-1}, m_N= 2^n} ,fora residue representative number (x_1 , x_2, ….., x_N) , α_{N-1}*is*

$$\propto_{N-1} = \left\| \frac{\gamma 1x1+\gamma 2x2+\cdots+\gamma NxN}{m2m3\ldots mN-1} \right\|_{2^n} \quad (7)$$

B. Sign detection for the moduli set {2^{n+1}-1,2^n-1, 2^n}

Here presenting new sign detection method for above moduli set.This sign detection method suitable for VLSI implementation and is concurrent.

Theorem IV: For the moduli set {2^{n+1}- 1, 2^n- 1, 2^n}, the signdetection of *X* = (x_1, x_2,x_3) is

$$Sgn(x1,x2,x3) = MSB(\left\| -2X1 + X2 + X3 + \frac{X2-X1}{2^n-1} \right\| 2^n \quad (8)$$

$$\propto_2 = |-2x1 + x2 + x3 - x1, n - \bar{w}|2^n$$

$$=|2^n - 1 - x1'' + x2 + x3 + 1 - \bar{w}|2^n$$

$$= |\overline{x1''} + x2 + x3 + W|2^n \quad (9)$$

x1,x2,and x3 arepowers of n+1th , n-1th and nth bits.Here denoted x1,n as aleast n bits of x1. Becouse the word x1is with one more bit than x2. For circuit design rewrite equation as

$$\left\| \frac{x2-x1}{2^n-1} \right\|_{2^n} = -x1,n - \bar{w} \quad (10)$$

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W bar is ones complement of *W*.

$$W = 1-\overline{W} = 1+\left\lfloor \frac{X2-X1'-X1,N}{2^n-1} \right\rfloor \quad (11)$$

This equation based main architecture works,main architecture of sign detection unit shown on fig.1

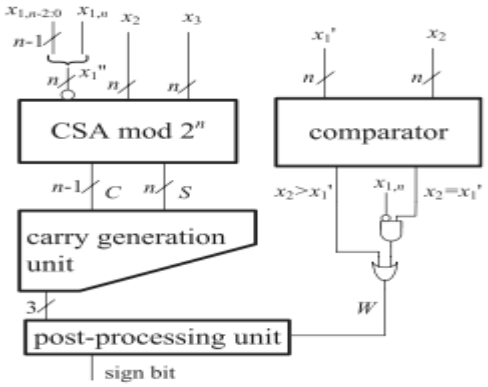

Fig .1. Sign detection unit for moduli set $\{2^{n+1}-1, 2^n-1, 2^n\}$.

In fig .1. the CSA mod 2^nused to produce the sum of x1''+x2+x3. The outputs of CSA is Sum and carry that represented as S and C.The carry generation unit and post processing unit shown below.The goal of carry generation unit and post processing is to develop nth bit of $\alpha_2 = C + S + W$.

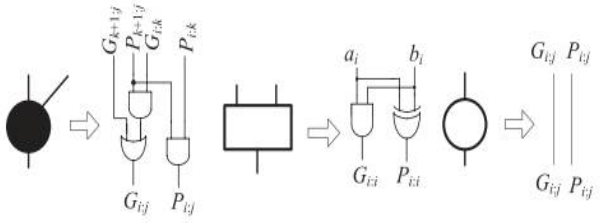

Fig.2. Blocks of carry generation unit and post processing unit.

The comparator unit used to compare x2>x1' and x2 = x1'.Here n=16 based operation performed.

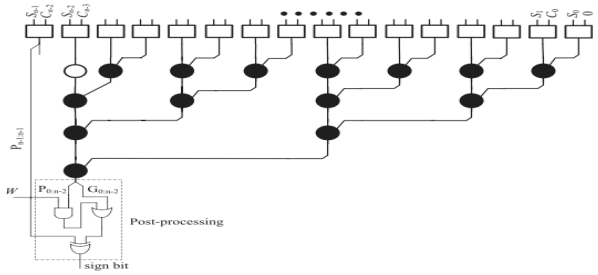

Fig.3. carry generation unit and post processing unit n=16

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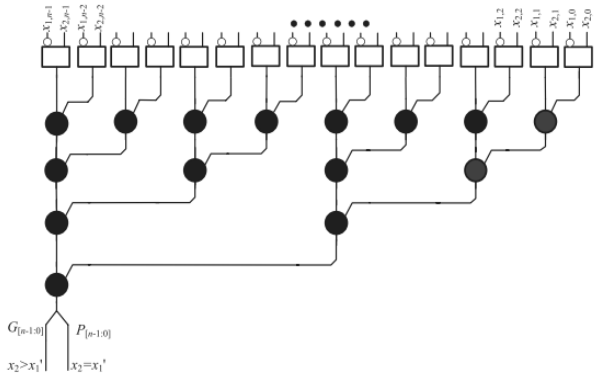

Fig.4. comparator unit n=16

III. PROPOSED SIGN DETECTION UNIT BASED ON PIPELINED ARCHITECTURE

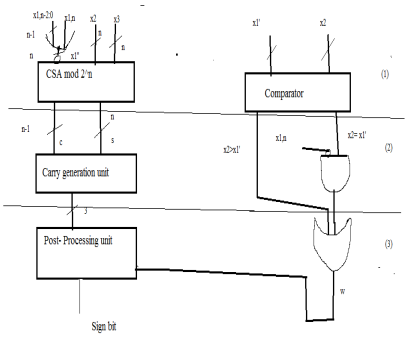

Fig.5. pipelined sign detection unit.

Proposed sign detection unit introduce pipelined architecture, in this way delay reduced and fast sign detection possible. The pipelined architecture introduced way area minimized. In pipelined situation mainly divided into three stages , for example CSA and comparator works at a time. Earlier situation comparator and CSA are works two distant instants. Next instant carry generation unit and AND gate operation done. At last post processing unit and OR gate works. In this way area and delay minimized way sign detected. Commonly pipelined case all stages synchronized under common clock control. Interface latches are used between adjacent segments to hold the intermediate results. Fig.5. shows the pipelined operation of the sign detection unit, figure clearly divides the earlier system into three regions.

IV.PERFORMANCE EVALUATION

In this section ,the performance of proposed sign detection unit with earlier sign detection unit evaluated. Here sign detection unit compared based two parameters based, area and delay.

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Table I
Area And Delay Comparison For Earlier And Proposed Sign Detection Unit

	Area(no. of slices)	Delay(ns)
Proposed sign detection unit	42	16.49
Earlier sign detection unit	44	14.075

Above table clearly shows comparison between earlier sign detection and proposed method.

V. CONCLUSION

In brief, here presenting fast sign detection algorithm for moduli set $\{2^{n+1}-1,2^n-1,2^n\}$.Our proposed technique is based on pipelined architecture introduced into earlier method. Based on proposed method at a time two blocks are executed. our architecture used to significant reduction in delay and area, compared to conventional methods. In this way significant improvements of sign detection of RNS is possible.

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BIOGRAPHY

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