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FPGA Implementation of Optimized Decimation Filter for Wireless Communication Receivers

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ABSTRACT: Digital down converter (DDC) is very important and integral part of the multi-rate wireless communication system. As it utilizes the major resources, therefore its low cost and efficient implementation is of main concern. This paper presents and implements a FPGA based optimized design of decimation filter for wireless communication receivers. Cascaded integrated comb (CIC) filters are multiplier less linear filters which are extensively used in multi-rate systems for the purpose of digital down conversion (DDC). An optimized architecture based upon these filters is analyzed and implemented. The prototype of the proposed filter is designed to decimate the input signal having sampling rate 10 MHz, by the decimation factor of 8 using Matlab-Simulink Model and Xilinx System Generator. The design is implemented on Vertex-5 based xc5vlx110t-3-ff1136 target device. The proposed design consumed considerably less resources on the target device to provide an efficient design for multi-rate wireless communication receivers.

KEYWORDS: Digital filters; DDC; digital down converter; CIC; decimation filter; multi-rate communication system; decimator; cascaded integrated comb; Non-recursive filter; Matlab Simulink; Xilinx System Generator

I. INTRODUCTION

Due to widespread use of digital representation of signals, digital communication has become more popular for transmission and reception. The multi-rate digital signal processing can be found everywhere in modem digital communication products. Interpolators and decimators are used to increase or decrease the sampling rate of the signal in multi-rate systems. The sampling rate conversion leads to the generation of aliasing and imaging errors [1]. Therefore there is need of a filter that should be placed to attenuate these errors.

For every wireless communication receiver, high speed, lower power consumption, lower resource utilization and lower circuit complexity are main design targets as they reduce the cost. Also the development cost and time-to-market factors associated with the design cannot be neglected. In this context, DSP processors are unable to meet desired performance due to their sequential-execution architecture [2] but FPGA's are very good solution to the problem as they provide balance of high flexibility, high speed, less time-to-market, low cost and better performance. The implementation of the proposed digital decimation filter is based on the efficient utilization of resources of FPGA which not only increases the speed but also improves the overall performance of the design.

II. RELATED WORK

The Cascaded Integrator Comb (CIC) filter was proposed by Hogenauer [3]. It a class of digital filters without multipliers for interpolation/decimation and uses only additions/subtractions which lead to better economical hardware. The filter is called CIC filter, as it consists of an equal number of integrator sections operating at the high sampling rate and a comb section operating at the low sampling rate as compared to Integrator section. In past few years various techniques has been proposed by many researchers [4]-[10] to design CIC (Cascaded-integrator comb) decimation filter and its design has been modified to provide improvements in power consumption, economical hardware and frequency response [4]-[10]. M. Madheswaran and V. Jayaprakasan [11] have presented the comparison of various efficient CIC filter structures for a decimation factor of 8 and concluded that Non-Recursive CIC filter Structure is best among all. V Elamaran [12] has presented efficient implementation of conventional CIC structure. In this paper the authors presents an optimized design of Non-Recursive CIC filter structure, achieving better performance in terms of hardware utilization than the CIC filter structures presented by [11] and [12].

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CIC decimation filter: Hogenauer [3] introduced the CIC filter structure for economical design of decimation and interpolation filters. This class of filters requires neither multipliers nor storage elements to store filter coefficients and therefore uses less resources than a corresponding FIR filter. The basic building blocks of a CIC filter are an integrator and a comb section. An integrator is simply a single-pole IIR filter with a unity feedback coefficient.

$$y(n) = y(n-1) + x(n) \tag{1}$$

The transfer function of the integrator in the z-plane is given by

$$H_1(z) = \frac{1}{1-z^{-1}} \tag{2}$$

The power response of integrator is a low-pass filter with a -20 dB per decade but with infinite gain at DC [13] due to the single pole at z = 1; the output can grow without bound for a bounded input. In other words we can say that a single integrator by itself is unstable and its basic structure is shown in Fig. 1.

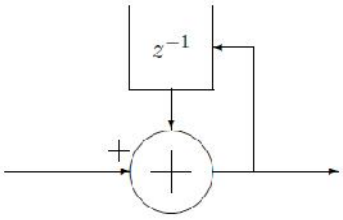

Fig. 1. Basic Integrator

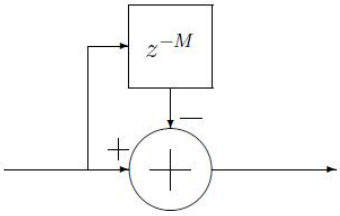

Fig. 2. Basic Comb

A comb filter running at the high sampling rate, f_s, for a rate change of R is an odd symmetric FIR filter described by

$$y(n) = x(n) - x(n-RM) \tag{3}$$

In this equation, M is a design parameter and is called the differential delay. M can be any positive integer, but it is usually limited to 1 or 2. The corresponding transfer function at f_s is given by

$$H_C(z) = 1 - z^{-RM} \tag{4}$$

When R = 1 and M = 1, the power response of comb is a high-pass function with 20 dB per decade gain (as it is the inverse of an integrator) [13]. The basic structure of comb is shown in Fig. 2. When a CIC filter is designed, we cascade N integrator sections and N comb sections together through a rate changer. So, a CIC decimation filter would have N cascaded integrator stages clocked at f_s, followed by a rate changer by a factor of R, followed by N cascaded comb stages running at f_s/R. The transfer function of the filter at f_s is given by

$$H(z) = H_I^N(z)H_C^N(z) = \frac{(1-z^{-RM})^N}{(1-z^{-1})^N} \tag{5}$$

The structure of CIC decimation filter is shown in Fig. 3.

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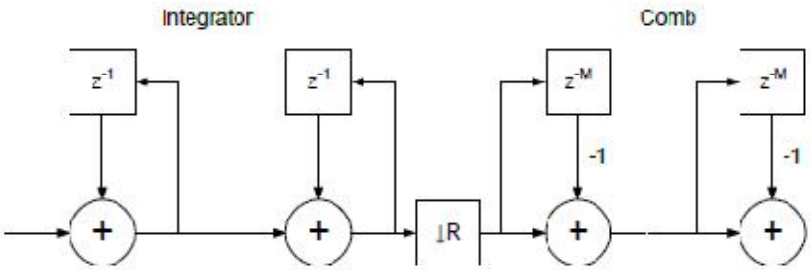

Fig. 3. CIC decimation filter

III. PROPOSED DECIMATION FILTER

An efficient solution for optimizing and the CIC decimation filter is non-recursive decimation filter. The structure of non-recursive decimation filter is based upon conventional CIC decimation filter [14]. The transfer function of conventional CIC filter is given by

$$H(z) = \frac{(1-Z^{-RM})^N}{(1-Z^{-1})^N} \tag{6}$$

If the value of differential delay (M) is one. The transfer function can be represented as

$$H(z) = \frac{(1-Z^{-R})^N}{(1-Z^{-1})^N} = \left[\frac{(1-Z^{-R})}{(1-Z^{-1})}\right]^N \tag{7}$$

The eq. 7 can also be represented as

$$H(z) = [1 + Z^{-1} + Z^{-2} + Z^{-3} + \cdots + Z^{-R+1}]^N \tag{8}$$

If the decimation factor (R) is represented as power of 2 then by using polynomial factoring the transfer function given in eq. 8 can be represented as

$$H(z) = (1 + Z^{-1})^N (1 + Z^{-2})^N (1 + Z^{-4})^N \ldots\ldots (1 + Z^{-2(k-1)})^N \tag{9}$$

Here decimation factor (R) is represented as Kth power 2 and the corresponding non recursive decimation structure is represented in Fig. 4.

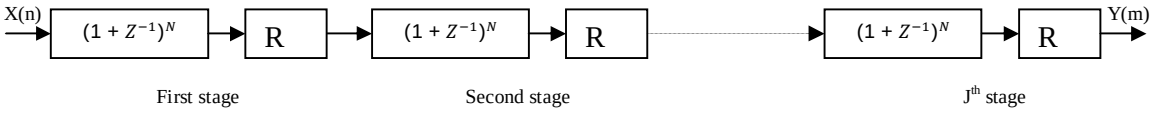

Fig. 4. Non-recursive decimation filter

The improvements provided by proposed non-recursive decimation structure over conventional cascaded integrator comb structure are listed below.

- As integrator is missing in non-recursive filter, bit growth occurs only at the rate of N bits per stage but in cascaded integrator comb filter due to the integrator section bit growth occurs at the rate of more than N bits per stage [14].
- Due to absence of integrator in non-recursive filter, the resource utilization is minimized by a significant factor.
- As it uses lesser number of resources, the power consumption of the filter is also minimized.
- Due to the lesser resource utilization, the speed of the filter is increased.

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IV. IMPLEMENTATION, SIMULATION RESULTS AND COMPARISON

The proposed architecture shown in Fig. 4 is implemented on Vertex-5 based xc5vlx110t-3-ff1136 target device using Matlab Simulink model and Xilinx System Generator. The filter is designed to decimate with a decimation factor R=8 and is implemented in 3 stages. The input signal having a sampling rate of 10MHz is down sampled by filter to the signal having a sampling rate 1.25MHz for pass band of 78.150 KHz. The single stage implementation of purposed filter and complete 3-stage design is shown in Fig. 5 and in Fig. 6 respectively.

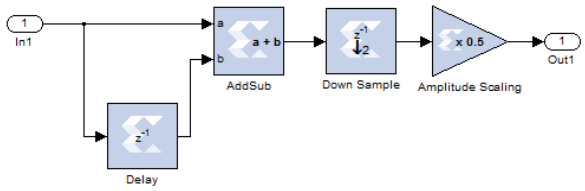

Fig. 5. Single stage implementation of purposed filter

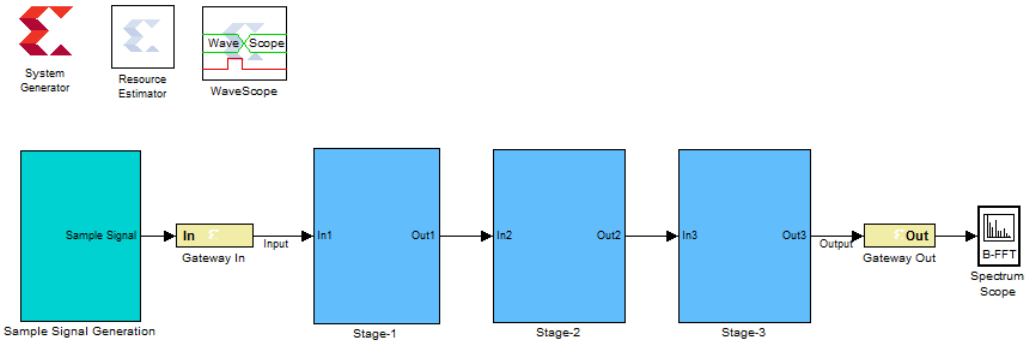

Fig. 6. Complete 3-stage structure of purposed filter

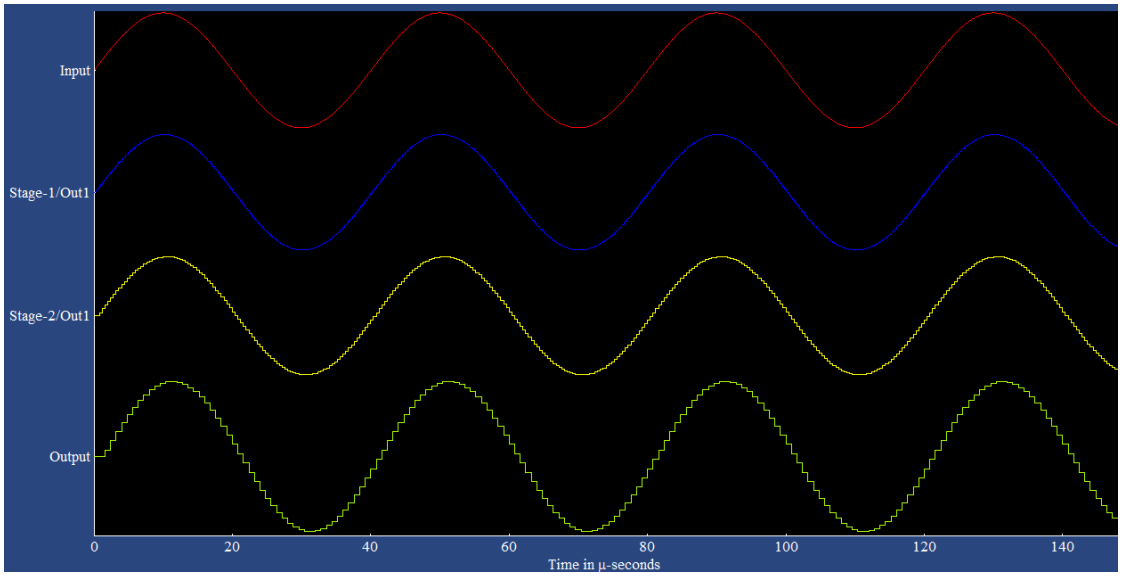

Fig. 7. Simulation results of purposed filter structure

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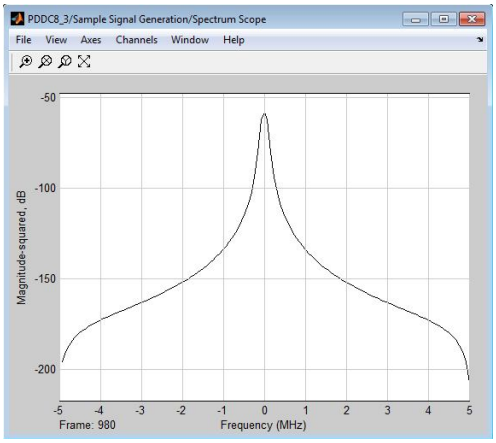

Fig. 8. Spectrum of input signal

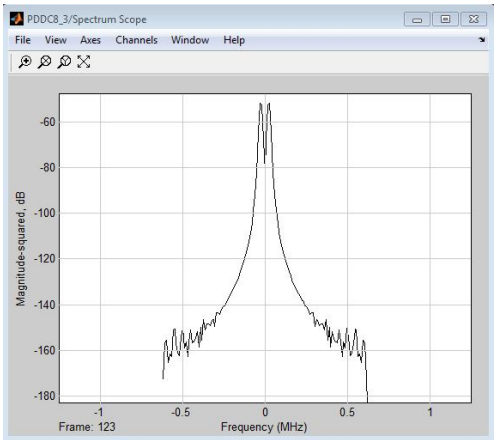

Fig. 9. Spectrun of decimated output signal

The simulation results, showing input, output of each stage and final output is shown in Fig. 7. The spectrum of input signal as well as decimated output signal is shown in Fig. 8 and Fig. 9 respectively which validates our purposed design. Table 1. shows the comparison of resource utilization of proposed structure with the existing similar structures proposed for decimation factor of 8 by M. Madheswaran and V. Jayaprakasan [11] and V Elamaran [12].

Resource utilization	Non-recursive[11]	Conventional CIC[12]	Proposed Non-recursive
Number of Slice Registers	133	133	136
Number of Slice LUTs	102	171	8
Number of LUT Flip Flop pairs used	152	114	8
Number of bonded IOBs	33	68	33
Number of BUFG/BUFGCTRLs:	---	1	1

Table 1. Comparison of resource utilization with existing structures

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V. CONCLUSION AND FUTURE WORK

The proposed architecture is designed and implemented on Vertex-5 based xc5vlx110t-3-ff1136 target device. The simulation results validate the implemented design. Table 1 show that the proposed design of the filter consumed considerably less resources on the target device as compared to the existing designs for the same decimation factor and provides an efficient design for multi-rate wireless communication receivers. As the performance of the proposed is better, in future the proposed design can be extended as per the specifications of 4G, WiMax and other modern wireless communication systems.

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BIOGRAPHY

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