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Reconfigurable Low Area Complexity Filter Bank Architecture Based on Frequency Response Masking For Software Defined Radio

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ABSTRACT: The high and constantly increasing demand to develop radio transceivers with enhanced functionalities, inter-standard portability, higher throughputs, compact physical size, low cost, and longer battery lifetime impose challenges on the radio designer. A Software Defined Radio is capable of meeting these challenges provided (i) enhanced signal processing algorithms with reduced complexities, (ii) high performance HW/SW platforms, and (iii) the optimized architectural design that finally maps the algorithms to the processing platform.

KEYWORDS; Reconfigurability, Low complexity, Digital filter banks, Software Defined Radio (SDR), Channelizer, reconfigurable architecture, Lookup Table (LUT)

I. INTRODUCTION

Software radios can significantly reduce the cost and complexity of today's cellular radio base stations. Software radios architectures centre on the use of wide band (WB) A/D converters and D/A converters as close to the antenna as possible, with as much radio functionality as possible implemented in the digital domain.The reconfigurable FIR filters are widely used in multiband mobile communication system. The filters using in mobile communication system must be operating in low frequency and realize to consumes less power and high speed. The advance technologies in mobile communication systems are demanding the low power and low complexity techniques. The Software Defined Radio (SDR) and the FIR filter researches are focused on reconfigurable realizations [2]. The SDR technology used to replace the analog signal processing with digital signal processing in order to provide flexible reconfiguration. A SDR design must meet today's reconfigurability requirements and adapt to emerging standards, as well as accommodate cost, power and performance demands. Reconfigurability of the receiver to work with different wireless communication standards is another key requirement in an SDR. Generally the complexity of FIR filter depends upon the number of adders performs in the multiplier unit. Chanalizer is known as the most important block of the SDR which operates in high sampling rate but the SDR must be realizing of low power consumption and high speed. Using a bank of FIR filters in the channel filters introduces the multiple numbers of narrowband channels from a wideband signal.

II. LITERATURE REVIEW

The PC approach is a straightforward approach and hence relatively simple. But the main drawback is that, the number of branches of filtering-DDC-SRC is directly proportional to the number of received channels i, e. The complexity of the PC approach is directly proportional to the number of channels. Hence the PC approach is not efficient when the number of received channels is large. The filters used in the PC approach are of a very high order and this results in high area complexity and thus increased static power. DFTFBs cannot extract channels with different bandwidths known as nonuniform channels, because they are modulated FBs with equal bandwidth forall bandpass filters–the bandwidths are same as that of the prototype LPF. Therefore, for multi-mode receivers, distinct DFTFBs are required for each communication standard. Hence the complexity the channelizer increases linearly with the number of

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standards. If the channel bandwidth is very small compared with wideband input signal (extremely narrowband channels), the prototype filter must behighly selective resulting in a very high-order filter.As the order of the filter increases, the complexity

increases linearly. Also the DFT size needs to be increased. Pucker, L. in paper [2] entitled "Channelization techniques for software defined radio" proposed DFT Filter Banks. DFT filter bank is a uniformly modulated filter bank, which has been developed as an efficient substitute for PC approach when the number of channels need to be extracted is more, and the channels are of uniform bandwidth (for example many single standard communication channels need to be extracted). The main advantage of DFT filter bank is that, it can efficiently utilize the polyphase decomposition of filters. The limitations of DFTFBs is that the channel filters have fixed equal bandwidths corresponding to the specification of a given standard.R. MAHESH et.al. in paper [3] entitled "Reconfigurable Low Area Complexity Filter Bank Architecture Based on Frequency Response Masking for Non uniform Channelization in Software Radio Receivers" proposed a new reconfigurable FB based on the FRM approach for extracting multiple channels of non uniform bandwidths. The FRM approach is modified to achieve following advantages: 1) incorporate reconfigurability at the filter level and architectural level, 2) improve the speed of filtering operation, and 3) reduce the complexity.

III. FRM-BASED FILTER BANK ARCHITECTURE

Filter reconfigurability means changing the coefficients of each filter in Fig. 1 according to the specifications of the new standard. It is well known that one of the efficient ways to reduce the complexity of multiplication operation is to realize it using shift and add operations [3]. In contrast to conventional shift and add units used in previously proposed reconfigurable filter architectures, a binary common sub expressions (BCSs) based shift and add unit has been employed in the filter architectures. The existing architecture of the filter for an 8-bit coefficient is shown in Fig. 3. M1 and M2 are 8 : 1 multiplexers; M3 is a 4 : 1 multiplexer and M4 and M5 are 2 : 1 multiplexers.

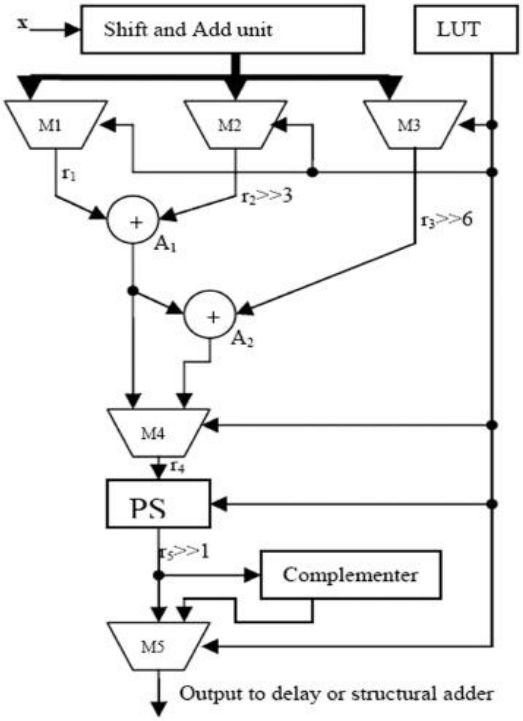

Fig.1 FRM based filter bank architecture

The input is given to the shift and add unit whose output is shared among the multiplexers. The filter coefficients are stored in the LUT in a coded format SDDDDXXXXXXXX, where S is the sign bit, DDDD is the shift value of the

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most significant non-zero bit in the coefficient, and X represents the bit values after the coefficients are shifted left so that the most significant bit (MSB) to the right of the decimal point (position value corresponding is always "1." Each row in the LUT corresponds to one coefficient. The MSB of the modified coefficient S stored in the LUT is given as the select signal to the multiplexer (MUX), M5.The MUX M5 determines whether to complement the output or not depending on the sign bit of the coefficient. The values DDDD form the select signal to the programmable shifter (PS) which will perform the shifting . The least significant 2 bits form the select signal to M4. The values r1,r2,r3 and r4 correspond to the outputs of multiplexers M1,M2,M3, and M4 respectively. The reconfigurability can be achieved by changing the coefficients in the LUT[3].

IV. PROPOSED SYSTEM OVERVIEW

It is well known that one of the efficient ways to reduce the complexity of multiplication operation is to realize it using shift and add operations. In contrast to conventional shift and add units are used in previously proposed reconfigurable filter architectures. A *programmable shifter* is more complex. Often the speed of multiplication *limits* the performance of the digital processor. So, we can use barrel shifter (a circuit that shifts multiple bits at a time) in proposed architecture instead of programmable shifter. The time required/delay will considerably improve by doing this and the proposed architecture is modified for reducing its complexity.

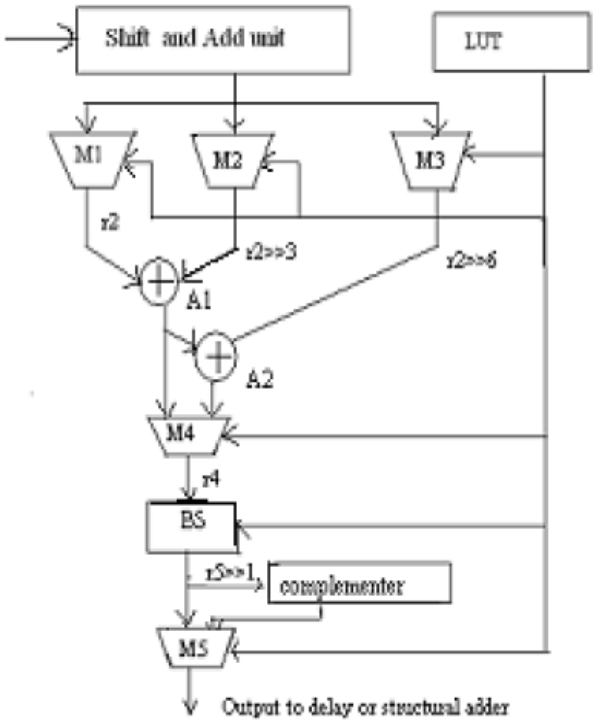

Fig.2 Proposed reconfigurable filter architecture

Barrel shifters have the ability to shift data words in a single operation over standard shift left or shift right registers that utilize more than one clock cycle. Barrel shifters will continue to be used in smaller devices because it has a speed advantage over software implemented ones. In general, it can be concluded that a barrel-shifter is appropriate for smaller shifters. For large shift values, the log shifter becomes more effective, in terms of area and speed. Also log shifter is more regular and hence can be easily generated automatically.In reconfigurable FIR filter architectures based on a binary sub-expression elimination (BSE) algorithm has been proposed. The architecture is consisted of a shift and add unit which will generate all the 3-bit BCSs using 3 adders. The proposed architecture of the filter for an 8-bit

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coefficient is shown in figure.4. M1 and M2 are 8:1 multiplexers; M3 is a 4 : 1 multiplexer and M4 and M5 are 2 : 1 multiplexers. The input is given to the shift and add unit whose output is shared among the multiplexers.

V. RESULTS & CONCLUSION

In this section, the synthesis results of the FRM FB, and modified FB architectures are presented and parameters like area and delay are compared. The comparison table states the architecture which has high speed and minimum delay. The Xilinx 9.1i ISE Virtex-II used for synthesizing purposes.

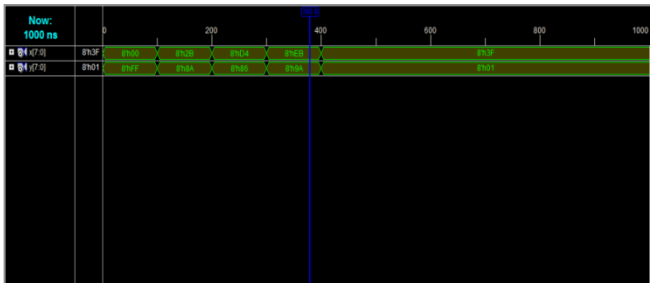

Table 1: The delay Comparison between the Existing and Proposed Method

Parameter	Existing Method From ref.3	Proposed Method
Delay(ns)	38.67	13.65

Graph 1: Delay comparison

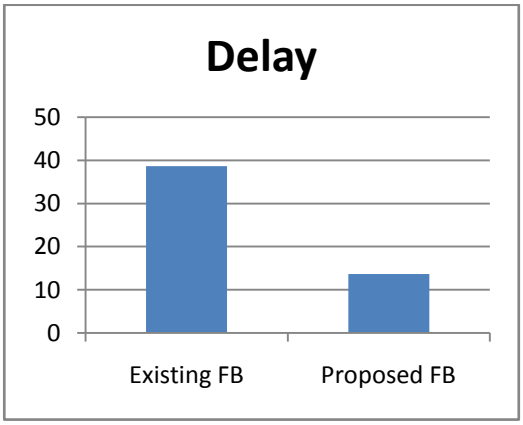

Table 2: The frequency Comparison between the Existing and Proposed Method

Parameter	Existing Method From ref.3	Proposed Method
Frequency ofoperation(speed MHz)	24	73.26

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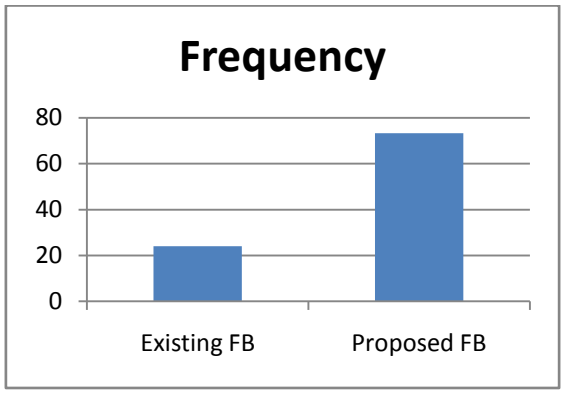
Graph 2: frequency comparison

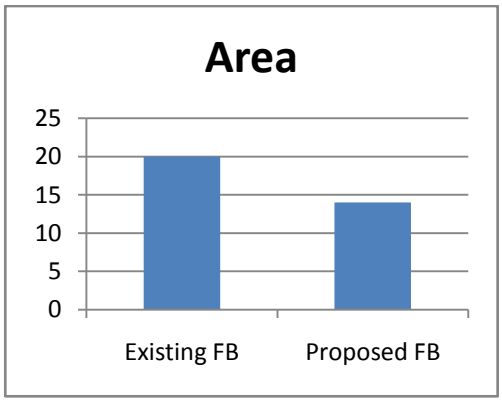


The comparison table states the architecture which has less area. The Xilinx 9.1i ISE spartan-III used for synthesizing purposes.

Table 3: The area Comparison between the Existing and Proposed Method

Parameter	From reference.4	Proposed Method
Area(slices)	20	14

Graph 3: Area comparison



VI. CONCLUSION

The proposed reconfigurable filters architecture results in low area and low delay. The FRM reconfigurable technique is modified to improve the speed and reduce the complexity. Synthesis results show that the proposed FB offers area reduction.

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