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# A Review: Design and Analysis of Multi-Valued Logic for Quaternary Combinational Circuits

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**ABSTRACT***:* The project presents the design of high performance quaternary Combinational circuits for lower power dissipation. Most of the digital electronic systems are based on the binary logic design which is limited by the requirement of interconnections which increases the chip area. The solution to this problem can be achieved using multi valued logic (MVL)/Quaternary logic. Most of the authors used methods which required Quaternary to Binary and Binary to Quaternary conversion for any arithmetic and logic operation and achieved satisfactory performances. Our aim is to develop MVL/Quaternary logic for combinational circuits under case study without converting these levels into binary logic and vice-versa. It will reduce one additional step, and improve the performance offering less chip size, saving more power. The design is targeted for 0.18um CMOS technology and the design tool for simulation will be Advanced Design System tool (ADS).

**KEYWORDS***:* Multi valued logic(MVL), Quaternary logic, Advanced Design System (ADS),Quaternary Half Adder (QHA)

## I. INTRODUCTION

Current digital electronics technologies are mainly based upon binary systems which require number of interconnections. These interconnections can be reduced when data is represented in multi valued logic system as it is effective than binary demonstration.

Multiple value logic are logical calculi in which there are more than two possible truth value. Logical calculi are bivalent. There are only two possible values for any proposition true and false. Lukasiewiczs was first author who proposed two value and three value logic. i.e (True, false and unknown). But MVL or quaternary logic is the new technology up growing in VLSI. Increased data density, reduced dynamic power dissipation, and increased computational ability are among some of the key benefits of Multiple Valued Logic (MVL). Several implementation methods have been proposed in the recent papers to realize the MVL circuits. They can fundamentally be categorized as current-mode, voltage-mode and mixed-mode circuits current-mode circuits have been popular and offer several benefits, the power consumption is high due to their inherent nature of constant current flow during the operation.
Alternatively, voltage-mode circuits consume a large majority of power only during the logic level switching. Hence, voltage-mode circuits do offer lesser power consumption which has been the key benefit of traditional CMOS binary logic circuits from the perspective of dynamic switching activity. Several approaches for quaternary circuit design have been proposed, in voltage mode technique.

Multi valued logic is defined as a non binary logic and involves the switching between more than two states. Multi valued logic offers important advantage like more information can be processed over a given set of lines to reduce the burden of interconnections and thereby switching. The advantage of multi valued logic are the use of fewer operations potentially fewer gates and reduction in number of interconnections & switching. The reduction of dynamic power dissipation is VLSI applications is the major challenge for today's engineers as major portion of the power is consumed by interconnect and switching.

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Quaternary logic (radix-4-valued) is chosen as the base radix for the work. This includes number 0,1,2,3. Using quaternary radix offers all the benefits of MVL such as reduced area due to signal routing reduction along with the important advantage of being able to easily interfere with traditional binary logic circuits.
Adders are the basic part of processing element. An adder is basically a circuit which is used in variety of applications. So, if we create an optimized adder simultaneously the processing elements will be improved. This will fasten the calculation of arithmetic and logic unit which further improves and fasten the performance of the unit. Using a optimized adder using quaternary logic will lessen the space required. These optimized adders will prove to be useful in other Digital Signal Processing as adders are the basic part of Digital Signal Processing.

## II. LITERATURE REVIEW

Novel quaternary half adder, full adder, and a carry-look ahead adder were introduced by M Thoidis. In his paper, the proposed circuits were static and operate in voltage mode. They reported no static power dissipation as the circuits were static in nature.

1] Vasundara Patel , K S Gurumurthy
"Arithmetic operations in multi-valued logic". Author presents arithmetic operations like addition, subtraction and multiplications in Modulo-4 arithmetic, and also addition, multiplication in Galois field, using multi-valued logic (MVL). Author used Hspice as tool for simulation, and Q-B conversion, B-Q conversion for implementation the arithmetic operation, for minimization of logic Karnaugh diagrams are being used.
From this paper we found that, Circuits for Modulo-4 addition, multiplication and subtraction require only 4 gates. Galois addition requires two XOR gates which is most optimized one while implementing the circuit in VLSI. With the help of quaternary logic, they have reduced the interconnections, used less number of gates due to which less area is required for Galois and modulo-4 arithmetic operations.

2] Bob Radanovic, Marek Syrzycki
"Current-Mode CMOS Adders Using Multiple-Valued Logic". Author presented the adder cell for radix 2 algorithm, using PD(Positive Digit) representation , they used two technology 0.8um CMOS and 1.5um CMOS , with step current of 12uA and 1uA respectively. They also address the design of 4 digit decimal adder with 10 step of current.
We found two major issues in efficient design of CMMV circuits are the numerical representation of numbers and the unit current step per logic level. A (PD) represent positive currents to encode the numbers, but increases circuit complexity. Proper choice of multiple value algorithm and current levels can potentially result in very high speed operation and low power supply which is very attractive in VLSI chip.

3] Ricardo Cunha, Henri Boudinov and Luigi Carro
"Quaternary Look-up Tables Using Voltage-Mode CMOS Logic Design". Author presented a new way to implement quaternary look-up tables using a multiplexer circuit to implement any quaternary logic function based on its truth table. Result has been compared with binary. Simulation has been carried out in Spice tool using TSMC 0.18 µm.
We found that by using voltage mode CMOS logic design in quaternary look up table gives high performance with negligible static and dynamic power consumption with less power dissipation and less number of transistors as compared to current mode CM MVL. But circuit complexity increases due to multiplexer.

4] Hirokatsu Shirahama and Takahiro Hanyu
"Design of High-Performance Quaternary Adders Based on Output-Generator Sharing". Author presented simple implementation of quaternary full adders which are proposed for a high-performance multi-processor system which consists of many processing elements (PEs). The result shows the delay of the proposed CM implementation reduced to 70% and the delay and power dissipation of the proposed VM implementation are reduced to 73% and 79%, respectively.
The use of appropriate input-value conversion makes it possible to reduce the number of output generators, which enables to implement high performance quaternary full adders.

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5] Anindya Das1, Ifat Jahangir2 and Masud Hasan
"Design of Quaternary Serial and Parallel Adders". Author presented the design of a logarithmic stage parallel adder which can compute the carries within log2(n) time delay for n value computing. Author compares the gate delays of full adder and logarithmic stage parallel using mathematical expressions.
We found that linearly increasing gate delay is the main disadvantage of ripple carry adder. So they have proposed logarithmic stage carry look-ahead adder which works within log2(n) gate-delay for n quaternary digits and have limited number of fan-in.

6] Y. Yasuda, Y. Tokuda, S. Zhaima, K. Pak, T. Nakamura A. Yoshida.
"Realization of quaternary logic circuits by n-channel mos devices". Author presented the new method for quaternary circuits using NMOS devices. They fabricated several fundamental circuits such as inverter, NAND, NOR, and delta literal by conventional NMOS technology. These circuits are consists of MOS transistors with three values of enhancement-mode threshold voltage and one depletion-mode threshold voltage.

## III. PREVIOUS WORK

As per the literature review, many of the authors used Quaternary to Binary and Binary to Quaternary conversion which consumes more power. Here we are going to implement combinational circuits without using any conversion so that we can consume less power and reduce the circuitry.

## IV. PROPOSED WORK

Here we propose Quaternary Half adder in voltage mode by using quaternary input and obtained the quaternary output without using any converter. Finally we will compare the results of Binary Half adder and Quaternary Half adder. The figure below shows the flow diagram showing all the modules of Quaternary Half adder.

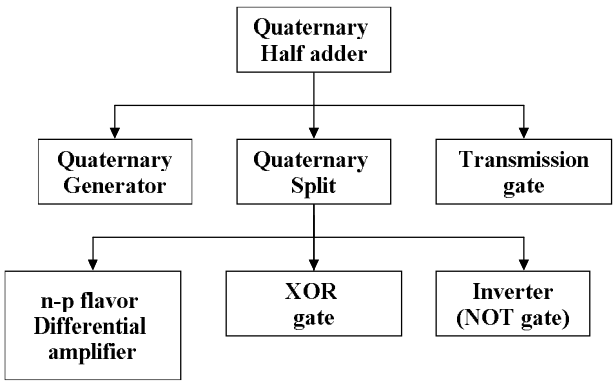


Figure1: Flow diagram showing modules of proposed design

The figure above shows the flow diagram of proposed module. It consists of Quaternary generator, Quaternary split, n-p flavour differential amplifier, XOR gate, inverter and transmission gate. These modules are for Quaternary half adder, the same modules can be used for Quaternary full adder with some modifications and changes. Each block is explained below in methodology.

### *A] METHODOLOGY*

i) Quaternary generator

The Quaternary generator consists of four logic levels. It is nothing but the pair wise logic signal generator which contains the time series such as

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time,0ns,0.165V,9.9ns,0.165V,10ns,0.495V,19.9ns,0.495V,20ns,0.66V,29.9ns,0.66V,30ns,0.825V,39.9ns,0.825V,40ns ,0.165V,49.9ns,0.165V,50ns.....139.9ns,0.495V,140ns,0.66V,149.9ns,0.66V,150ns,0.825V,159.9ns,0.825V for input and similar time series for output
time,0ns,0.165V,39.9ns,0.165V,40ns,0.495V,79.9ns,0.495V,80ns,0.66V,119.9ns,0.66V,120ns,0.825V,159.9ns,0.825V These voltages are generated using piecewise linear voltage source which is available in ADS tool. The figure below shows the results of Quaternary generator. This series is applied as the input to QHA.

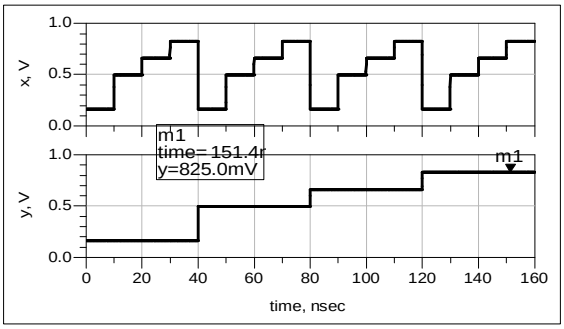


Figure 2: Simulation results of Quaternary generator

The figure above shows the results of above mentioned linear piecewise voltage and time series which is applied to the inputs of the proposed modules.

ii) Quaternary split

To design QHA, we need to design Quaternary Logic Level Checker i.e. Quaternary split which splits its input into four logic levels in place of conversion level. In the design of Quaternary split we design n-p flavour differential amplifier with XOR gate and inverter. This circuit is heart of the project which achieves high performance during the implementation. In this study, transmission gate is used as switch in logic operation of half adder. Quaternary split is used as a mediator in between quaternary input generator and transmission gate.

The split circuitry is used for converting the four logic levels i.e 0,1,2,3 into the series of individual pulses for 4 outputs which can be used to ON and OFF the switch matrix as shown below with its simulation waveform. The split circuit is basically an encoder. To avoid conversion we require split circuitry which can be used to switch the switch network according to truth table. The output of Quaternary split is used to switch the particular transmission gate in switch matrix. As told earlier it consists of differential amplifier, using this we create level converter which is nothing but the comparative ladder having some reference values and series of op-amp. After that there is a XOR gate in series which converts thermometer code into the required output.

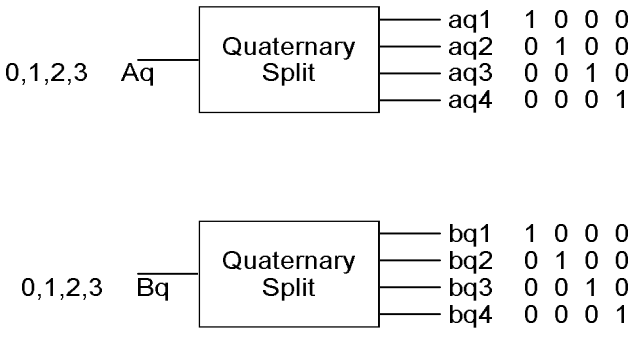


Figure 3: Quaternary split

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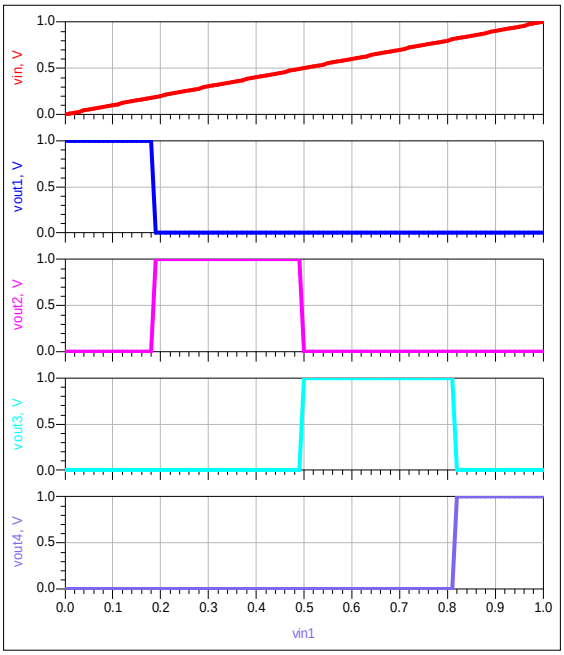


Figure 4: Simulation result of Quaternary split

The figure above gives the splits results as discussed Vout1= 1 0 0 0 , Vout2= 0 1 0 0 , Vout3= 0 0 1 0 and Vout4= 0 0 0 1.

iii) Transmission gate

The transmission gate (TG) is used in digital CMOS circuit design to pass or not pass a signal. Here TG are used in place of switches where the input is obtained at the output when the particular switch is closed.

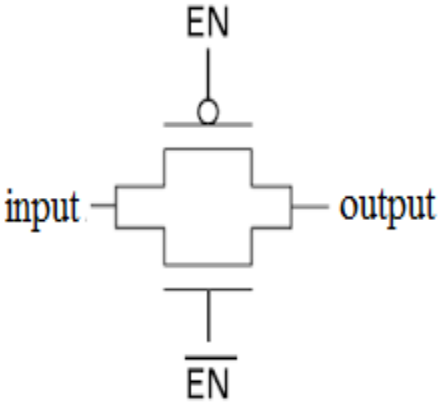


Figure 5: Diagram for Transmission gate

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| Aq | Bq | Sq | Cq |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 0 | 2 | 2 | 0 |
| 0 | 3 | 3 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 2 | 0 |
| 1 | 2 | 3 | 0 |
| 1 | 3 | 0 | 1 |
| 2 | 0 | 2 | 0 |
| 2 | 1 | 3 | 0 |
| 2 | 2 | 0 | 1 |
| 2 | 3 | 1 | 1 |
| 3 | 0 | 3 | 0 |
| 3 | 1 | 0 | 1 |
| 3 | 2 | 1 | 1 |
| 3 | 3 | 2 | 1 |

Table 1: Truth table of QHA

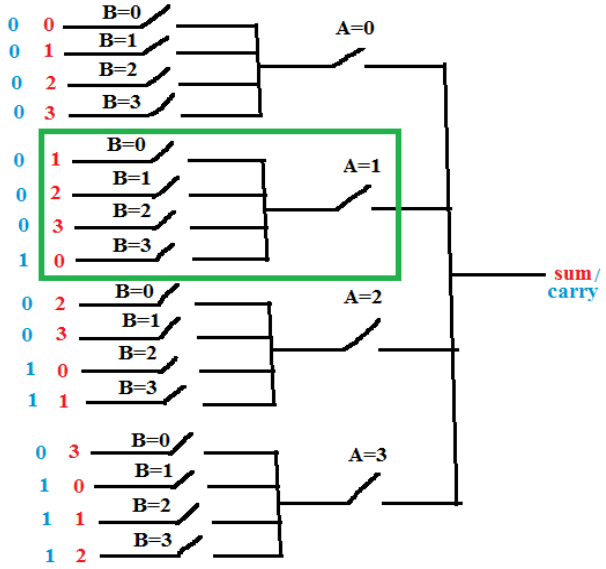


Figure 6: Switch matrix for Sum and Carry

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The figure above shows the simple switch matrix for sum (Sq) and Carry (Cq) which explains the truth table for Quaternary Half adder and its logic. From the figure, the inputs indicated in red are sum (Sq) and the one in blue are carry (Cq).

Consider when A=1, and B= 0,1,2,3 ; A=1 switch is closed and others are open, so we get sum as 1,2,3,0 or when A=1 and any one of the B input, say B=1; the switch A=1 will be closed and the switch indicating B=1 will be closed and hence we will get the sum =2; since 1+1=2.

## V. CONCLUSION

We are going to implement all the blocks as discussed in the methodology. As discussed earlier, Quaternary split i..e logic level checker also called as quaternary encoder is the main circuit of the project which avoids all types of conversions i.e. Quaternary to Binary and vice versa which drastically decreases the power. The switch network discussed is less complex and can be modified according to the various circuits such as subtractor, multiplier etc. The switch network is less complex and has low power. The influence of technology scaling and voltage scaling can be used for optimization.

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