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Low Delay and LUT for Universal Shift Register using PG and FG Reversible Gate

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ABSTRACT: Over the last few decades, reversible logic system/circuits have received considerable attention in the diversified fields such as nanotechnology, quantum computing, cryptography, optical computing and low power design of VLSI circuits due to their low power dissipation characteristics. In this paper, we proposed the design of reversible shift register (SR) i.e. serial-in-serial out (SISO), serial-in-parallel out (SIPO), parallel-in-serial out (PISO), parallel-in-parallel out (PIPO) SR and universal shift register using reversible D_FF. The D_FF is consisting of reversible PG and FG gate. The all design is implemented Xilinx software, VHDL language and calculated different parameter i.e. number of slice, number of look up table and maximum combinational path delay.

KEYWORDS: Serial in Serial Output (SISO), Serial in parallel out (SIPO), Parallel in Serial out (PISO), Parallel in Parallel out (PIPO), Maximum Frequency

I. INTRODUCTION

The synthesis of reversible logic circuits has been the main area of research in recent years. Reversible circuits are of high interest in the field of low power CMOS design, optical computing, quantum computing and nanotechnology. With increasing complexity of CMOS VLSI circuits, Power dissipation has become the main area of concern in VLSI design. It has been demonstrated by Landauer [1961] that circuits and systems constructed using irreversible logic will result in power consumption and energy dissipation due to information loss [1]. It is proved that the loss of one bit of information dissipates kT*log2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [1]. Bennett [1973] showed that zero power dissipation in logic circuits is possible only if a circuit is composed of reversible logic gates since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation [2]. The state of the output prior to and during present output transition must be known to perform a non-dissipative transition of the output. That is the copy of the state of the output must be present at all times which can be obtained by using reversible logic. The circuit constructed using Reversible logic do not erase or lose information. Reversible computation in a system can be performed only when the system comprises of reversible gates. The field of quantum computing also uses reversible logic. All quantum gates are reversible [3]. The number of output bits is relatively small compared to that of input bits in many computing tasks. All of the information encoded in the input must be preserved at the output in computational tasks such as digital signal processing, communication, computer graphics and cryptography. Hence there are compelling reasons to consider circuits composed of reversible gates and the synthesis of such networks.

II. DESIGN SYNTHESIS FLOW DIAGRAM

Synthesis is the process that reduces and optimizes the HDL or graphical design logic. Some third-party synthesis tools are available as a part of the FPGA vendor's complete development package. Simplicity's Simplify and Mentor Graphics' Leonardo Spectrum, Precision RTL and Precision Physical are some examples of third-party synthesis tools. Xilinx offers ISE Project Foundation, which is a complete development application that includes a synthesis tool [3]. Although some FPGA vendors offer synthesis, they still recommend using a third-party's synthesis tools. The synthesis tool must be set up prior to actually synthesizing the design. The synthesis process takes this information and the user-defined constraints and produces the output netlist. A constraints file specifies information like the critical signal paths and clock speeds. Synthesis can begin after completing set-up. General synthesis flow for tools involves three steps: creating structural element, optimizing, and mapping. Figure 1 shows a synthesis flow diagram.

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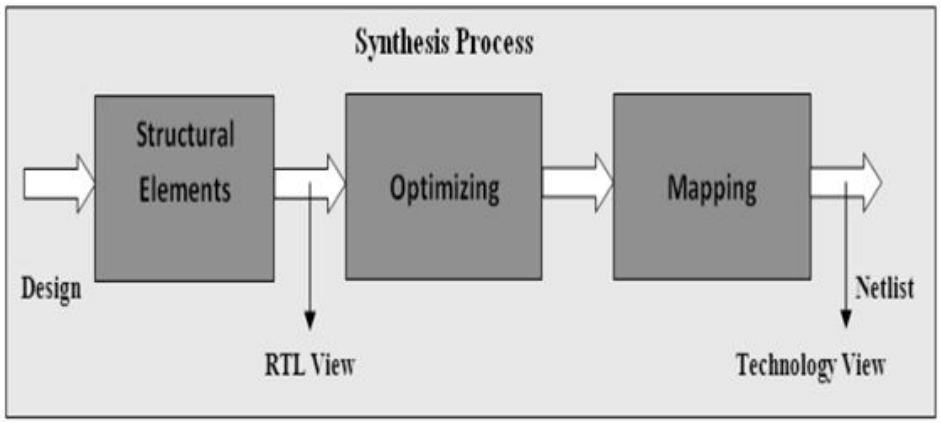

Figure 1: Design Synthesis Flow Diagram

The first step in the synthesis process takes the HDL design and compiles it into structural elements. The next step involves optimizing the design, making it smaller and faster by removing unnecessary logic and allowing signals to arrive at the inputs or output faster. The goal of the optimizing process is the make the design perform better without changing the circuit's functions. The final step in the synthesis process maps or associates the design to the vendor specific architecture [4]. The mapping process takes the design and maps or connects it using the architecture of the specific vendor. This means that the design connects to vendor specific components such as look-up tables and registers. The optimized netlist is the output of the synthesis process. This netlist may be produced in one of several formats. Edif is a general netlist format accepted by most implementation tools, while '.xnf' format is specific to Xilinx and is only recognized by Xilinx's implementation. In addition to the optimized netlist, many synthesis tools like Simplify will produce a netlist for gate-level simulation and other report files. Stimulus applied to this netlist instead of the original HDL design produces the functional-level simulation, which lets the designer verify that the synthesis process hasn't changed the design's functions.

III. PROPOSED METHODOLOGY

This sequential device loads the data present on its inputs and then moves or "shifts" it to its output once every clock cycle, hence the name Shift Register. A shift register basically consists of several single bit "D-Type Data Latches", one for each data bit, either a logic "0" or a "1", connected together in a serial type daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on. Data bits may be fed in or out of a shift register serially, that is one after the other from either the left or the right direction, or all together at the same time in a parallel configuration. The number of individual data latches required to make up a single Shift Register device is usually determined by the number of bits to be stored with the most common being 8-bits (one byte) wide constructed from eight individual data latches. Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices. Shift register IC's are generally provided with a clear or reset connection so that they can be "SET" or "RESET" as required. Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:

- Serial-in to Serial-out (SISO) - the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.
- Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
- Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- Parallel-in to parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

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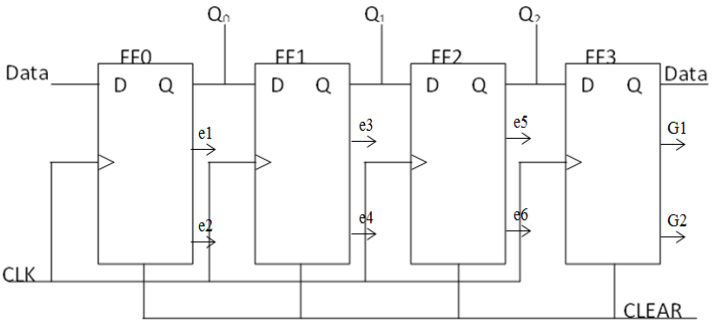

Figure 2: Flow Diagram of Serial in Parallel Output Shift Register

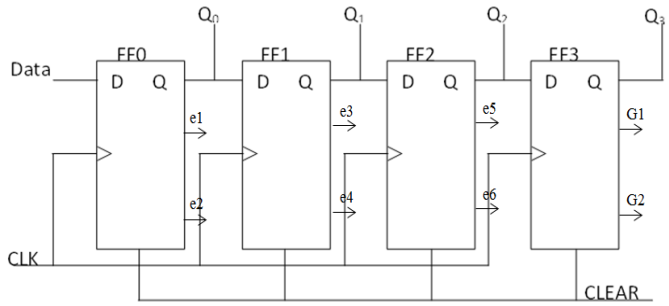

Figure 3: Flow Diagram of Parallel in Serial Output Shift Register

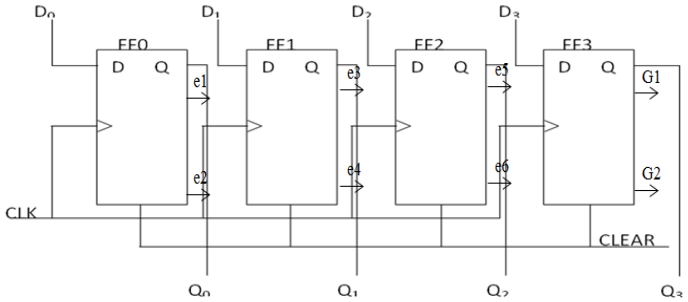

Figure 4: Flow Diagram of Parallel in Parallel Output Shift Register

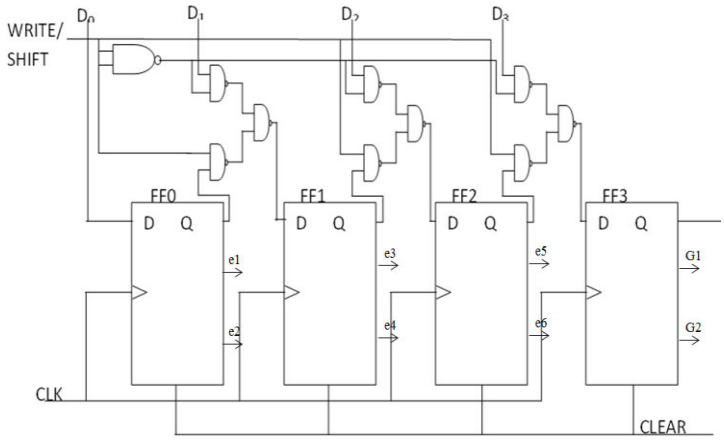

Figure 5: Block Diagram of Reversible Parallel in Serial out Shift Register

Reversible D_FF

In the figure bellow (fig. 6) [6], FLIP-FLOP D is designed with five conventional irreversible NAND gates. The Figure (fig. 7) shows its reversible equivalent.

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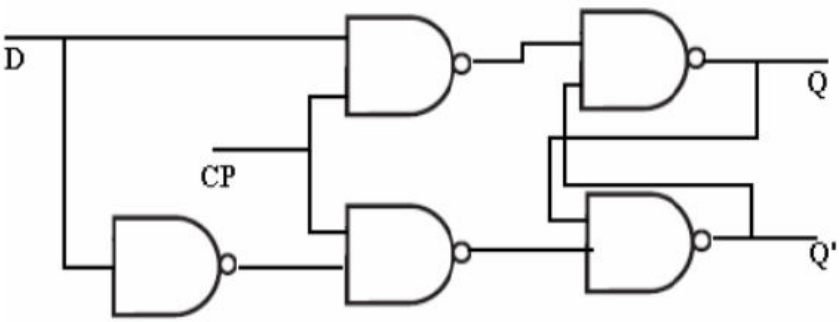

Figure 6: Conventional D Flip Flop

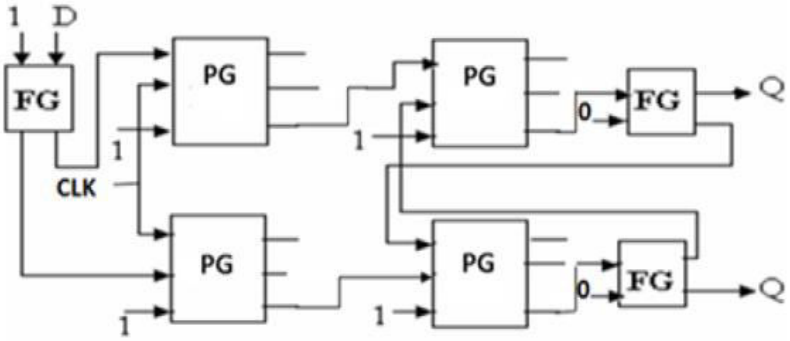

Figure 7: Our Design D Flip Flop with Reversible Gates

IV. SIMULATION RESULT

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 14.1i updated version. Xilinx 9.2i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISE™ (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low. ISE 14.1i that provides advanced tools like smart compile technology with better usage of their computing hardware provides faster timing closure and higher quality of results for a better time to designing solution. ISE 14.1i Xilinx tools permits greater flexibility for designs which leverage embedded processors. To simplify multi rate DSP and DHT designs with a large number of clocks typically found in wireless and video applications, ISE 14.1i software features breakthrough advancements in place and route and clock algorithm offering up to a 15 percent performance advantage. Xilinx 14.1i Provides the low memory requirement while providing expanded support for Microsoft windows Vista, Microsoft Windows XP x64, and Red Hat Enterprise WS 5.0 32-bit operating systems.

VTS and RTL of 4-bit universal reversible SR with D_in (3 down to 0), clk, rst and Q (3 down to 0) entity of 4-bit universal reversible SR is present in fig. 8 and fig. 9.

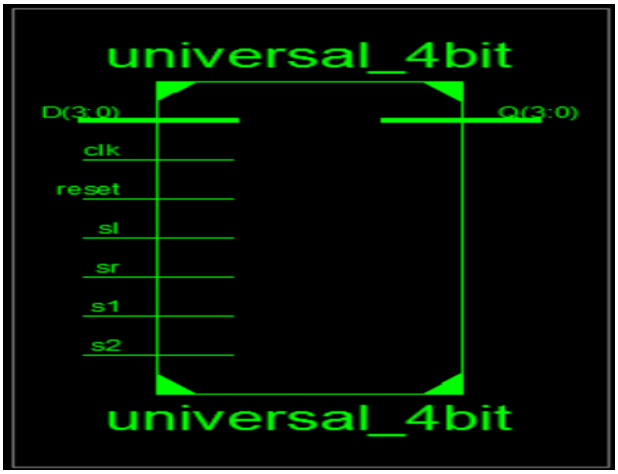

Figure 8: VTS of 4-bit Universal Reversible SR

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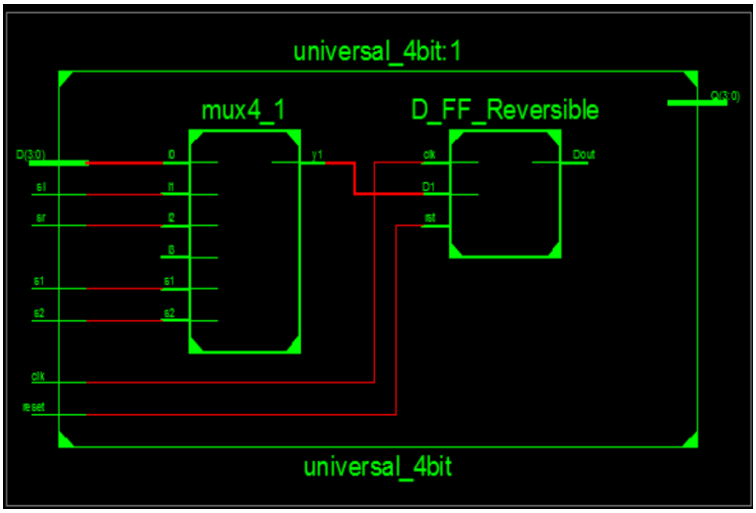

Figure 9: RTL of 4-bit Universal Reversible SR

DUS of 4-bit universal reversible SR is present in fig. 10. The MCPD is 10.690 ns present for 4-bit universal reversible SR.

```
Device utilization summary:
---------------------------

Selected Device : 3s50pq208-4

 Number of Slices:                       11  out of    768     1%
 Number of Slice Flip Flops:              4  out of   1536     0%
 Number of 4 input LUTs:                 25  out of   1536     1%
 Number of IOs:                          14
 Number of bonded IOBs:                  13  out of    124    10%
 Number of GCLKs:                         1  out of      8    12%
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 4.555ns (Maximum Frequency: 219.539MHz)
   Minimum input arrival time before clock: 5.077ns
   Maximum output required time after clock: 10.242ns
   Maximum combinational path delay: 10.690ns
```

Figure 10: DUS of 4-bit Universal Reversible SR

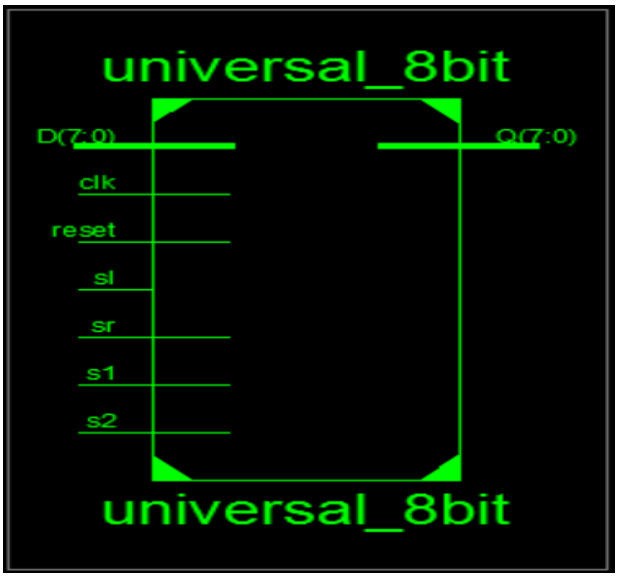

Figure 11: VTS of 8-bit Universal Reversible SR

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```
Device utilization summary:
---------------------------

Selected Device : 3s50pq208-4

 Number of Slices:                       10  out of    768     1%
 Number of Slice Flip Flops:              4  out of   1536     0%
 Number of 4 input LUTs:                 23  out of   1536     1%
 Number of IOs:                          22
 Number of bonded IOBs:                  16  out of    124    12%
 Number of GCLKs:                         1  out of      8    12%

Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 4.628ns (Maximum Frequency: 216.076MHz)
   Minimum input arrival time before clock: 5.076ns
   Maximum output required time after clock: 10.379ns
   Maximum combinational path delay: 10.827ns
```

Figure 12: DUS of 8-bit Universal Reversible SR

V. CONCLUSION

In this paper, we have discussed the VHDL implementation of configurable linear feedback shift register by number of slice, number of flip flop, input output bounded, minimum period, arrival time before max input clock, arrival time after max input clock and maximum frequency. Its means that the proposed universal shift registers is high speed compared to previous design.

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