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Simulation and Synthesis of a Novel Approach for Parallel BCD Multiplier

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ABSTRACT: Nowadays, to perform to perform arithmetic operations in financial, commercial, internet and scientific based applications, decimal multiplication plays a crucial role. In this paper, a fully pipelined decimal multiplier has been designed consists of carry save adder and the same grouped to BCD-4221. The proposed design is presented based on multiplier operands recoded in Signed Digit (SD) Radix-10, it also consists of a simplified partial products generator and decimal adders. Different types of models has been proposed in several ways but these synthesis and simulation results were exhibits the optimized performance parameter values in terms of delay/speed and area.

KEYWORDS: Arithmetic Operations, BCD, Decimal Floating Point, Signed Digit Radix-10, FPGA**.**

I. INTRODUCTION

Decimal arithmetic became a requirement in the computation of many applications, like financial and commercial, where the results must match those obtained by human calculations. This is why over recent years decimal operations have become popular. The new revision of the IEEE 754-2008 standard for floating point arithmetic includes specification decimal multiplication format serves to satisfies the development of high performance .An important and frequent operation in many applications is decimal multiplication. It is complex to implement in hardware due to the larger range of decimal digits (0, 9) and the inefficiency of binary codes to represent decimal values, so that decimal multipliers have lower performance and larger area than comparable binary multipliers. For example, because of the high-area requirements of a pipelined parallel implementation, decimal multiplication in IBM Power6 and Z/system high-end processors is performed serially using a BCD (Binary Coded Decimal) carry-propagate adder and hardware assists.

In this Paper, the generation of decimal partial products is based on the techniques described below. First of all, decimal digits of A are represented in BCD-4221 (4221) to prevent the corrections previously mentioned. This reduces the computation complexity of multiplicand multiples coded into (4221). A BCD-5211 (5211) format is introduced in this Section. Both of these formats are necessary to determine the set of multiples.The rest of the paper organized as follows. Section-2 depicts about the existing design. Section-3 represents the proposed design based on the BCD multiplier. Section-4 consists of the simulation and synthesis results of the proposed design. Finally the paper is concluded with necessary notations and summary.

II. EXISTING DESIGN

Decimal multiplication coded in BCD-8421 (8421) presents a more complex implementation than binary multiplication due to the presence of invalid (8421) digits between {A, B, F}. These need to be corrected generating an extra cost in computation as well as additional multiplicand multiples that must be implemented by the multiplier.

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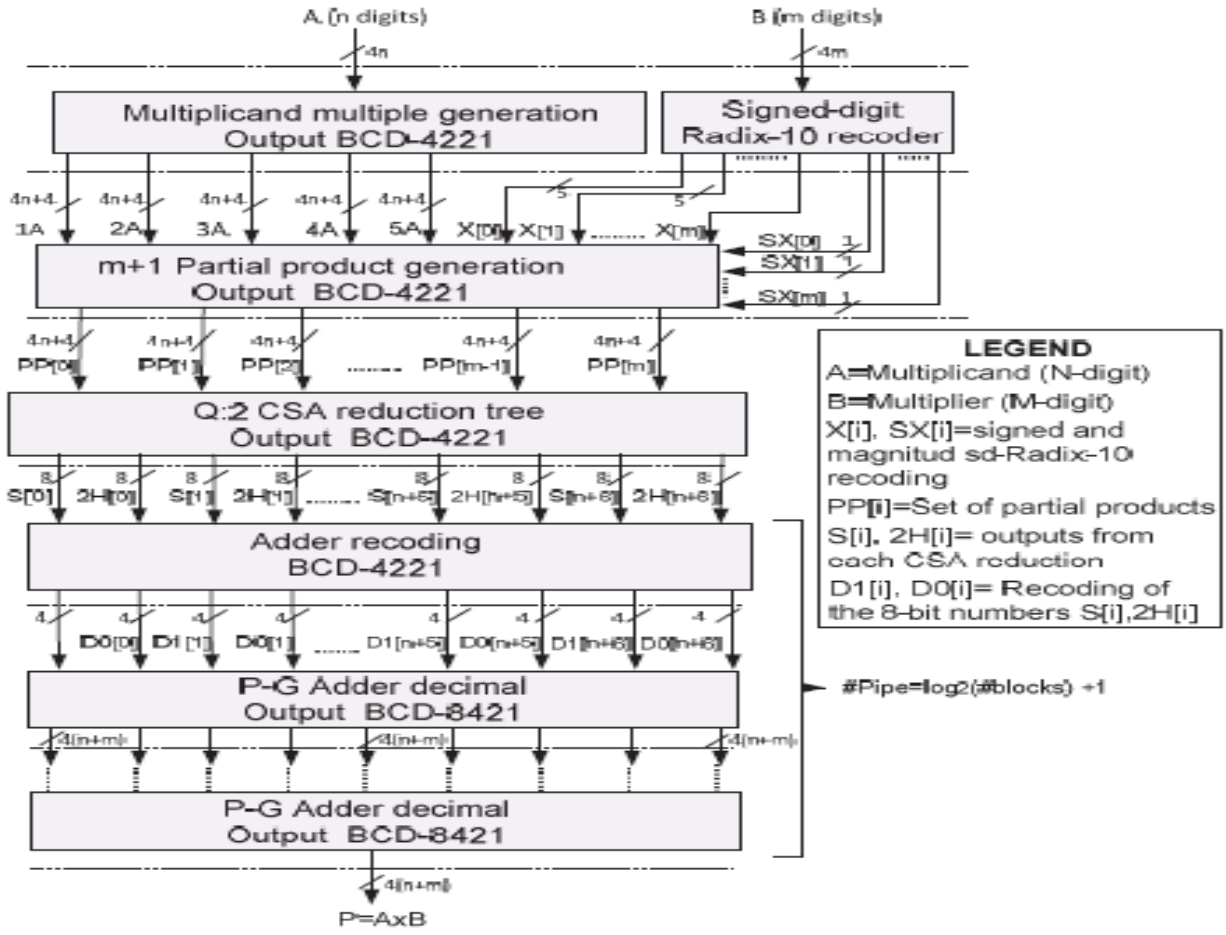

Figure 1: General Structure of a BCD Multiplier

III. PROPOSED DESIGN

The generation of decimal partial products is based on the techniques described below. First of all, decimal digits of A are represented in BCD-4221 (4221) to prevent the corrections previously mentioned. This reduces the computation complexity of multiplicand multiples coded into (4221). A BCD-5211 (5211) format is introduced in this Section. Both of these formats are necessary to determine the set of multiples.

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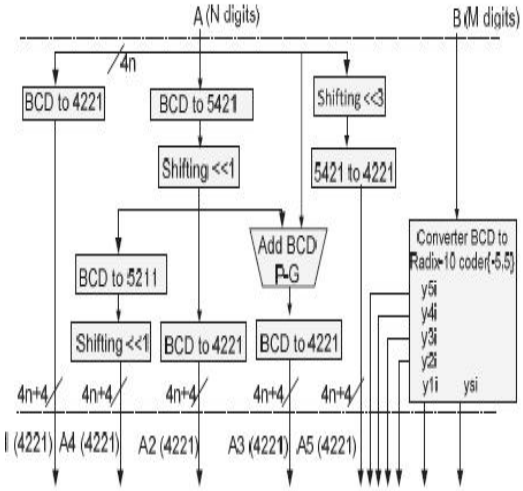
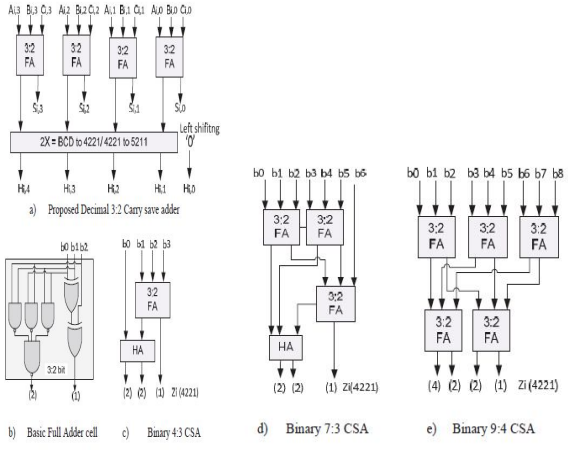


a) Multiplicand Multiples Generation

N	(4221)	Reduced (4221)
0	0000	0000
1	0001	0001
2	0100, 0010	0100
3	0101,0011	0101
4	0110,1000	0110
5	1001,0111	1001
6	1010,1100	1010
7	1011,1101	1011
8	1110	1110
9	1111	1111

b) Reduced BCD-4221 coding

A N-digit multiplicand A and a M-digit multiplier B as unsigned decimal are assumed. The (8421) multiplication is processed as follows: the multiplicand multiples generation unit takes the operand A and computes a set of N + 4-digitmultiplicand multiples {1A, 2A, 3A, 4A, 5A} coded into (4221). In parallel, the sd-radix-10 unit recodes each digit (8421) of B between {-5, -4, -3, +3, +4, +5} that is represented with a 1-bit sign and 5-bit magnitude format. There coded B is multiplied digit-by-digit by the previously computed multiplicand multiples. It is important to emphasize that the (8421) coding introduces a computational cost due to the corrections in the decimal reduction CSA. An alternative to prevent this drawback is to use (4221) coding



a) Proposed Decimal 3:2 Carry save adder
b) Basic Full Adder cell
c) Binary 4:3 CSA
d) Binary 7:3 CSA
e) Binary 9:4 CSA

Figure Proposed Decimal 3:2 CSA and several Binary Adder schemes

The block diagram is depicted in the Fig. 2a, the recoding is applied to each digit of B. This transforms a 8421) set {0, 1, 2.., 9} into the signed-digit set {-5, -4… +4, +5} made up of a sign signal SX(i) and a 5-bit magnitude X(i). Each digit X(i) selects the corresponding multiplicand multiples coded in(4221). The sign SX verifies if a negative multiple is produced. It is important to highlight that a negative version of a partial product is obtained simply by inverting the bits of the positive version using arrays of XOR gates manipulated by SX(i). The above circuit requires 2 slices and 6 LUTs. The following section discusses Multiplicand Multiples Generation (Fig. 2a), this set of multiples are coded into(4221). Multiples 2A and 5A are generated with re-coding(8421 to 4221, 5211 to 4221) and carrying out

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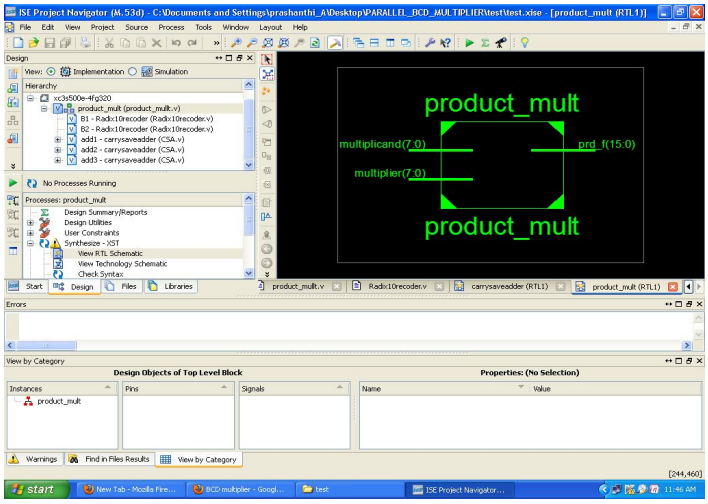
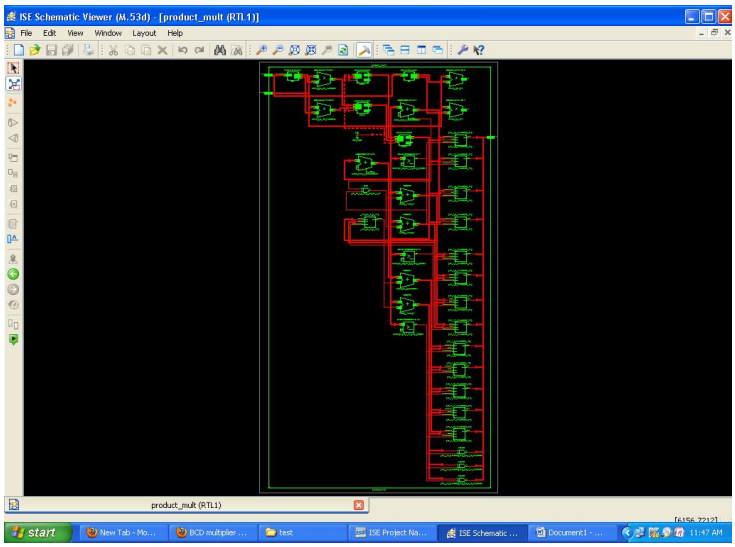
a left shifting process. Multiple 4A is computed as 2x2A and 3A comes from a decimal addition between A and 2A. Each partial product has N + 3 digits.

B. Reduction partial product

After generating the M + 1 partial products, coded into (4221), the reduction of partial products is developed by means of decimal Q:2 carry save additions (CSA). First, the partial products are aligned and divided into blocks as it is shown in Fig 4. A circuit based on decimal 3:2, 4:2, and 8:2 CSA compressors is proposed, which entail to utilize block sizes of(M + 3 + M / #blocks) x Q decimal operands.

IV. EXPERIMENTAL RESULTS





The RTL Schematic of BCD Multiplier Top Module is as showninabovefig.Which yields lowercomplexity by increasing throughput.

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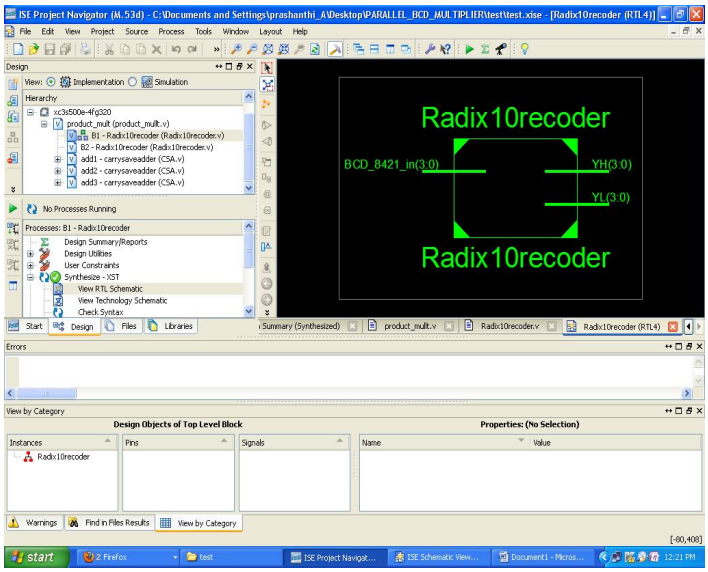

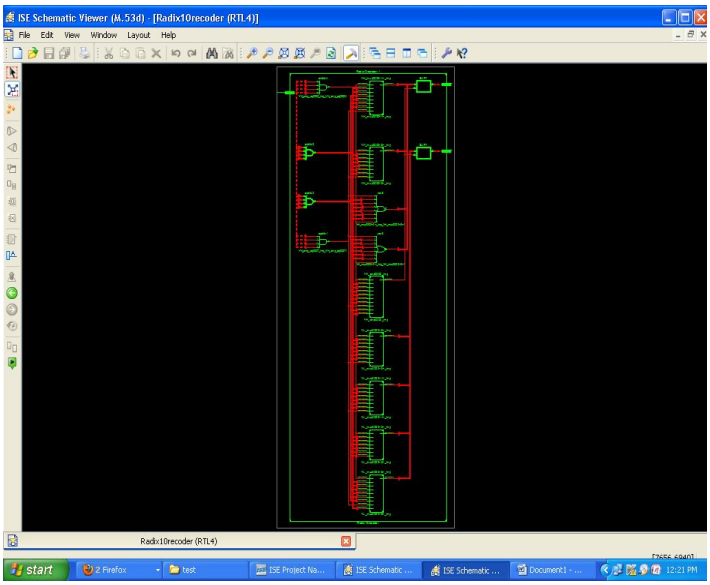

The RTL Schematic of BCD Multiplier Radix-10 Booth Recoder Module and its Internal Diagram is as shown in abovefig.Which yields lowercomplexity by increasing throughput and performance.

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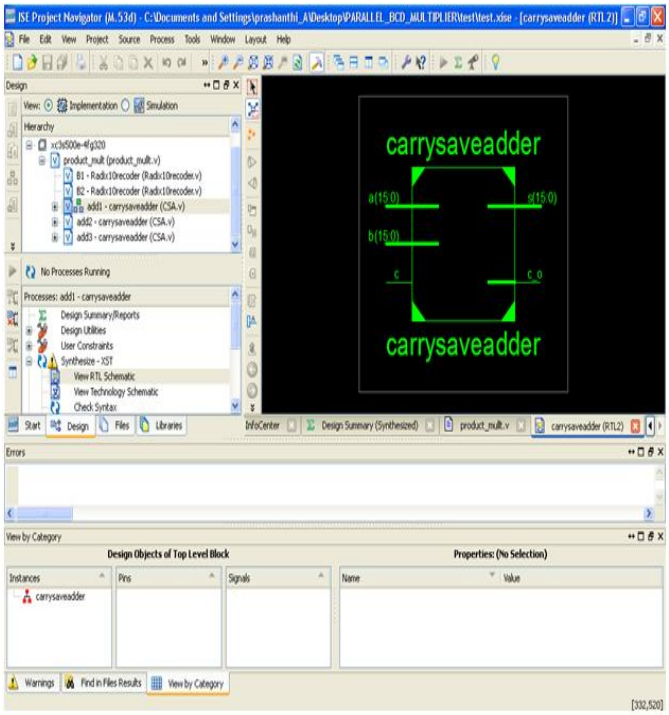

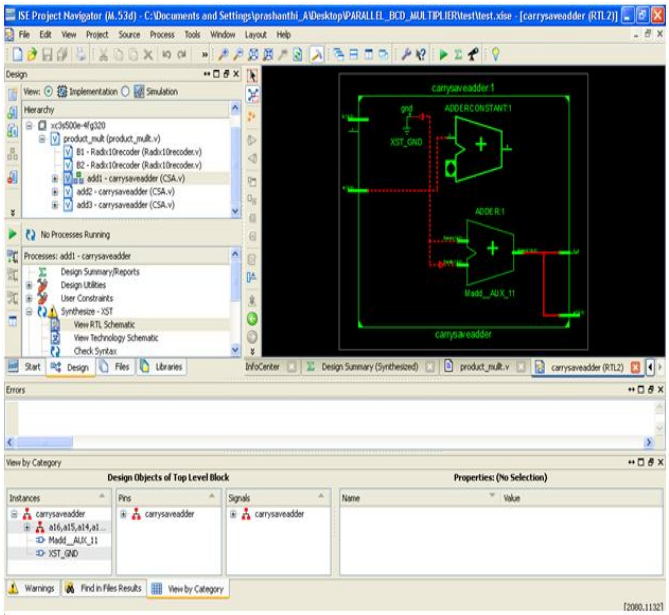

The RTL Schematic of BCD Multiplier Carry Save Adder Module and its Internal Diagram is as shown in abovefig.Which yields lowercomplexity by increasing throughput and performance.

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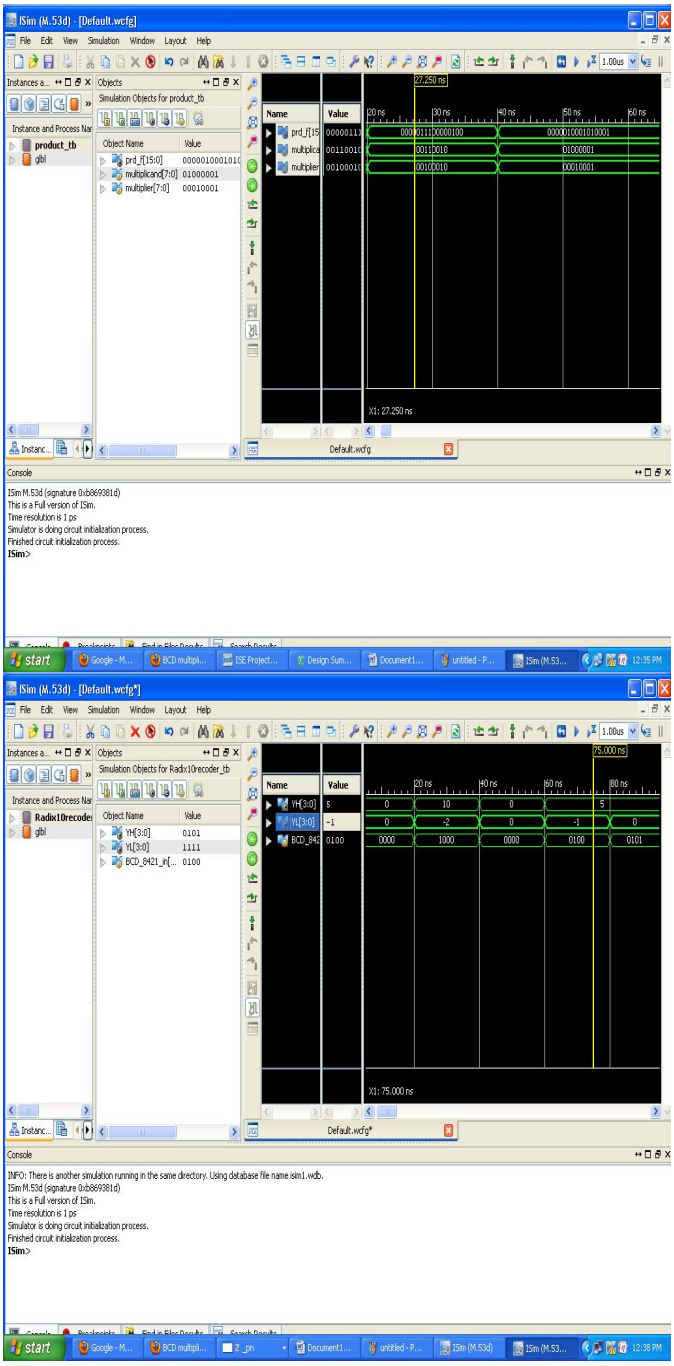
V. SIMULATION RESULTS



The Simulation Results of BCD Multiplier Top Module and its Results in analyzing the Performance is as shown in abovefig.Which yields lowercomplexity by increasing throughput and performance.

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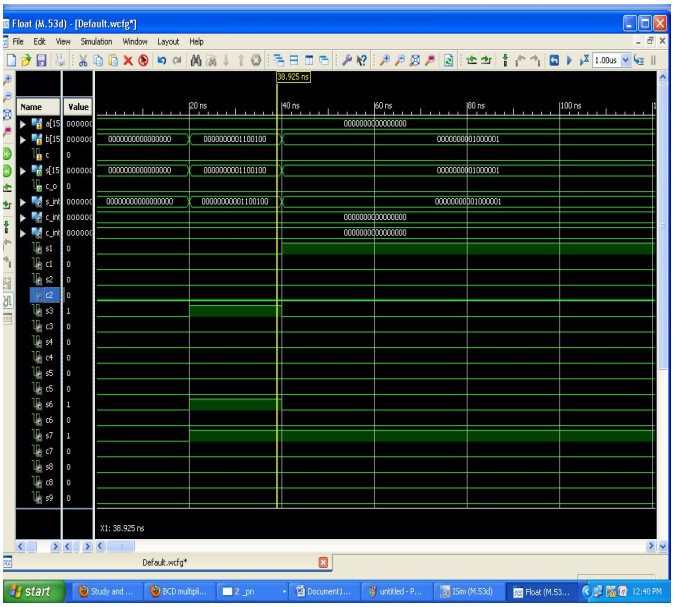

VI. CONCLUSION

This work presents the design of several BCD multipliers and their implementations on Virtex-6 FPGA. Previous techniques and designs proposed are analyzed to carry out Performance comparison in terms of area-delay as it was seen in Section 4.The proposed pipelined multiplication is based on a multiplier operand coded into SD radix-10 recoding. A parallel generation of decimal partial products is reduced by carry save adder techniques and decimal adders. The proposed circuit presents a high-performance design of decimal multiplier. Our proposal shows encouraging results one hand, its figures are comparable and outperformed than other multipliers. The other hand, a considerable number of cores can be fit into large FPGA.

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