



IJIRCCCE

e-ISSN: 2320-9801 | p-ISSN: 2320-9798



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN COMPUTER & COMMUNICATION ENGINEERING

Volume 8, Issue 10, October 2020

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 7.488

 9940 572 462

 6381 907 438

 ijircce@gmail.com

 www.ijircce.com

Process Selection of Photolithography in VLSI

Amar Prakash Sinha

Department of Electronics and Communication Engineering, BIT Sindri, Jharkhand, India

ABSTRACT: Decreasing cost reducing size and increasing performance of electronic products ascertains that fabrication technique in this field has to be matured. Always important trends have been – decreasing feature size, increasing chip and wafer size, increasing integration level, reduced defect density and power dissipation etc. Automation in the fabrication of VLSI chip is required to face the requirements for these trends and the challenges of the competitive global market. This paper discusses certain issues of automation in the fabrication area. The processes in VLSI fabrication have a large number of alternative methods and setups. This paper has used Factor Comparison Method from Value engineering to select the best suitable option for the purpose of automation and also meeting the demands of current trends.

I. INTRODUCTION

Electronic devices have been witnessing revolutionary improvements since the era of vacuum tube till the present time of VLSI (very Large scale Integration) and ULSI (Ultra Large Scale Integration). The improvements have been both in the structure as well as in the processes. In structure, invention of new device designs allowing greater circuit performance, power control and reliability has been noticed. Changes in the process are fabrication of devices and circuits in smaller dimensions in ever higher density, quantity and reliability. Feature size and Integration level are the index of IC development. Semiconductor Industry Association (SIA) has predicted the future targets for development indices and the IC manufacturing industry has to gear up technologically to face the requirements and challenges of these developments. The nature of the process and the requirements of the current trends of the product make the IC fabrication highly suitable for automation and robotization.

Manufacturing of solid state devices are in four distinct stages - Material preparation, Crystal growing and wafer preparation, Wafer fabrication and packaging. Each of these stages has many sub stages. A lot of material handling is required during these sub stages. The wafer has to move between different workstations many times in infinite number of sequences. So, Automating the material handling will be extremely beneficial.

Solid state devices are manufactured in four distinct stages – Material preparation, Crystal growing and wafer preparation, Wafer fabrication and packaging. Each of these stages have several sub stages. The wafer moves between workstations for these sub stages many times in infinite sequences during manufacturing. So there is a vast amount of material handling and huge benefits can be gained by the automation of material handling in microchip manufacturing.

photolithography is one of the four basic operations of the wafer fabrication or commonly called fab. Patterning, Photomasking, Masking, Oxide or Metal Removal (OR, MR) and Microlithography are some of the terms used for the same. It is very much similar to photography where the required pattern is first formed in reticles or photomasks and transferred into the surface layers of wafers through photomasking steps.

II. PROBLEM DEFINITION

There are ten basic processes in photolithography – 1. Surface Preparation, 2. Priming, 3. Photoresist Spinning, 4. Soft Bake 5. Alignment and Exposure, 6. development, 7. Hard Bake, 8. Develop Inspect, 9. Etch, 10. Resist Stripping. Some or all of these processes are used in different sequences. Each of the processes in Photolithography has a large number of alternative methods and setup. We have to select for each process the option that is best suitable for our purpose of automation and must also be capable to meet the requirements of current development trends.

III. METHODOLOGY

Factor Comparison Method was used for the selection of appropriate option from the different alternative methods available for a process. Different factors/criteria affecting the process selection were compared with each other in a Paired Comparison Matrix. Based on their degree of superiority over other they were assigned a suitable weight. The sum of weights for each factor was calculated. This weight was carried by corresponding factor in the decision matrix.

Decision matrix is an alternative option Vs. criteria matrix, where each alternative is given certain score for each criteria depending upon its performance against that criteria. This score is multiplied by the corresponding weight

of the criteria. Finally adding all this product in a row of the alternative gives us the total score of that alternative. Naturally the alternative with highest total score will be the best suitable process.

IV. RESULTS AND DISCUSSION

As explained earlier, the photolithography process involves large number of steps. A detailed study with advantages and limitations of each of the steps was done and process selection for each step was made using the explained methodology. Here a few of the more significant processes are discussed.

(a) Alignment and Exposure :

S.No	Aligner system	Exposure Sources	Resolution (microns)	Throughput in wafers/ hr.
1	Contact/Proximity	Hg	0.25 – 0.50	30 – 120
2	Scanning / Projection	Hg	0.9 – 1.25	30 – 100
3	Step and Repeat	Hg/KrF/DUV	0.35 – 0.80	65 – 90
4	Step and scan	Hg/KrF/DUV	0.25 – 0.40	50 *
5	X - Ray	X - ray	0.10 -	20+
6	E - Beam	Electron beam	0.25 -	2 - 10

Table1: Evaluation chart for different Alignment and Exposure processes

The factors for process selection are :

- A) Resolution
- B) Wafer throughput
- C) Compatibility for automation
- D) Capability to meet requirements of current trends

Paired Comparison Matrix :

- 0 – No difference
- 1 – Minor difference
- 2 - Medium difference
- 3 – Major difference

	B	C	D	Total
A	A1	C2	D2	1
	B	C2	D3	0
		C	D1	4
			D	6

Decision Matrix :

1 – Poor, 2 – Average, 3 – Good, 4- Very good, 5- Excellent

S.No.	Criteria Alternatives	A	B	C	D	Score
		1	0	4	6	
1	Contact / Proximity	3	3	2	1	17
		3	0	8	6	
2	Scanning / Projection	2	3	3	1	20
		2	0	12	6	
3	Step and repeat	2	3	3	2	26
		2	0	12	12	
4	Step and Scan	3	3	4	4	43*
		3	0	16	24	
5	X - Ray	4	2	3	4	40
		4	0	12	24	
6	E - Beam	3	2	3	4	39
		3	0	12	24	

Table2 Process selection for Alignment and Exposure

*As Step and Scan process has highest score hence it is selected for Alignment and Exposure.

Limitations of contact aligner systems are

- They are manual in operation and control.
- Contact damages the soft resist layer, the mask or both.
- Contact can leave dirt on the mask affecting the exposure.
- Alignment of larger diameter wafers presents a light uniformity problem.

The problems related to contact between photoresist and mask are minimized by Proximity aligners, but the resolution capability is affected as mask is not in contact with resist. So, these are not used in VLSI photomasking.

Scanning projection aligners have limitations such as alignment and overlay problems associated with the full size mask, image distortion and masking induced defects from dust and glass damage.

* A better overlay and alignment are provided by stepping system because each chip is individually aligned. The stepping allows precise matching of larger diameter wafers. Other advantages are resolution improvements and less vulnerability to dust and dirt.

Automatic alignment system is the main reason for use of steppers in production. Passing low energy beams through alignment marks on the reticle and reflecting them of corresponding alignment marks on the wafer surface, a signal is received and analyzed with computer. It also moves the chuck in required direction to get the correct registration.

(b) Development :-

The factors for process selection are :

- A) Compatibility for automation
- B) Developer consumption
- C) Wafer throughput
- D) Capability to meet requirements of current trends

Paired Comparison Matrix :

- 0 – No difference
- 1 – Minor difference
- 2 - Medium difference
- 3 – Major difference

	B	C	D	Total
A	A3	A2	D2	5
	B	C2	D3	0
		C	D2	2
			D	7

Decision Matrix :

1 – Poor, 2 – Average, 3 – Good, 4- Very good, 5- Excellent

S.No.	Criteria Alternatives	A	B	C	D	Score
1	Immersion Development	5	0	2	7	30
		2	2	3	2	
2	Spray Development	10	0	6	14	51*
		3	3	4	4	
3	Puddle Development	15	0	8	28	51*
		3	3	4	4	
		15	0	8	28	

Table 3 Process selection for Development

*As Spray and Puddle development have same score hence any one of the two can be used as per type of photoresist used. The work station and equipments are same in both the options.

Limitations of the immersion system are –

- Surface tension of developer prevents it from penetrating into small openings.
- Tank becomes contaminated as hundreds of wafers are processed through them.
- Probability of wafer contamination because they are drawn through liquid surface

- Fluctuation in room temperature changes the developing rate of solution
- Directionality is poor.

Advantages of Spray development are –

- Better image definition due to mechanical action of the spray pressure.
- Reduction in the chemical used
- Spray system is cleaner as each wafer is developed with fresh chemical.
- Single wafer processing is possible, hence suitable for in-line automation.
- Limitation of spray system is with positive resist development which is extremely temperature sensitive and adiabatic cooling reduces the developer temperature.

Puddle development combines the benefits of immersion and spray development and overcomes the drawback of spray development regarding positive resist.

* So the choice is spray or puddle development process, depending upon the type of resist used. The workstation is of same design for both the processes.

(C) Etch :-

The factors for process selection are :

- Compatibility for automation
- Selectivity
- Directionality
- Capability to meet requirements of current trends
- Wafer throughput

Paired Comparison Matrix :

0 – No difference

1 – Minor difference

2 - Medium difference

3 – Major difference

	B	C	D	E	Total
A	A2	A2	D2	A3	7
B		B1	D2	B2	3
		C	D2	C2	2
			D	D3	9
				E	0

Decision Matrix :

1 – Poor, 2 – Average, 3 – Good, 4- Very good, 5- Excellent

S.No.	Criteria Alternatives	A	B	C	D	E	Score
1	Immersion etching	2	3	1	1	2	34
		14	9	2	9	0	
2	Spray etching	3	3	2	3	2	61
		21	9	4	27	0	
3	Plasma etching (Barrel)	4	2	2	3	3	65
		28	6	4	27	0	
4	Plasma etching (Planar)	4	2	3	3	3	67
		28	6	6	27	0	
5	Ion Milling	4	1	4	3	3	66
		28	3	8	27	0	
6	R.I.E.(Reactive Ion Etching)	4	2	4	3	3	69*
		28	6	8	27	0	

Table 4 Process selection for Etching

*As R.I.E. process has highest score hence it is selected for Etching.

Limitations of different wet etching methods are –

- Wet etching is limited to pattern sizes of 3 μm.
- Wet etching is isotropic, resulting in sloped side walls

- A wet etch process requires rinse and dry steps.
- The wet chemicals are hazardous and / or toxic.
- Wet processes represent a contamination potential.
- Failure of the resist – wafer bond causes undercutting.

Limitations of Barrel Plasma Etcher are –

It is isotropic in nature, resulting in sloped side walls.

Etch Uniformity is a problem.

Radiation damage from the high energy plasma field

In–line automation is a problem.

Above problems are reduced to a large extent by Planar Plasma Etcher but the problem of radiation damage still persists.

Ion Milling is a physical process so it has a better directionality but has a poor selectivity. Also radiation damage from the ionization mechanism is a problem

Reactive Ion Etching system combines plasma etching and ion milling. It has an excellent selectivity. So, R.I.E. systems have become the etching system of choice for most advanced product lines.

V. CONCLUSIONS

Using the methodology discussed above, for each process of photolithography the best suited option for the purpose of automation and its capability to meet the requirements of current development trends had been made. The processes and the selected method has been given in the table 5 –

S.No.	Operations	Method selected
a.	Dehydration Bake	Conductive moving belt
b.	Priming	Automatic spinner
c.	Photoresist spinning	Automatic spinner
d.	Soft bake	Conductive moving belt
e.	Alignment and exposure	Step and scan
F.	Development	Spray / Puddle development
g.	Etch	Reactive Ion Etching (RIE)

Table 5, selected options for each of the process

REFERENCES

- [1] . Elliot D. J., Integrated circuit fabrication, 2nd edition, McGraw – Hill Publishing Company, NY, 1989
- [2] Zant P. V., Microchip fabrication – A Practical Guide to Semiconductor Processing, 4th ed., McGraw – Hill Publishing Company, NY,
- [3] Groover M. P., Automation Production system and Computer Integrated Manufacturing, 2nd edition, Pearson Education, ND.
- [4] Kumar S., Industrial Robots and Computer Integrated Manufacturing, Oxford and IBH Publishing Company Pvt. Ltd. ND, 1992
- [5] Pillai, D., Material Handling Automation for wafer fabrication facilities, IEEE Ninth International Electronic manufacturing Technology symposium , Washington. DC , USA 1990, p. 277-86
- [6] Pierce N.G. Stafford R., Modeling and simulation of material handling for semiconductor wafer fabrication, IEEE Winter Simulation conference. Lake Buena Vista. FL. USA 1994. p 900- 6.
- [7] Kumar S. and Agarwal A., Value Engineering and Cost Control (A Fast Track to Profit Improvement), Dhanpat Rai & Co., Delhi



INNO  SPACE
SJIF Scientific Journal Impact Factor

Impact Factor:
7.488

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN COMPUTER & COMMUNICATION ENGINEERING

 9940 572 462  6381 907 438  ijircce@gmail.com



www.ijircce.com

Scan to save the contact details