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High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications

Pallavi R. Yewale

ME Student, Dept. of Electronics and Tele-communication, DYPCOE, Savitribai phule University, Pune, Maharashtra, India.

ABSTRACT: Transpose form finite impulse response (FIR) filter is naturally a pipelined structure which supports the multiple constant multiplications (MCM) technique but direct form FIR filter structure does not support MCM technique. The MCM is more effective in Transpose form when the common operand is multiple with the set of constant coefficients that reduce the computational delay. The implementation of MCM technique is easier in fixed coefficient Transpose form FIR filter but complex in reconfigurable coefficients. In fixed coefficients transpose FIR filter, area and delay are reduced by using MCM technique. The low-complexity design using the MCM technique is implemented for fixed coefficients transpose form FIR filters and multiplier-based design is used for reconfigurable transpose form FIR filter. The implemented transpose form FIR filter structure achieved less area and delay than the direct-form FIR filter structure. The XILINX software tool is used for simulation.

KEYWORDS: Transpose form FIR filter, multiple constant multiplications (MCM) technique, Block processing.

I. INTRODUCTION

Finite Impulse response (FIR) digital filter is used in several DSP applications, such as, echo cancellation, speech processing, equalization, adaptive noise cancellation, and various communication applications, including software-defined radio (SDR), etc. Many of these applications require FIR filters of large order to meet the stringent frequency specifications. And this filters need to support high sampling rate for high-speed digital communication. The number of multiplications and additions required for their filter output, increases linearly with the filter order. Nodes in MANET have limited battery power and these batteries cannot be replaced or recharged in complex scenarios. To prolong or maximize the network lifetime these batteries should be used efficiently. The energy consumption of each node varies according to its communication state: transmitting, receiving, listening or sleeping modes. Researchers and industries both are working on the mechanism to prolong the lifetime of the node's battery. But routing algorithms plays an important role in energy efficiency because routing algorithm will decide which node has to be selected for communication.

There is no redundant computation available in the FIR filter, real-time implementation of a large order FIR filter in a resource constrained environment is a challenging task. Filter coefficients very often remain constant and known *a* prioriin signal processing applications. This feature has been utilized to reduce the complexity of realization of multiplications. FIR filter has two maintaining the Integrity of the Specifications configurations, namely direct form FIR filter and transposes form FIR filter.

Several designs have been designed by various researchers for efficient realization of FIR filters (having Fixed coefficients) using multiple constant multiplication (MCM) and distributed arithmetic (DA) [6] and methods [7]. DA-based designs use lookup tables (LUTs) to store pre-computed result stored the computational complexity.

The Transpose form FIR filter only needs N delay units, where N is the order of the filter – potentially half as much as direct form. This structure is obtained by reversing the order of the numerator and denominator sections of Direct Form, since they are in fact two linear systems. Then, one will notice that there are two columns of delays that tap off the center net, and these can be combined since they are redundant. The disadvantage is that Transpose form increases the possibility of arithmetic overflow for filters of high Q or resonance. This is because, conceptually, the signal is first passed through an all-pole filter (which normally boosts gain at the resonant frequencies) before the result of that is

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saturated, then passed through an all-zero filter (which often attenuates much of what the all-pole half amplifies). In this paper, we realize the possibility of block FIR filter in transpose form configuration to take advantage of the MCMtechnique and the naturally pipelining for area delay efficient realization of large order. The main contributions of this paper are as follows.

1. The Computational analysis of transpose form FIR filter and derivation of flow graph with reduced register complexity.
2. Block formulation for transpose form FIR filter.
3. Design of transpose form FIR filter block for reconfigurable applications
4. A low-complexity design method using multiple constant multiplications technique for the block implementation of fixed FIR filters.

II. EXISTING SYSTEM

In [2] authors used average residual battery level of the entire network and it was calculated by adding two fields to the RREQ packet header of a on-demand routing algorithm i) average residual battery energy of the nodes on the path ii) number of hops that the RREQ packet has passed through.According to their equation retransmission time is proportional to residual battery energy. Those nodes having more battery energy than the average energy will be selected because its retransmission time will be less. Small hop count is selected at the stage when most of the nodes have same retransmission time. Individual battery power of a node is considered as a metric to prolong the network lifetime in [3]. Authors used an optimization function which considers nature of the packet, size of the packet and distance between the nodes, number of hops and transmission time are also considered for optimization. In [4] initial population for Genetic Algorithm has been computed from the multicast group which has a set of paths from source to destination and the calculated lifetime of each path. Lifetime of the path is used as a fitness function. Fitness function will select the highest chromosomes which is having highest lifetime. Cross over and mutation operators are used to enhance the selection. In [5] authors improved AODV protocol by implementing a balanced energy consumption idea into route discovery process. RREQ message will be forwarded when the nodes have sufficient amount of energy to transmit the message otherwise message will be dropped. This condition will be checked with threshold value which is dynamically changing. It allows a node with over used battery to refuse to route the traffic in order to prolong the network life. In [6] Authors had modified the route table of AODV adding power factor field. Only active nodes can take part in rout selection and remaining nodes can be idle. The lifetime of a node is calculated and transmitted along with Hello packets. In [7] authors considered the individual battery power of the node and number of hops, as the large number of hops will help in reducing the range of the transmission power. Route discovery has been done in the same way as being done in on-demand routing algorithms. After packet has been reached to the destination, destination will wait for time δt and collects all the packets. After time δt it calls the optimization function to select the path and send RREP. Optimization function uses the individual node's battery energy; if node is having low energy level then optimization function will not use that node.

III. DRAWBACKS

- It provides only block performances.
- High delay.
- Occupies high area Units.

IV. PROPOSED SYSTEM

The proposed structure for block FIR filter is shown in Figure for the block size L = 4. It consists of one coefficient selection unit (CSU), one register unit (RU), M number of inner product units (IPUs), and one pipeline adder unit (PAU). The CSU stores coefficients of all the filters to be used for the reconfigurable.

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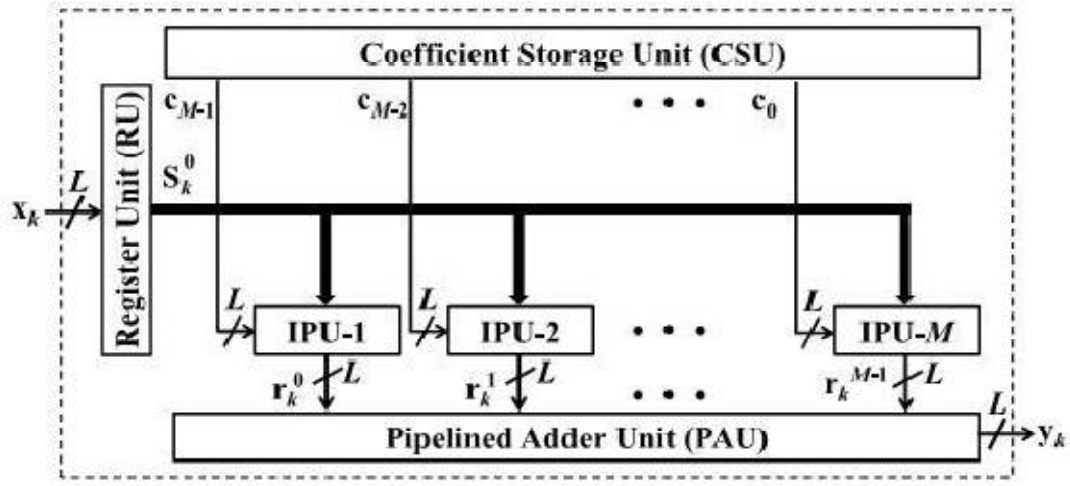
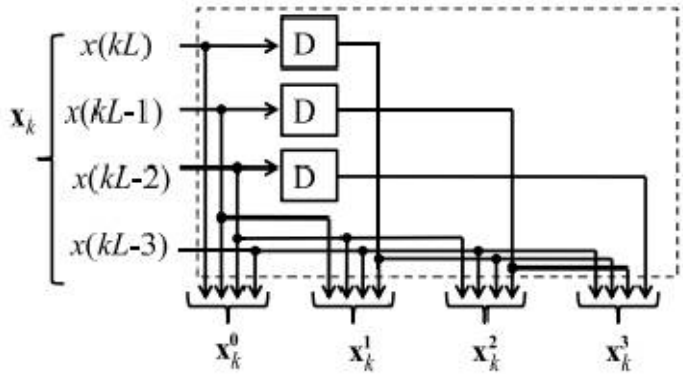
Application. It is implemented using N ROM LUTs, such that filter coefficients of any particular channel filter are obtained in one clock cycle, where N is the filter length. The RU receives xk during the kth cycle and produces L rows of S0 k in parallel. L rows of S0 k are transmitted to M IPUs of the proposed structure. The M IPUs also receive M short-weight vectors from the CSU such that during the kth cycle, the (m + 1) th IPU receives the weight vector cM−m−1 from the CSU and L rows of S0 k form the RU. Each IPU performs matrix vector product of S0 k with the short-weight vector cm, and computes a block of L partial filter outputs (rm k). Therefore, each IPU performs L inner-product computations of L rows of S0 k with a common weight vector cm. In each cycle, the proposed structure receives a block of L inputs and produces a block of L filter outputs, where the duration of each cycle is T = TM + TA + TFA log2 L, TM is one multiplier delay, TA is one adder.



Fig

Fig.1 Proposed structures



(a)

Fig.1 (a) Structure of RU

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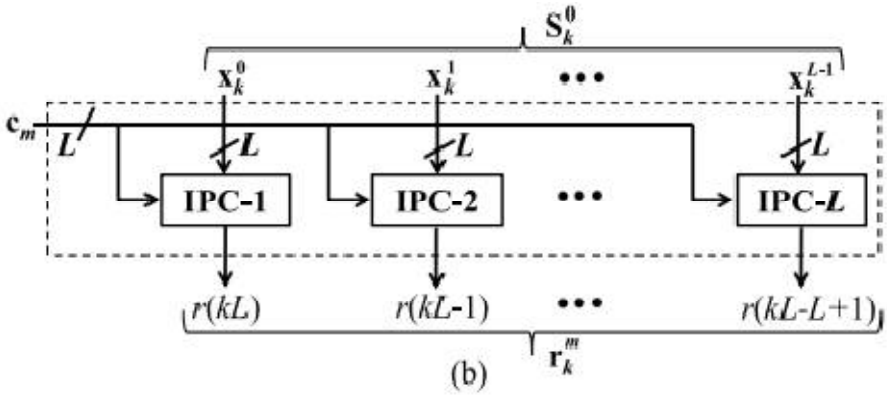

Fig.1 (b) Structure of (m+1) IPU

V. MCM-BASED IMPLEMENTATION OF FIXED-COEFFICIENT FIR FILTER

We discuss the derivation of MCM units for transpose form block FIR filter, and the design of proposed structure for fixed filters. For fixed-coefficient implementation, the CSU is no longer required, since the structure is to be tailored for only one given filter. Similarly, IPUs are not required. Those multiplications are required to be mapped to the MCM units for a low-complexity realization. In the following, we show that the proposed formulation for MCM-based implementation of block FIR filter makes use of the symmetry in input matrix **S**0*k* to perform horizontal and vertical common sub expression elimination [17] and to minimize the number of shift-add operations in the MCM blocks.

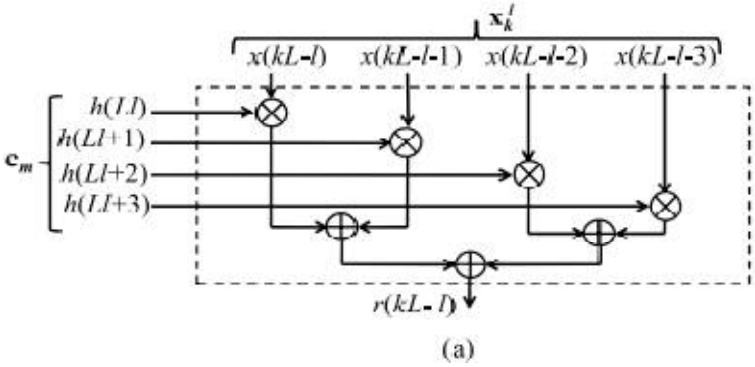

Fig.2 (a) Internal structure of (l + 1)th IPC for L = 4.

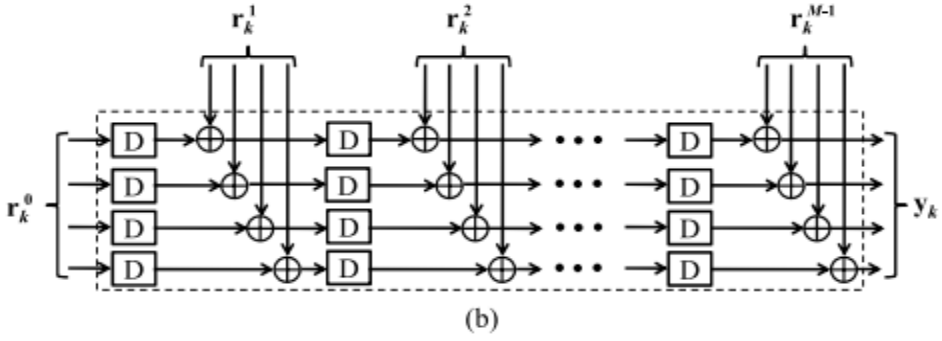

Fig.2 (b) Structure of PAU for block size L = 4.

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Is no longer required, since the structure is to be tailored for only one given filter. The recurrence relation can be expressed as Y (z) = z−1 ··z−1 (z−1rM−1 +rM−2 +rM−3) ···+r1+r0. Where R =S0 k ·C Similarly, IPUs are not required. The multiplications are required to be mapped to the MCM units for a low complexity realization. In the following, we show that the proposed formulation for MCM based implementation of block FIR filter makes use of the symmetry in input matrix**S**0*k* to perform horizontal and vertical common sub expression elimination and to minimize the number of shift-add operations in the MCM blocks.

Input matrix

$$\mathbf{R} = \begin{bmatrix} x(4k) & x(4k-1) & x(4k-2) & x(4k-3) \\ x(4k-1) & x(4k-2) & x(4k-3) & x(4k-4) \\ x(4k-2) & x(4k-3) & x(4k-4) & x(4k-5) \\ x(4k-3) & x(4k-4) & x(4k-5) & x(4k-6) \end{bmatrix} \times \begin{bmatrix} h(0) & h(4) & h(8) & h(12) \\ h(1) & h(5) & h(9) & h(13) \\ h(2) & h(6) & h(10) & h(14) \\ h(3) & h(7) & h(11) & h(15) \end{bmatrix}$$

MCM in TRANSPOSE FORM BLOCK FIR FILTER
Of Length = 16 and Block Size = 4

Input sample	Coefficient Group
$x(4k)$	$\{h(0), h(4), h(8), h(12)\}$
$x(4k-1)$	$\{h(0), h(4), h(8), h(12)\}$ $\{h(1), h(5), h(9), h(13)\}$
$x(4k-2)$	$\{h(0), h(4), h(8), h(12)\}$ $\{h(1), h(5), h(9), h(13)\}$ $\{h(2), h(6), h(10), h(14)\}$
$x(4k-3)$	$\{h(0), h(4), h(8), h(12)\}$ $\{h(1), h(5), h(9), h(13)\}$ $\{h(2), h(6), h(10), h(14)\}$ $\{h(3), h(7), h(11), h(15)\}$
$x(4k-4)$	$\{h(1), h(5), h(9), h(13)\}$ $\{h(2), h(6), h(10), h(14)\}$ $\{h(3), h(7), h(11), h(15)\}$
$x(4k-5)$	$\{h(2), h(6), h(10), h(14)\}$ $\{h(3), h(7), h(11), h(15)\}$
$x(4k-6)$	$\{h(3), h(7), h(11), h(15)\}$

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As shown in Table I, MCM can be applied in both horizontal and vertical direction of the coefficient matrix. The sample $x(4k-3)$ appears in four rows or four columns of the following whereas $x(4k)$ appears in only one row or one column Therefore, all the four rows of coefficient matrix are involved in the MCM for the $x(4k-3)$, whereas only the first row of coefficients are involved in the MCM for $x(4k)$. For larger values of N or the smaller block sizes, the row size of the coefficient matrix is larger that results in larger MCM size across all the samples, which results into larger saving in computational complexity.

The proposed MCM-based structure for FIR filters for block size $L = 4$ is shown in Fig. 9 for the purpose of illustration. The MCM-based structure (shown in Fig. 9) involves six MCM blocks corresponding to six input samples. Each MCM block produces the necessary product terms as listed in Table I. The sub expressions of the MCM blocks are shift added in the adder network to produce the inner-product values ($r_{l,m}$), for $0 \le l \le L-1$ and $0 \le m \le (N/L)-1$ corresponding to the matrix product of (14). The inner-product values are finally added in the PAU of Fig. 8(b) to obtain a block of filter output.

VI. HARDWARE AND TIME COMPLEXITIES

The proposed structure for reconfigurable application consists of one CSU, one RU, M IPUs, and one PAU. The CSU consists of N ROM units of P words each, where P is the number of FIR filters to be implemented by the proposed reconfigurable structure. We have excluded complexity of CSU in the performance comparison, since it is common in all the RFIR structures. Each IPU is comprised of L IP cells, where each IP cell involves L multipliers and $(L-1)$ adders. The RU involves $(L-1)$ registers of B-bit width. The PAU involves $(M-1)$ adders and the same number of registers, where each register has a width of $(B+B\_)$, B, and $B\_$ respectively, being the bit width of input sample and filter coefficients. Therefore, the proposed structure involves LN multipliers, $L(N-1)$ adders, and $[B(N-1)+B(NL)]$ (flip flops) FFs; and processes L samples in every cycle.

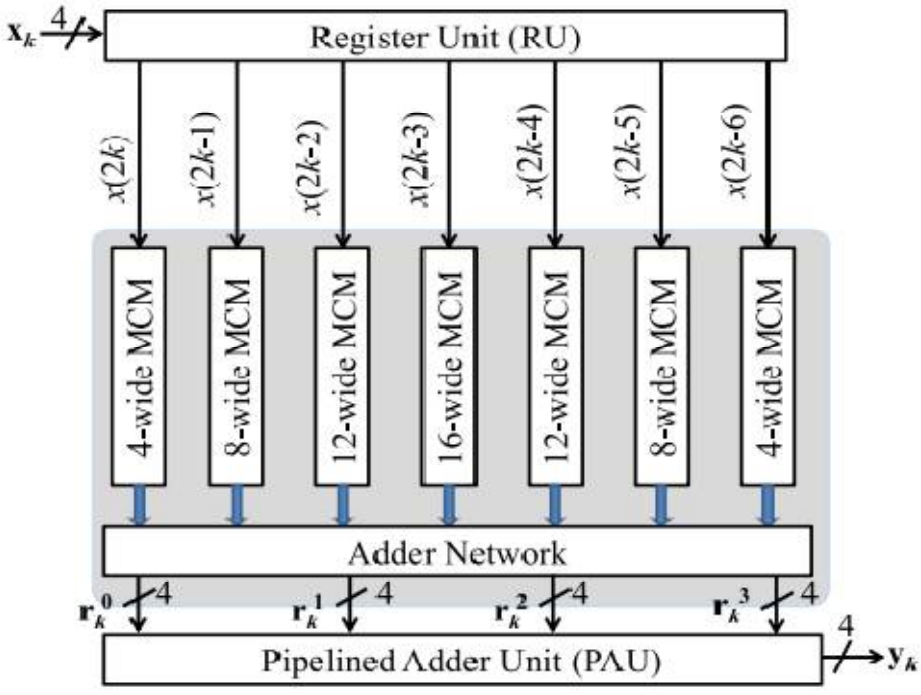

Fig.3 Proposed MCM Structure

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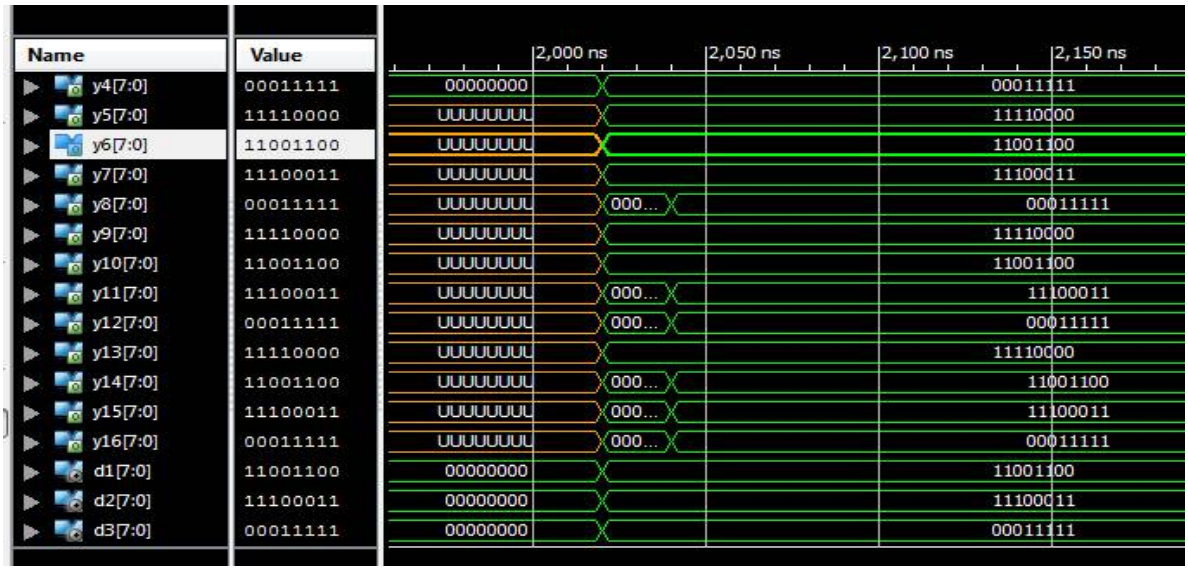
VII. ADVANTAGES

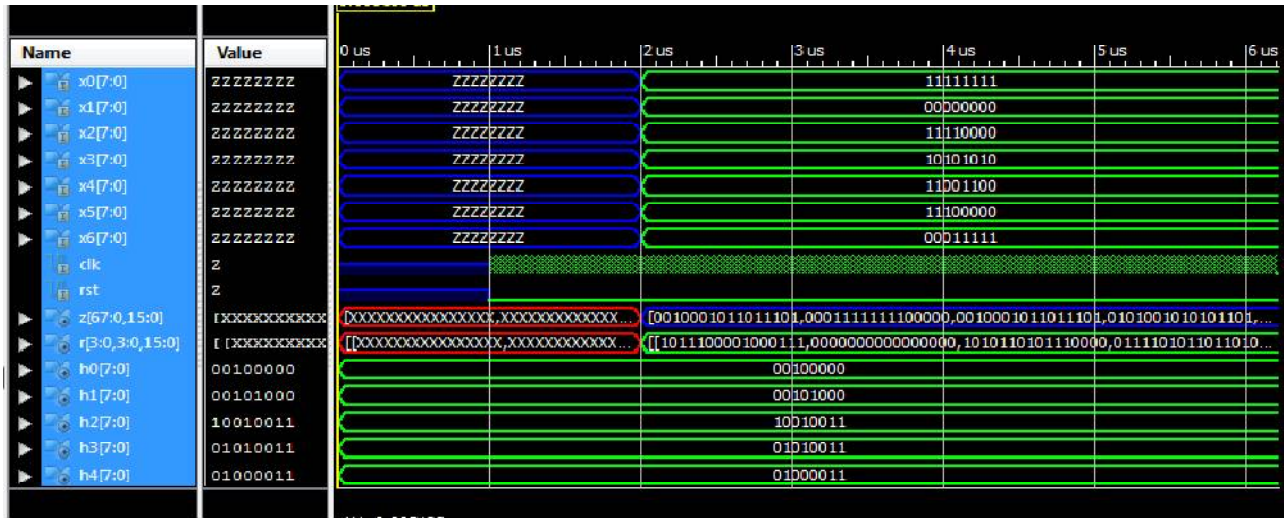
- Block and higher order N processing.
- Less area requirement
- Low delay

VIII. SIMULATION AND DISCUSSION

Experimental Result for fixed FIR Filter



Experimental Result of Reconfigurable FIR Filter



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To implement the fixed and reconfigurable coefficients Transpose form FIR filter is simulated using Xilinx Tool. The area (no. of LUT's and flip-flop's clock buffers and I/O buffers) and delay were analyzed for Fixed and reconfigurable coefficients. From the analysis, it is observed that the area and delay reduced when compare to the direct form FIR filter. In the below simulation result is for Fixed coefficient Transpose form FIR filter with 15 coefficients. The input given to the filter is 0001(1) and the output achieved for the filter is 1010. The delay for the fixed transpose form FIR filter is 1.19 ns. The delay of the fixed transpose form filter is reduced when compare to the direct form filter delay. The delay of the direct form fir filter is 1.35ns.

In the below simulation result is for reconfigurable coefficients Transpose form FIR filter. The input given to the filter is 0001(1) and the coefficients given for the filter is, 0000, 0001, 0010, 0011, 0100, and 0101. The output achieved for the filter is 1111 (15). The total number LUT used for the reconfigurable FIR is 152 and the Flip-flops are 63 and the shift register, clock buffers and I/O buffers are used 27 cells. The LUTs, Flip-flops are reduced when compare to the direct form FIR filter. The delay for the reconfigurable transpose form FIR filter is 1.27 ns. The delay of the fixed transpose form filter is reduced when compare to the direct form filter delay. The delay of the direct form fir filter is 1.35ns direct form filter delay. The delay of the direct form fir filter is 1.36ns.

IX. PERFORMANCE MEASUREMENT

Table 1: comparison table reconfigurable fir for the area and delay

	Delay (ns)	**LUT's and Flip Flop's**
Direct form Reconfigurable FIR	1.35	368
Transpose form Reconfigurable FIR	1.26	241

Table 2: comparison table fixed fir for the area and Delay

	Delay (ns)	**LUT's and Flip Flop's**
Direct form Reconfigurable FIR -	1.36	120
Transpose form Reconfigurable FIR	1.198	60

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X. CONCLUSION

In this paper, we implemented the design of Transpose form FIR filter for fixed coefficient and reconfigurable coefficients. The transpose form FIR filter is naturally a pipelined structure which supports the multiple constant multiplications (MCM) technique. The implementation of MCM technique is easier in fixed coefficient Transpose form FIR filter but complex in reconfigurable coefficients. In fixed coefficients transpose FIR filter, area and delay are reduced by using MCM technique. The low-complexity design using the MCM technique is implemented for fixed coefficients transpose form FIR filters and multiplier-based design is used for reconfigurable transpose form FIR filter. The implemented transpose form FIR filter structure achieved less area and delay than the direct-form FIR filter structure. In future, the delay and area will be further reduced in transpose form FIR filter by applying another technique.

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