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FPGA based OFDM System Implementation using FFT

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ABSTRACT: Orthogonal Frequency Division Multiplexing (OFDM) is a multicarrier system which modulate and multiplex the data. The system designed results in optimal usage of bandwidth and resistant to multipath effects. In this paper the OFDM system is implemented using FFT/IFFT on FPGA kit. The coding of this OFDM system is done in VHDL language and simulation is done on XILINX ISE software.

KEYWORDS: FFT, IFFT, butterfly structure, complex multiplier.

I. INTRODUCTION

Orthogonal Frequency Division Multiplexing is a different case of multicarrier transmission. Multiplexing is applied to independent signals but these independent signals are the part of single signal in OFDM. In OFDM, the signal itself is first split into independent channels, modulated by data and then re-multiplexed to create the OFDM carrier. OFDM is a technique which is convenient for wireless communication due to its resistance to inter-symbol interference (ISI) and inter-carrier interference (ICI) [1].

In the new era of communication, Orthogonal Frequency Division Multiplexing (OFDM) is a main modulation method. The total signal bandwidth in a conventional parallel data system can be divided into N non-overlapping frequency sub-channels. Independent symbol modulate individual sub-channel and then the N sub-channels are frequency multiplexed. Spectral overlap is avoided to eliminate the inter-carrier interference (ICI), i.e. between two adjacent sub-channels, empty spectral region is provided. But this results in poor usage of the ready spectrum. To deal with this wastefulness, through the improvement of frequency division multiplexing (FDM) with coincidental sub-channels. The sub-channels were organized so that, the sidebands of the individual carriers overlap without generating ICI. To obtain this, the carriers must be mathematically orthogonal. From this confinement the perception of Orthogonal Frequency Division Multiplexing (OFDM) was proposed [2].

II. RELATED WORK

An OFDM Transmitter Implementation paper using Cordic based Partially Reconfigurable IFFT Module by Arun Kumar K A describes in the advancement of modern-era wireless communication systems, reconfigurable technology plays a critical duty. OFDM is a method in which is wireless communication in practice and in this digital data is encoded in big number of closely separated orthogonal sub-carrier signals. The Baseband FPGA execution of an OFDM transmitter is also discussed in this paper. The module is executed using a method called partial reconfiguration so that someone can swap between distinct modulation techniques, coding techniques and number sub-carriers demanded in less time. In this execution the person which is using it can exchange between four OFDM transmitters in less than a minute without troubling the standard working of the module. In this PR based execution of OFDM Transmitter a greater area of the Modulator, coding and IFFT modules will be static and a lesser area will be dynamic.

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At the time of swapping only the dynamic area of the FPGA is reconfigured in less time which will decrease power and configuration time [3].

Mujtaba Afzal, Dayal Sati, HeenaChoudhary, Ashish Vats and RomikaChoudhary in the Design, Modelling and Implementation paper of Variable FFT Processor explained about the research which concentrates on the planning, Modeling and execution of inconsistent FFT Processor. In orthogonal frequency division multiplexing (OFDM) and OrthogonalFrequency-Division Multiple Access (OFDMA) techniques important block is Fast Fourier transform (FFT). Fromwired-communication to wireless-communication modems, Wi-Fi, IEEE802.16, Wi-MAX or 3GPP longterm evolution (LTE), digital subscriber lines (xDSL), process baseband data, OFDM is having large applications. Initially the design is constructedfor 8 point FFT and then it is used to execute variable FFT processor. The design is created with the support ofVHDL programming language and combined on Virtex-5 FPGA in Xilinx 14.2 software and functional simulation isdone in Modelsim software [4].

In FPGA Implementation of MIMO-OFDM Transceiver paper of K. Srinandhini and V. Vaithianathan, they explained Orthogonal Frequency Division Multiplexing (OFDM). FDM modulation is a guaranteed process for high data rate applications such as video streaming. This technique works efficiently for multipath frequency selective channels. Multiple Input and Multiple Output (MIMO) is a wireless technology which uses number of antennas at the transceiver terminals. Link throughput and network capacity it increases. The combination of both MIMO and OFDM gives a module that is robust against the frequency-selective fading which is due to sever multi-path scattering and narrowband interference. This judgment has accelerated the enhancement of System-onchip (SoC) platform to help the physical layer of these techniques. Field Programmable Gate Array (FPGA) execution of channel coder, decoder, interleaver and deinterleaver which is of MIMO-OFDM are explained in this paper. Convolutional encoder of code rate 112 is used because of its minimum complexity and Viterbi decoder is used for decoding. Interleaver and Deinterleaver is used to delete the burst error thus enhancing the performance [5].

III. PROPOSED ALGORITHM

A. *Modulator (QAM):*

Quadrature Amplitude Modulator (QAM) transfers data by changing few form of a carrier signal, or the carrier wave, (usually a sinusoid) in reply to a data signal, like all modulation techniques. The amplitude of two same frequency signals, 90° out-of-phase with each other (in quadrature) are modulated to represent the data signal, in the case of QAM.

B. *Serial to Parallel and Parallel to Serial Converter*

The bit streams are input to the serial to parallel converter and the parallel to serial converter is at the output side as shown in the block diagram of OFDM. One register 'temp' is taken for temporary holding of data and after n number of clock cycles, the value in 'temp' is allotted to the output register. Similarly, in parallel to serial converter, for every clock cycle, least significant bit (LSB) of input is allotted to output and his input number is right shifted by one place. In this way, we get LSB at output, for every clock cycle.

C. *FFT and IFFT*

To calculate discrete Fourier transform there is an algorithm named as a fast Fourier transform (FFT). And because of a Fourier transform, conversion of time domain signal into frequency domain signal is possible. Thus FFT is used in a great extent in DSP method, also in applications of communication in greater extent. FFT is essential and widely used numerical algorithm [4]. In the field of digital signal processing as well as image processing FFT is one of the rudimentary operations. Use of FFT is necessary in most of the signal processing applications [6]. There are efficient multiplication methods to minimize the partial product which is happened in conventional multiplication method therefore the FFT and inverse fast Fourier transform (IFFT) with efficient multiplication and with greater speed is used and important for Orthogonal Frequency Division Multiplexing (OFDM) Modulator and Demodulator [7]. High speed and efficient multiplication is required in most of the applications. And therefore conventional multicarrier method are mostly selected, but this gives results in lower spectrum efficiency [8]. Hence, the principles of OFDM are important. The speed enhancement is the useful contribution of the main processing blocks in OFDM system [9]. FFT is used for demodulation and it is exactly opposite to IFFT.

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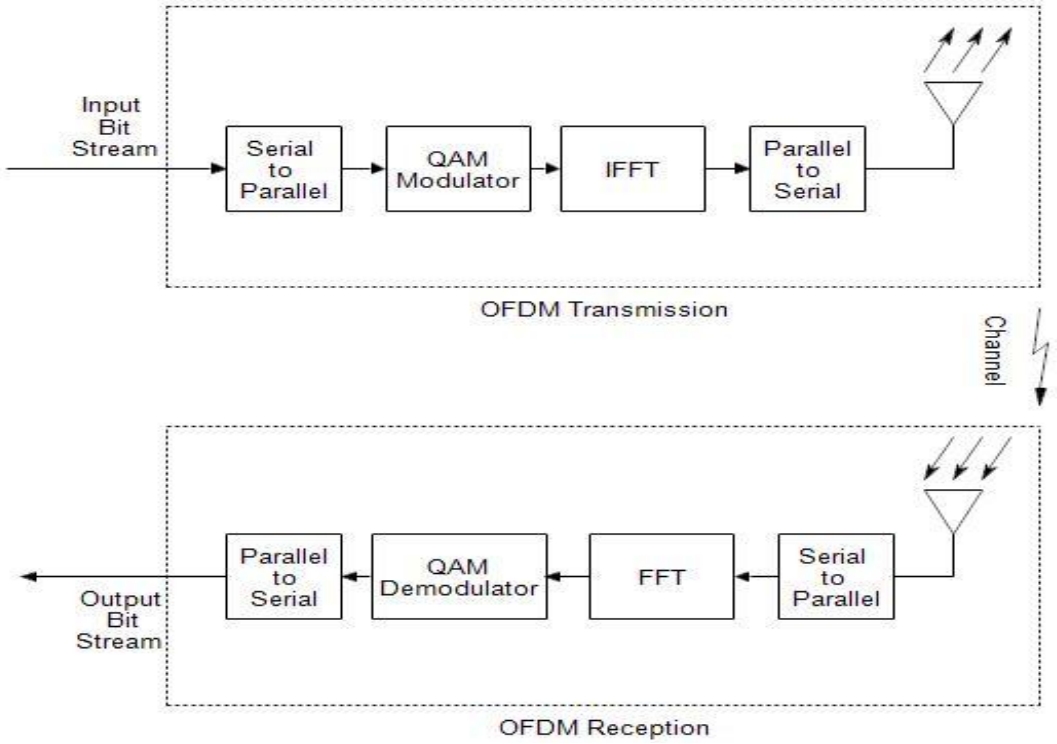

Fig.1 OFDM Block Diagram

IV. SIMULATION RESULTS

All VHDL design in this dissertation work was performed in the Xilinx ISE (IntegratedSoftware Environment) version 13.2 for Windows. ISE combines a VHDL text editor, IP core support, behavioral simulation, and synthesis support in one program. The primary challenge in writing the VHDL components is translating the software operations of each module in OFDM, into digital logic for hardware.

OFDM transmitter has 4 blocks such as Serial to Parallel Converter, Modulator, IFFT and Parallel to Serial Converter. In serial to parallel converter, which is input block of OFDM transmitter and receiver, data is taken in serial form and converted to parallel form. For this purpose, one register `temp' is considered for temporary storage of data and after n number of clock cycles, the value in `temp' is assigned to the output register. Similarly, in parallel to serial converter, for every clock cycle, least significant bit (LSB) of input is assigned to output and this input number is right shifted by one place. In this way, for every clock cycle, we get LSB at output.Fig.2 and Fig.3 shows the serial to parallel and parallel to serial converter respectively.

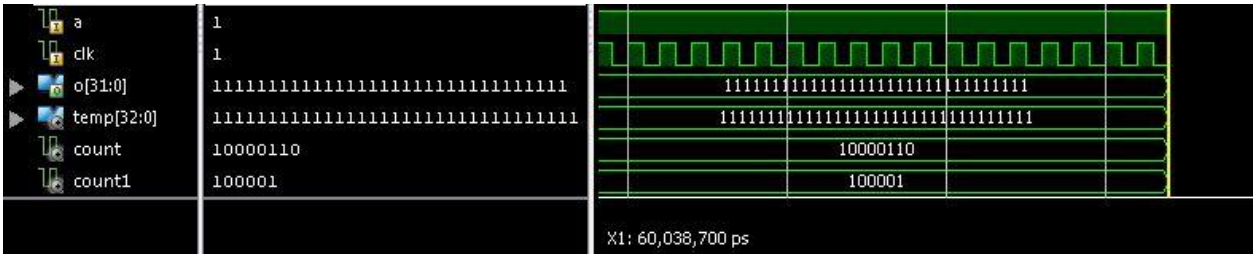

Fig.2 Simulated Output of Serial to Parallel Converter

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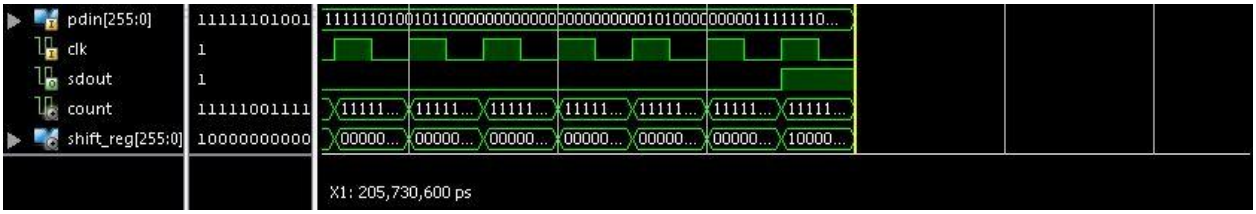

Fig.3 Simulated Output of Parallel to Serial Converter

Presented system uses QAM modulation so 16 constellation points are used. To have different constellation values data is divided in groups of 4 bits each and convert that binary code to gray code for better accuracy. Higher two bits are used to specify imaginary number and lower two bits are used for real number.In this modulation scheme, bit combination 00 corresponds to -3, 01 corresponds to -1, 11 corresponds to +1, 10 corresponds to +3. To achieve this, a separate process is written in VHDL code. Output of 16-QAM block applied to IFFT block. Fig.4 shows block diagram of 16-QAM.

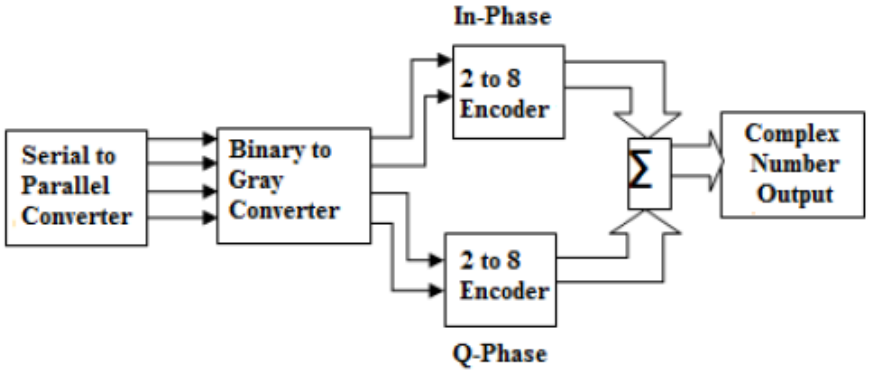

Fig.4 16-QAM Block Diagram

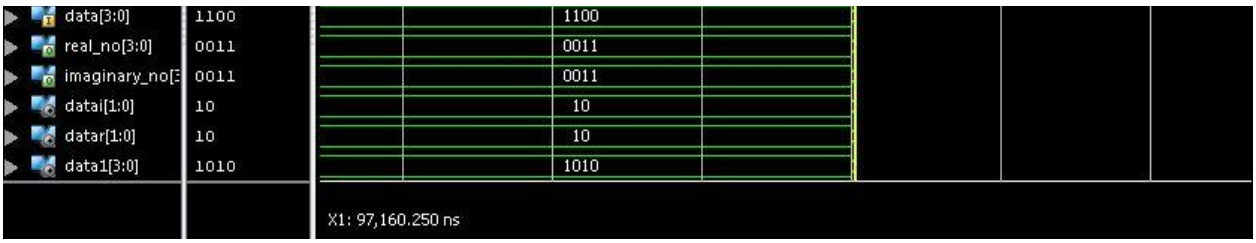

Fig.5 Simulated Output of QAM

As shown in Fig.5, data[3:0] 1100 is input and it is in binary form. Firstly data in binary form is converted in gray code and we get data1[3:0] 1010. Two Bits at the MSB side will give ous imaginary number and remaining two bits gives ous real number. In this way we will get complex number from real and imaginary number which is input to the IFFT. FFT and IFFT maintains the orthogonality in OFDM. To implement FFT on FPGA using VHDL, an algorithm was developed. A stepwise implementation of buttery diagram is done, in this algorithm.

During computation of N point IFFT/FFT, $(N/2)\ log_2 N$ complex multiplications and $N\ log_2 N$ complex additions are required to be performed. So, for 8 point IFFT/FFT, there is a requirement of 12 complex multiplications and 24 complex additions. All complex multiplications are between, the twiddle factors and output of butterfly unit. But in actual, only 5 complex multiplications are required; remaining all are avoided because twiddle factor W_4^0 is equal to 1. One complex multiplication consists of 4 simple multiplications and 2 simple additions. So, if we can reduce number of

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complex multiplications required, then we can save required resources. In our proposed 8 point IFFT/FFT, only 2 complex multiplications are required to be performed i.e. with twiddle factor W_4^1 *and* W_4^3. And also, for these two complex multiplications, only 4 simple multipliers and 7 simple adders are required. Remaining 2 complex multiplications with W_4^2 can be performed, by simple mathematical operations such as taking negation of a number, exchanging real and imaginary part of a complex number. This results in lot of resource saving.

FFT of constellation array is obtained in 3 stages, as shown in Fig.6. As FFT is performed in stages using butterfly module, in the same way, the VHDL code also does it in 3 stages. In first stage, no complex multiplication is required, only complex addition and subtraction is needed. For one complex addition, two simple additions are required. Input data to FFT are added and subtracted, as per the shown in butterfly diagram. For multiplication by -1, just take 2's complement of the number. It will reduce usage of the multiplier block.

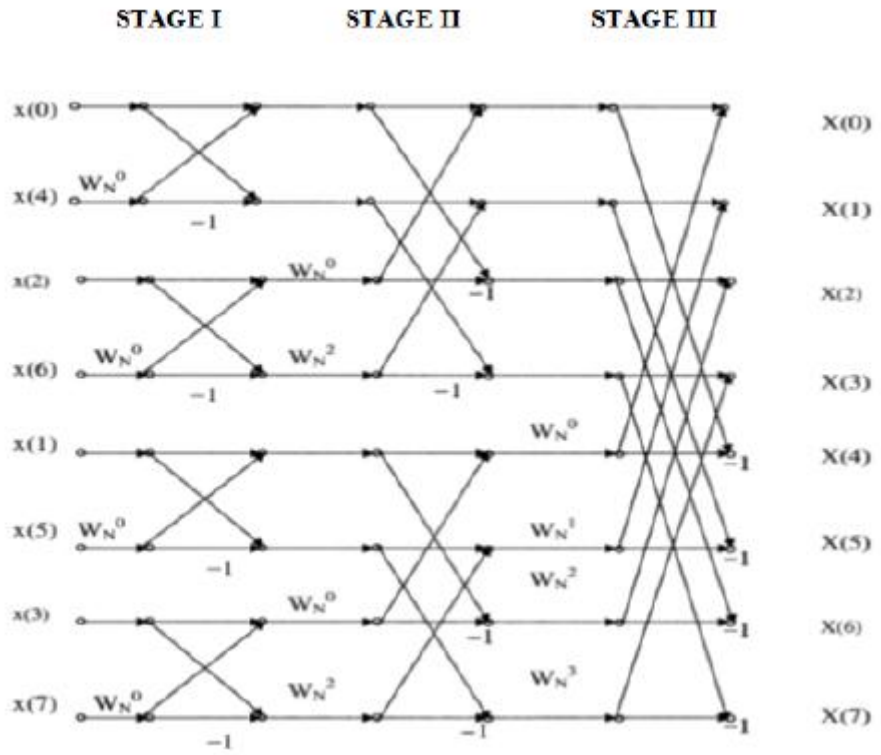

Fig.6 Decimation-In-Time FFT

In this technique, for multiplication with twiddle factor $W^1 = 0.707 - j\,0.707$ i.e.181-181j, only 2 simple multiplications are required. For this, multiply real and imaginary part of complex number, to be multiplied, with 181. We can get the final complex multiplication answer, by simple operations like taking negation and addition of simple multiplication outputs. We have to apply, similar method for multiplication with twiddle factor W^3.

In third stage, complex multiplication only with W^2 is required. And this can be avoided by simple mathematical operations. After complex multiplications, add/sub operations are performed according to butterfly diagram and the result is ready. Fig.7 and Fig.8 shows IFFT Input and IFFT Output respectively.

In this way, for implementing FFT using proposed technique, requirement is of only 4 multipliers whereas by normal method, it will require 20 multipliers. Thus, for FFT/IFFT implementation, by proposed technique, we can save multipliers up to 80%. Multiplier requires much resources and more power. Thus, much of the resources can be saved.

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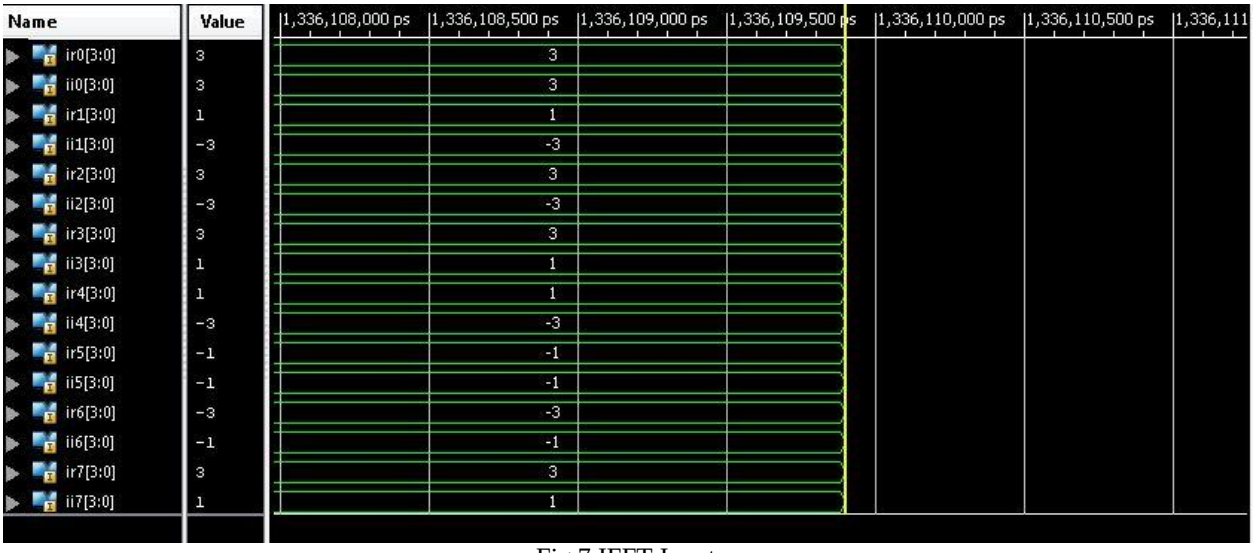

Fig.7 IFFT Input

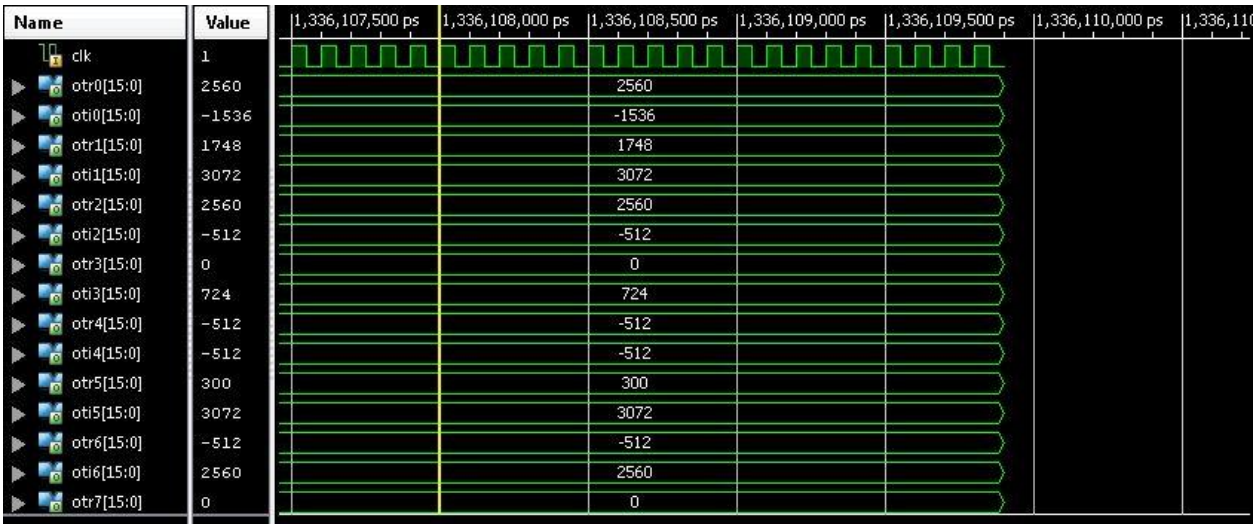

Fig.8 IFFT Output

V. CONCLUSION AND FUTURE WORK

The 8 point FFT implementation in Orthogonal Frequency Division Multiplexing (OFDM) is proposed. In OFDM system, IFFT/FFT blocks are used to provide orthogonality between the successive channel sub-careers. In regular frequency division multiplexing, multi-carrier approach is used. Between each channel, guard bands are provided to avoid the interference. But in OFDM, overlapping carriers are used. Each pair of successive carriers of the sub-channel is orthogonal to each other. For this purpose FFT and IFFT blocks are used. The conventional OFDM is implemented in FPGA. This project contributes the implementation of 8-point FFT using VHDL. The system is designed and simulated using XILINX ISE.

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