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# Design of Reconfigurable Interpolation Filter Architecture

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**ABSTRACT**: Interpolatoris used in digital signal processing (DSP) systems to increase the sampling rate digitally. It comprises an up-sampler and an anti-imaging (interpolation) filter. The up-sampler change the sampling rate of base-band signal, while the interpolation filters suppress the undesired interference effect resulted due to up-sampling the base-band signal. The interpolation filter computation is analyzed for different up-sampling factors. This analysis identify the redundant computations which are eliminated by the use of partial results. A block-formulation is presented to share the partial results for parallel computation of filter outputs of different up-sampling factors. The parallel reconfigurable architecture for the interpolation filter is expected to have reduced complexity and reduced number of registers. The reconfigurable architecture is mainly used in software defined radio (SDR) application. A single interpolation filter in SDR application consume large amount of resource. So a reconfigurable Finite Impulse Response (FIR) interpolation filter is the most appropriate for a resource and power constrained multi-standard SDR receiver which could support different up-sampling factors as well as filter specifications. Thus the use of multiple filters can be replaced efficiently by the use of a single reconfigurable interpolation filter. To validate the design, input is extracted with the help of MATLAB R2010a, codes can be developed using Verilog HDL in Xilinx ISE Design Suite 14.2 and to be simulated in ISimISE O.61xd Simulator.

**KEYWORDS**: Interpolation filter; up-sampling; Reconfigurable; Redundant; digital up- converter; SDR.

## I. INTRODUCTION

Digital Signal Processing (DSP) refers to various techniques for improving the accuracy and reliability of digital communications. The theory behind DSP is quite complex. Basically, DSP works by clarifying, or standardizing, the levels or states of a digital signal. All communications circuits contain some noise. This is true whether the signals are analog or digital, and regardless of the type of information conveyed. Noise is the eternal bane of communications engineers, who are always striving to find new ways to improve the signal-to-noise ratioin communications systems. In signal processing, a filter is a device or process that removes some unwanted components or features from a signal. Filtering is a class of signal processing, the defining feature of filters being the complete or partial suppression of some aspect of the signal. Most often, this means removing some frequencies and not others in order to suppress interfering signals and reduce background noise. However, filters do not exclusively act in the frequency domain; especially in the field of image processing many other targets for filtering exist. Correlations can be removed for certain frequency components and not for others without having to act in the frequency domain.

Many signal processing applications require the parameters of the digital filter to be dynamically varied. Such on-the-fly reconfigurable digital filters are useful in adaptive systems, radar, sonar and control systems, biomedical signal processing, vibration analysis, audio signal processing, and wireless communications.

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One of the simplest methods to realize a reconfigurable filter is to use a programmable (or reloadable, i.e., variable coefficient) filter in which the filter coefficients corresponding to various $f_c$ (cutoff frequency) values are stored in the memory, and appropriate coefficients are loaded into the filter structure as per the desired $f_c$. Disadvantages of this method are: 1) huge memory requirement to store all the filter coefficients corresponding to all the desired $f_c$values, 2) large number of variable parameters (dependent on filter length), and 3) large number of memory access operations required every time when filter needs to be reconfigured. Considering these disadvantages more efficient methods have been identified for the design of programmable or reconfigurable digital filters. Sampling rate of a digital filter is an important parameter that determines the performance of a digital filter. In signal processing, sampling is the reduction of a continuous signal to a discrete signal. A common example is the conversion of a sound wave (a continuous signal) to a sequence of samples (a discrete-time signal). Sampling can be done for functions varying in space, time, or any other dimension, and similar results are obtained in two or more dimensions. Reconstructing a continuous function from samples is done by interpolation algorithms. In multirate digital signal processing the sampling rate of a signal is changed in order to increase the efficiency of various signal processing operations. Decimation, or down-sampling, reduces the sampling rate, whereas expansion, or up-sampling, followed by interpolation increases the sampling rate.
Interpolator is used in digital signal processing (DSP) systems to increase the sampling rate digitally. It comprises an up-sampler and an anti-imaging (interpolation) filter. The up-sampler change the sampling rate of base-band signal, while the interpolation filter suppresses the undesired interference effect resulted due to up-sampling the baseband signal. Pulse shaping filters (PSFs) like root raised cosine (RRC) filter is commonly used as interpolation filter due to its high inter-symbol interference (ISI) rejection ratio and high bandwidth limitation criteria . Interpolation filter has a different coefficient-vector for different up-sampling factors of a base-band signal. Software defined radio (SDR) technology enables for digital implementation of wide band trans receivers of multi-standard wireless communications. A multi-standard SDR system involve interpolators with different filter coefficients, filter-lengths and up-sampling factors to meet the stringent frequency specifications of different communication standards. For example: Universal Mobile Telecommunication Standard (UMTS) uses interpolators with interpolation factors (4, 8, and 16), and filter lengths (25, 49, 97), respectively. A SDR receiver consumes huge amount of resource when these interpolators are implemented individually in a hardwired circuit.

Software defined radio include mainly the high frequency application. SDR include those applications where the hardware complexity is more and required features are obtained by software updation. A reconfigurable finite impulse response (FIR) interpolation filter is the most appropriate for a resource and power constrained multi-standard SDR receiver which could support different up-sampling factors as well as filter specifications.

## II. RELATED WORK

Many digital processing applications require the need of reconfigurable digital filter for their efficient performance. In such a case there are several techniques to design an efficient reconfigurable digital filter. In the reconfigurable frequency response masking (FRM) technique [13], each of the delay elements of the filter structure is replaced by $M$ delays and reconfigurability is achieved using appropriate value(s) of $M$. It is an efficient way of designing low complexity narrow *tbw* variable filter. In the coefficient decimation (CDM) technique [14], impulse response of the filter is modified either by replacing (by zero) or by discarding the filter coefficients other than every $D_{th}$coefficient. Interpolation and CDM based variable filters are easy to reconfigure (as the values of $M$ and $D$ can be easily varied by using multiplexers) and have very low complexities; however the discrete nature of the controlling parameters results in only coarse control over $f_c$. Fast filter bank (FFB) based filter in [15] has very wide $f_c$ range and narrow *tbw*at very low complexity. However, its group delay is very large and it offers only *discrete* control over $f_c$. All-pass transformation and frequency transformation based methods provide *continuous* control over $f_c$ at the cost of increase in the complexity of the filter structure. An all-pass transformation based filter [16] is realized by replacing each unit delay in the prototype filter structure by an all-pass structure. However, even though the prototype filter is a linear-phase filter, the resultant filter is not a linear-phase filter. Frequency transformation based filters [17], [18] retain the linear phase property of the prototype filter. However, they have limited $f_c$ range and/or the *tbw*of the frequency transformed filter is significantly wider than that of the prototype filter. The reconfigurable filter based on the combination of second-order

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frequency transformations and the interpolation technique (ISFT filter) [19] has very wide $f_c$ range (approximately equal to Nyquist band) and narrow *tbw*.

A programmable FIR filter allows us to modify the filter coefficients while the filter is operating. Hence, some low cost implementations that require special coding of filter coefficients, such as the Canonical Signed Digit (CSD) representation, distributed arithmetic**,** and memory based approaches, are not suitable for programmable filters because coding of coefficients is difficult to accomplish in real time. To implement programmable filters, one multiplier and one adder are needed for each tap. Hence, Multiplier-and Accumulator (MAC) based architectures are frequently adopted for programmable filters. However, the cost of multipliers is high and they are not suitable for high-order filters. Due to their simplicity in implementation FIR filters with powers of- two coefficients, which are often referred to as 2PFIR filters have received considerable attention in digital signal processing. By employing only those coefficients that are sums and differences of signed powers-of-two, each multiplication in 2PFIR filtering can be replaced with simple shift-and-add operations. Realization of a programmable 2PFIR filter is considerably more difficult than that of a fixed filter, because it requires programmable shifters such as barrel shifters, shift registers and pre shifters, which greatly increase the hardware complexity or slacken the processing speed. In Low-Power Digit-Based Reconfigurable FIR Filter, due to a wide range in the filter coefficient precision for different applications, it is next to impossible to achieve reconfigurability without incurring overhead in hardware. As an example, a binary pseudorandom number (PN) code matched filter, which is an important block in CDMA receivers, requires only 1-bit coefficient precision while a pulse-shaping filter may require as high a coefficient precision as 16 bits. Since the tap complexity in these two cases can be very different, the reconfigurable FIR filter is quite inefficient. So we adopt the finest granularity for filter implementation and propose a reconfigurable FIR filter architecture with extreme flexibility. With this architecture, both the tap number and the number of nonzero digits in each tap can be arbitrarily assigned given that enough hardware resource is available. Techniques that yield an FIR filter with the minimum total number of CSD for a given frequency response specification can be found in and a software program has been developed. The filter implemented with the architecture can be easily configured as a matched filter, a pulse-shaping filter, or other filters. Furthermore, the FIR architecture also has scalability, modularity, and cascadability, making it amenable to VLSI implementation. Last but not least, the critical path delay in the architecture stays quite invariant in different filter configurations.

Apart from low complexity, reconfigurability is another key requirement of channel filters in SDRs because the filter specifications change in accordance to the selected communication mode. The architecture was independent of the number of taps because the number of taps and non-zero digits in each tap were arbitrarily assigned. But the existing architecture demanded huge hardware resources, which makes the method infeasible for resource-constrained SDR applications. A high-speed and programmable CSD based FIR filter was analyzed. This architecture consisted of a programmable CSD based Booth encoding scheme, a partial product Wallace adder tree and a carry look ahead adder at the last stage. The existing method in always resulted in high speed but there was no consideration for reducing power consumption.

## III.INTERPOLATION FILTER

Interpolator is used in digital signal processing (DSP) systems to increase the sampling rate digitally. It comprises an up-sampler and an anti-imaging (interpolation) filter. The up-sampler change the sampling rate of base-band signal, while the interpolation filter suppress the undesired interference effect resulted due to up-sampling the base-band signal Pulse shaping filters (PSFs) like root raised cosine (RRC) filter is commonly used as interpolation filter due to its high inter-symbol interference (ISI) rejection ratio and high bandwidth limitation criteria . Interpolation filter has a different coefficient-vector for different up-sampling factors of a base-band signal. During the last decade, several multiplier and multiplier-less designs have been suggested for efficient hardware realization of reconfigurable FIR filters and filter-banks for SDR channelization.

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A few multiplier-less designs are proposed for interpolation filter. Symmetric property of PSF and a LUT decomposition scheme are used to reduce the area complexity of 1:4 interpolation filter. In addition to this, LUT sharing of in-phase and quadrature-phase filters are used to save LUT words which offers a significant saving in area complexity of the interpolation filter. Both these designs cannot be reconfigured for up-sampling factor other than 4, and for different filter specifications. A distributed arithmetic (DA)-based reconfigurable FIR interpolation filter architecture is proposed in . The DA-LUT stores partial results of all the sub-filter outputs of interpolation filter with three different interpolation factors. Therefore, the structure requires a large size DA-LUT which is not favorable for single chip realization.

With this assumption, the input-matrix of the reconfigurable interpolation filter only resizes when changes. For example: the size of the input-matrix of an interpolation filter for filter length and up-sampling factors , 4 and 8, are respectively, (2 X 8), (4 X 4), and (8X 2). Due to resize of the input-matrix, the number of sub-filters of an interpolation filters changes with the column size of the input-matrix where the length of each sub-filter is equal to the size of the row. The number of sub-filters required for reconfigurable interpolation filter for full-parallel realization is equal to the highest up-sampling factor. When a full-parallel reconfigurable interpolation structure is configured for lowest up-sampling factor, then maximum number of sub-filters remain unused in the parallel structure. Similarly, when the full-parallel structure is configured for highest up-sampling factor, then hardware resource of each sub-filter are partially utilized.

Therefore, a full-parallel reconfigurable interpolation filter structure has a low hardware utilization efficiency (HUE). Computation of sub-filters can be folded into a single sub-filter since they have identical computational structure. A folded reconfigurable interpolation filter structure has better HUE than the full-parallel structure. It involves only one sub-filter irrespective of up-sampling factor and computes one sub-filter output per cycle . Therefore, the reconfigurable interpolation filter architectures of uses a folded structure instead of a full-parallel structure. But, the folded interpolation filter structure has one major problem. Its output sampling frequency remains constant irrespective of the up-sampling factor and the input sampling frequency decreases inversely with the up-sampling factor. In other words, the folded structure does not increase the output sampling rate for higher up-sampling factor. Instead of that it decreases the input sampling rate by times. Therefore, the folded reconfigurable interpolation filter architectures are suitable for base-band signals of low sampling frequency. On the other hand, the parallel interpolation filter structure increase the output sampling rate proportionately with , but the structure is not hardware efficient. We observe that the existing reconfigurable interpolation filter architecture is derived using a straight-forward FIR filter design of . Since, the reconfigurable interpolation filter has a different data-flow than the reconfigurable FIR filter, a different design approach need to be considered for interpolation filter. We do not find any such design approach in the literature. The interpolation filter algorithm need to be reformulated taking the data flow of reconfigurable filter into consideration. Here an analysis on interpolation filter computation for different up-sampling factors is designed to identify redundant computations.

The key contribution is:

• Reuse of partial results in reconfigurable interpolation filter.

• A novel block-formulation is presented for efficient realization of reconfigurable interpolation filter.

• Parallel inner-product computations are performed using array-multiplication and addition to facilitate reuse of partial results in an interpolation filter.

• A parallel reconfigurable architecture is presented for area delay and power efficient realizationof interpolation filters.

The reconfigurable architecture is shown in Fig. 1 It has three main units, i) coefficient selection unit (CSU), ii) input-vector generation unit (VGU), and iii) arithmetic-unit. The CSU is comprised of number of :1MUXes or number of ROM LUTs of depth words each, where is the filter length and is the number of interpolation filters of different coefficient vector to be realized in the reconfigurable architecture. To avoid longer critical path delay, MUX-based CSU is used for , otherwise the ROM-based CSU is preferred. The required coefficient-vector of a particular interpolation filter is selected in one cycle from the CSU. The VGU receives one input-block in each cycle and generates input-vectors of size each in parallel, where is the smallest up-sampling factor from a set of different up-sampling factors to be realized by the reconfigurable architecture. Internal structure of the VGU is shown in figure 2. It is comprised of registers. The VGU receives a block of input samples in every cycle and produces 8 data-vectors.

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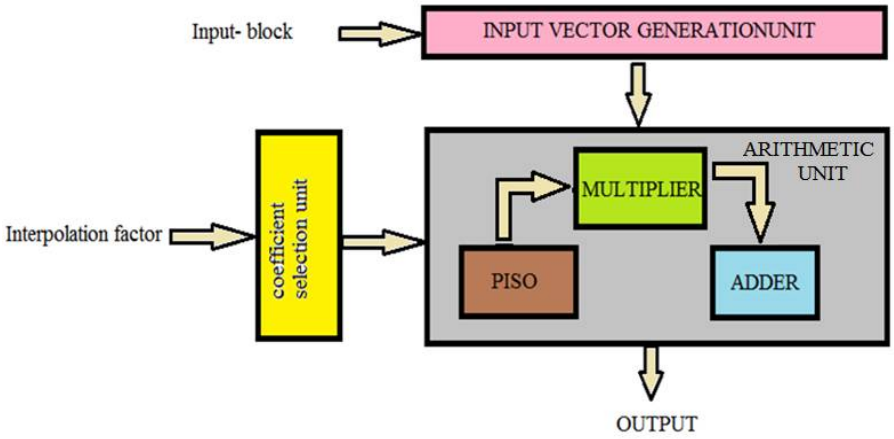


Fig 1: Architecture of an interpolation filter.

The architecture reuse the partial results for parallel computation of filter outputs of different up-sampling factors. It does not require reconfiguration to compute filter outputs of a particular interpolation filter for different up-sampling factors, and configured when there is a need to change the filter specification. In that case, a coefficient-vector of the desired filter is selected from the CSU and fed to the AU to perform the filter computation. The VGU and AU constitute the core of the proposed structure and they do not require any reconfiguration to change the filter computation. Therefore, the proposed architecture offers reconfigurabilty without using any overhead complexity unlike the existing reconfigurable architectures.

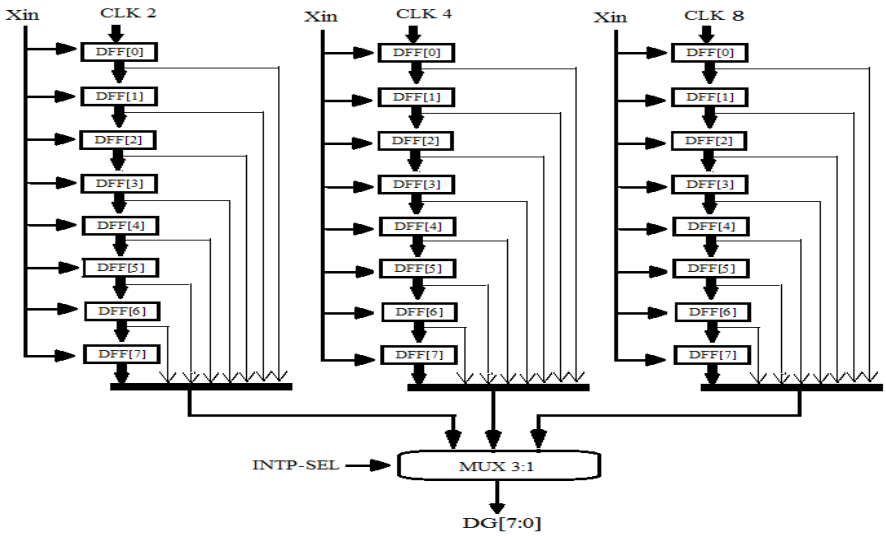


Fig 2 :Internal structure of the vector generation unit (VGU)

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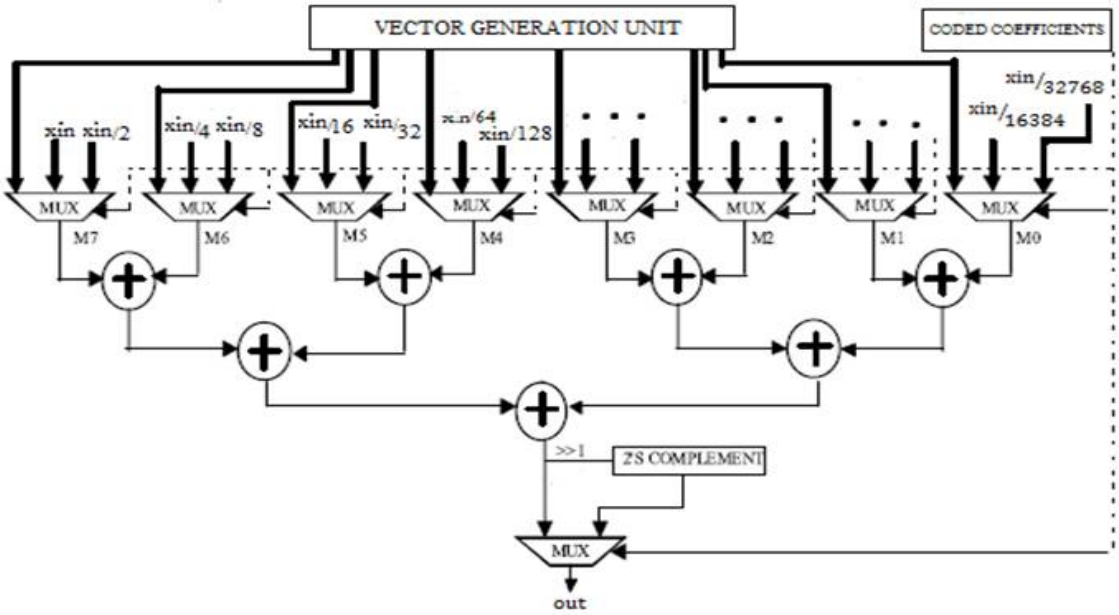


Fig 3 :Internal structure of the arithmetic unit

The filter outputs of (up-sampling factor 8) are added separately to obtain the filter outputs of (up-sampling factor 4). Similarly, the outputs are further added to obtain the filter outputs. Therefore, it is always an advantage to realize the proposed architecture for the lowest upsamplingfactor , and filter outputs of higher up-sampling factors of a given set of up-sampling factors can be obtained in parallel without performing any extra computation. This is an unique feature of the proposed structure which produces filter outputs at multiple sampling frequency of an input sampling frequency. One has to select the filter output of desired sampling rate from the output port. Besides, the complexity of the VGU is independent of input block-size, while the complexity of AU increases proportionately with the block-size. Overall, the complexity of the proposed architecture is independent of up-sampling factor and it does not increase proportionately with the blocks-size. Therefore the area-delay efficiency of the proposed architecture is expected to be better for higher block-sizes.

The interpolation filter is mainly used in those applications where a single reconfigurable filter can replace multiple filters. When a single reconfigurable filter is used it reduces the area and power consumption.the main application of using such type of filters are high frequency applications like the SDR. Interpolation is mainly done to increase the sampling rate at the output of one system so that this can be used as the input of another system working at high frequency. If the sampling rate has to reduced then decimation is done instead of interpolation. Thus the work of both interpolation and decimation has been done.

## III. SIMULATION RESULTS

The interpolation filter architecture consist of three main blocks which include the vector generation unit (VGU),the coefficient selection unit (CSU) and the arithmetic unit(AU).The VGU has been designed and simulated and the result has been obtained. The vector generation unit consist of a series of registers. These registers are designed as D-flipflop. The single module of D-flipflop has been designed and simulated. The coefficient unit is used for the storage of coefficients. Basically CSU is a memory unit. It can be either a mux or a ROM. To avoid critical path delay , mux is avoided. The filter coefficients are taken from the MATLAB. The arithmetic unit consist of a series of multipliers and adders. This is mainly designed to introduce a block formulation so that partial results can be reused to get rid of the redundant terms. Both the process of interpolation and decimation has been done to facilitate the upsampling and down sampling. The difference between upsampling and downsampling is that the process of

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downsampling is that decimation take a longertime to produce the otput since it has longer sample period.the difference between interpolation and decimation is visible in the subfilter section of VGU unit. The results obtained are as follows.

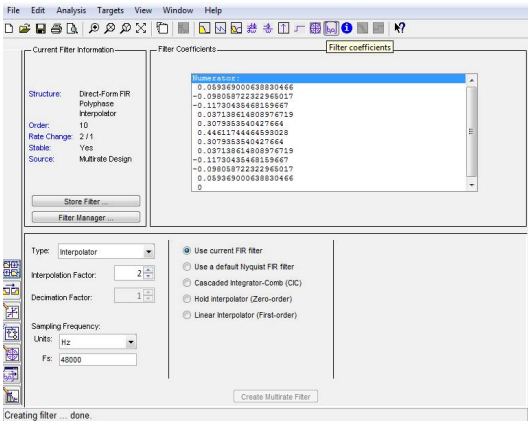


Fig 4 : Co-efficients from MATLAB

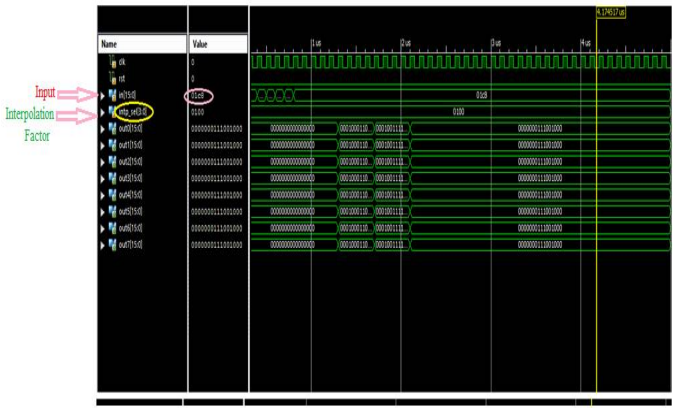


Fig 5 : Waveform of VGU

Fig 4 shows how the coefficients are taken from the MATLAB.there are sixteen 16-bit coefficients. the coefficients are obtained using the fda tool. Fig 5 shows the output waveform of the VGU unit. The input to VGU are hexadecimal values of an audio signal.the output are data vectors and are obtained according to the interpolation factor given.

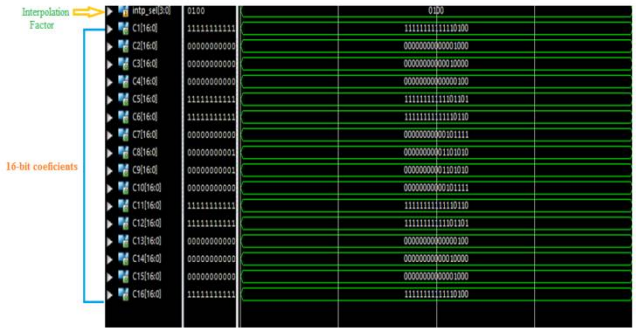


Fig 6 :Waveform of CSU

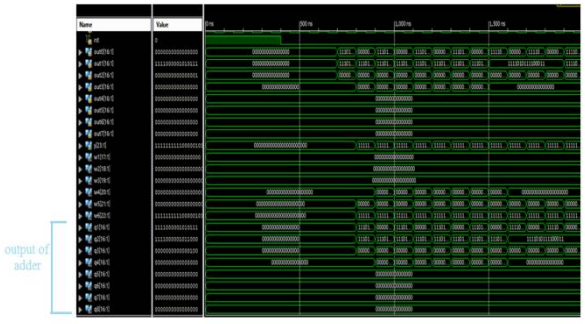


Fig 7 : Waveform of Arithmetic unit

Fig 6 shows the output waveform of the CSU unit. The coefficients are stored in the memory. The coefficients are obtained according to the interpolation factor given. Fig 7 shows the output waveform of the arithmetic unit. The arithmetic unit receives input from the VGU and CSU and the arithmetic operations are done and the output is obtained.

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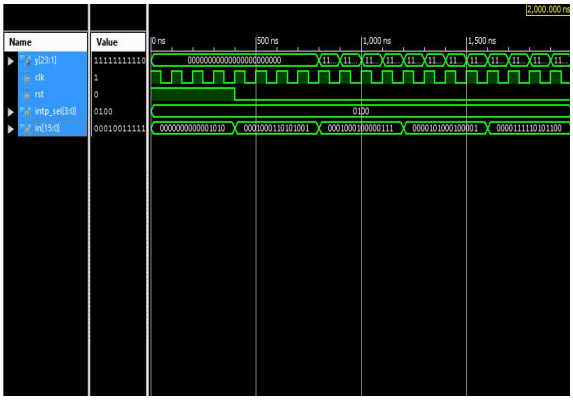

Fig 8 : Waveform of Interpolation Filter

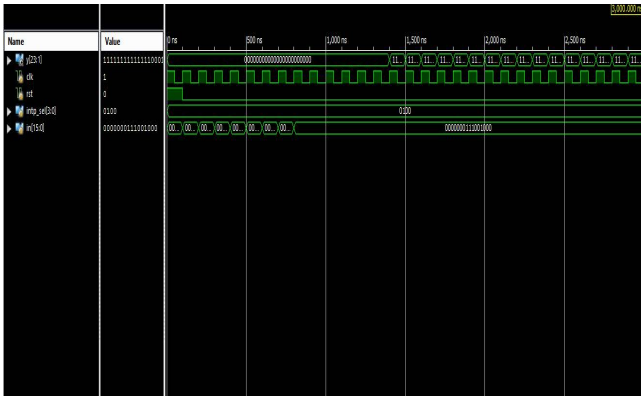

Fig 9 : Waveform of Decimation Filter

Fig 8 shows the final output waveform of the interpolation filter. y is obtained as the output when the audio signal is given as the input along with the coefficients and interpolation factor. Similarly fig 9 shows the final output waveform of the decimation filter where y is obtained as the output.

## V. CONCLUSION AND FUTURE WORK

The most efficient way to design a variable digital filter is interpolation.Interpolation is upsampling followed by filtering.Interpolator is used in digital signal processing (DSP) systems to increase the sampling rate digitally. It comprises an up-sampler and an anti-imaging (interpolation) filter. The up-sampler change the sampling rate of base-band signal, while the interpolation filter suppresses the undesired interference effect resulted due to up-sampling the base-band signal. The interpolation filter architecture mainly consist of three blocks which include vector generation unit (VGU), coefficient selection unit (CSU) and the arithmetic unit (AU). Interpolation filters are mainly used in SDR and other such applications where the hardware is complex .The complexity of the hardware can be reduced and the system works efficiently by the use of interpolation filter. Communication system with different units working with different frequencies can be designed efficiently by the use of interpolation and decimation filters.

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