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Optimal Design and Analysis of 12T MTCMOS and MCAM Using VLSI

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ABSTRACT: Memories are an integral part of most of the digital devices and hence reducing power consumption of memories as well as area reduction is very important as of today to improve system performance, efficiency and reliability. A transistorized SRAM cell is conventionally used as the memory cell. The memristor behaves as a switch, much like a transistor. However, unlike the transistor, it is a two-terminal rather than a three-terminal device and does not require power to retain either of its two states. Note that a memristor change its resistance between two values and this is achieved via the movement of mobile ionic charge within an oxide layer, furthermore, these resistive states are non-volatile. This project focuses on new approach towards the design and modeling of memristor based CAM (MCAM) using a combination of MOS devices to form a core of a memory or logic cell that forms the building block of the CAM architecture and 6T SRAM and 12T MTCMOS SRAM cell. Our proposed work will be, new memory model have been determined and compared with existing models and proposed cell design dissipates less power at different temperatures than existing models. Simulation did on the basis of Microwind 3.1 Back End CMOS Technology to reduce power consumption and enhance data stability.

KEYWORDS: Energy efficient algorithm; Manets; total transmission energy; maximum number of hops; network lifetime

I. INTRODUCTION

In today's day to day life, there is need of storing devices, where these devices require memory to store the data. This term memory is concept of the actual chips capable of holding data. DRAM, SRAM, PROM, MCAM, FLASH etc. are types of memory having various properties shown in the fig.1.1. Out of which, we explore concept, design and modeling of memory cell as a part of Memristor based Content Addressable Memory architecture using a combination of switch having some fixed resistance value as memristor and n-type MOS devices. It is that new circuit elements defined by the single valued relationship dø=Mdq must exist; whereby current moving through memristor is proportional to the flux of magnetic field that flows through the material and static random access memory the term refers to read and write memory. It is volatile, which means that it requires a steady flow of electricity to maintain its contents. Both memories are based on fundamental concept of nMOS logic provide a strong basis both for the conceptual understanding and development of CMOS design.

VLSI technology is used in both analog system as well as digital integrated system has various advantages such as it has small size of chip, low power consumption, high performance speed, large storage capacity etc. However, such technology needs a complex method to implement on hardware as this technology uses very small size of chips ranging from micro to nanometer of size. It is required to use simulation based circuit design. In addition to transistor-level circuit design issues, the accurate prediction and reduction of interconnect parasitic has become a very important while desighning high-performance digital integrated circuits.

To aware customers to choose the best storing device in between different SRAM and MCAM cell with consideration of all parameters? Hence this reason motivated me to select this project. The main objective of this work deals with the design and analysis of high speed performance addressable memory for future search engines to develop low power consumption and no loss of store data in a cell even if the power supply is turn OFF.

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II. RELATED WORK

In [1] Leon Chua more recently argued that the definition should be generalized to cover all 2-terminal non-volatile memory devices based resistance switching effects. In this paper they explore concept, design, and modeling of the memory cell as part of a memristor-based content addressable memory (MCAM) architecture using a combination of memristor and n-type MOS devices. In [2] authors reviewed CAM-design techniques at the circuit level and at the architectural level. The main CAM was designed to reduce power consumption associated with the large amount of parallel active circuitry, without sacrificing speed or memory density. In [3] authors present paper on CMOS 6-transistor SRAM cell for different purposes including low power embedded and stand-alone SRAM applications. The data is retained by the cell with the help of leakage current and positive feedback Also, the proposed cells uses a single bit-line for both read and write purposes.Switching operational voltage of the bit-line lies between 0.25 to 0.5VDD to decrease power consumption. All simulations are done using0.18um Technology. In [4] authors proposed new low-power SRAM using bit-line Charge Recycling (CR-SRAM) for the write operation, differential voltage swing of a bit-line is obtained by recycled charge from its adjacent bit-line capacitance, instead of the power line Applying such a charge recycling technique to the bit-line significantly reduces write power. In [5] authors developed their compact models for current-controlled and voltage-controlled memristors. These models were developed based on the fundamental relationships between charge and flux of memristors. In [6] Authors research on application of 45nm VLSI technology to design layout of static RAM memory. In [7] authors has proposed structure of a 12T MTCMOS based SRAM cell is proposed. A charge recycling technique is used to minimize the power consumption during the mode transition and two voltage sources are used at the output nodes to reduce the swing voltages during switching activity.

III. PROPOSED METHODOLOGY

The proposed methodology flow chart is shown in figure 3.1.

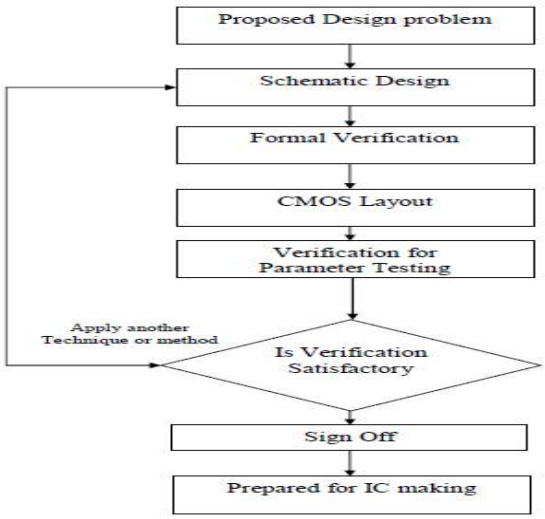

Fig.3.1. Design Flow Chart

To achieve the proposed target following design steps are include in the design and analysis of proposed phase-locked loop.

- Schematic design of proposed SAR logic based ADC using CMOS transistors (BSIM4)
- Performance verification of all the different parameters.

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- CMOS layout designs for the proposed all types of oscillators using VLSI backend.
- Parameter testing verification.
- If the goal is achieved for all proposed parameter including detail verification then only sign off design analysis and it will be ready for IC making.
- If detail verification of parameters would not complete then again follow the first step with different methodology or technique.

Oscillator is key circuit use in modern communication, processors and in many systems. These oscillators are use is to create a periodic logic or analog signal with a stable and predictable frequency. Here we are going to design the oscillator that solves the problem of power consumption, area consumption and generate the desired frequency band. While dealing with physical design implementation, we need to follow various CMOS design rules. Here in this project, we are following the Lambda based design rules.

CMOS layout design rules are given below;

1. Minimum width: The purposes of the design rules are to guarantee the precise layout according to the rules defined by the specific process. Minimum width: In order to prevent the line layer from notching or necking, the minimum width for each specific layer is defined; such as minimum width for active, polyl, poly2, or metal layers.
2. Minimum spacing: The line to line spacing is defined to avoid line shorts or bridging for polyl, poly2 and metal layers.
3. Overlap: This check is for two overlapped layers. Normally it is needed to check metal contact, poly contact or active contacts. For different voltages, different overlap rules are required.
4. Misalignment: In this process, n-well is a major flat layer, active and p-field to n-well are direct alignments, active to p-field is an indirect alignment, polyl, poly2, **N+** implant and **P+** implant to active are direct alignments. They are in indirect alignments with each other. Contact to poly2, metal to contact and pad to metal are direct alignments.
5. CMOS color map and technology files: In general, color map and technology files are needed only for layout drawing. To create a layout drawing, we need to specify all the layers. "A technology file defines various masks and symbolic layers in a cell. This file also defines the color, fill pattern, and outline pattern used to display each layer, and references a color map file that sets each layer's color^^, (Valid layout EDITOR REFERENCE MANUAL of Microwind).

IV. SOFTWARE USED

EDA TOOL-MICROWIND:

Integrated circuit is used to simulate and design using MICROWIND software at physical description level. This package contains a library common logic and analog ICs to view and simulate the various designs to obtain different parameters. We can achieve access to circuit simulation by pressing single key. The electric extraction of circuit is automatically performed and the analog simulator produces voltage and current curves immediately. Also we are using 32 nm technology, the high K dialectic is used. It enables the thinner equivalent oxide thickness while keeping the leakage current lowThe main screen of Microwind is illustrated in this screen given below. It is also possible to cut, past, duplicate, generate matrix of layout, use the layout editor to insert contacts, MOS devices, pads, complex contacts and path in one single click. . Pa1ette Editor Display given in microwind will provided you different interconnects with

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different colours as; p active layer would be in yellow on a colour graphics terminal1,n active layer is in green, polysilicon layer (poly2) is in red, metal layer is in blue, contact cut is cross, n-well layer is dashed line.

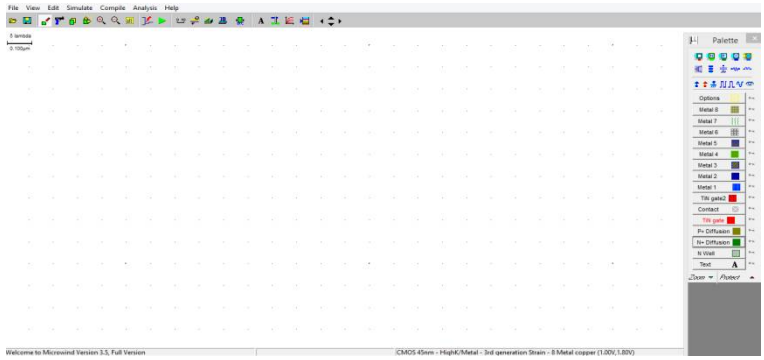

Fig. 3.2: GUI of Microwind tool

V. SIMULATION RESULTS

The simulation studies involves finding out the frequency v/s power output calculations, we need to modify the input in various values. By changing the values of the input, the proposed cell is varied with various frequencies and will gives rise to the power dissipation at the particular frequency. The test cases are given as below;

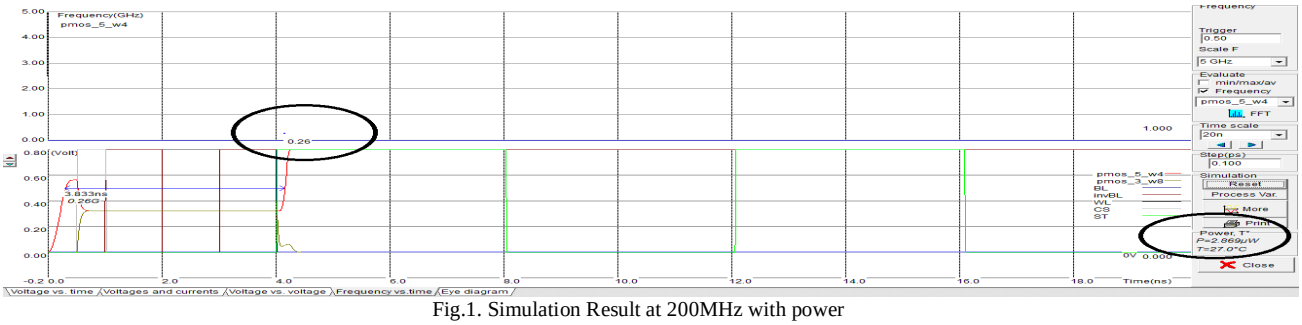

Fig.1. Simulation Result at 200MHz with power

Above fig. shows first case of simulation result of frequency v/s power dissipation. Upper encircle point shows frequency and lower encircle point shows power dissipation. First reading from table 1.5 shows 2.869 µw power dissipate at 200 MHZ frequency by using 32nm technology, which is compared with existing 12T MTCMOS cell using 45 nm technology i.e 4.827 µw at 200 MHZ. It concludes that our memory cell design is better than previous one.

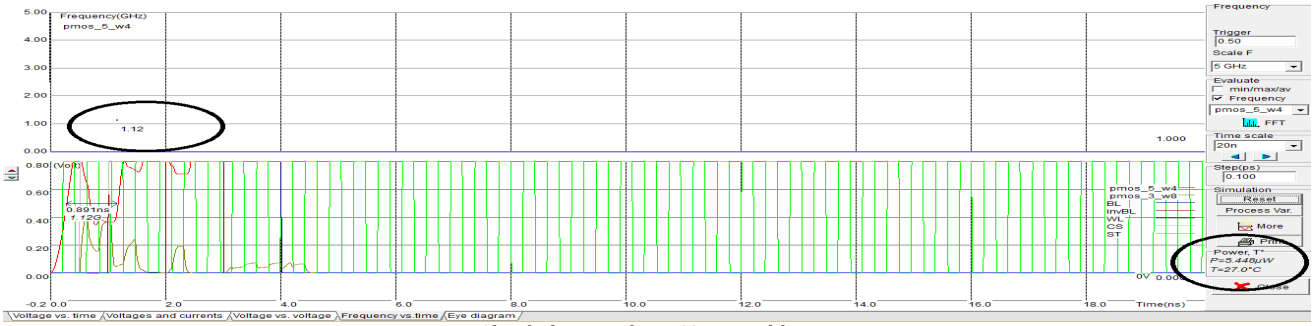

Fig.2. **Simulation Result at 500MHz with power**

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Above fig. shows second case of simulation result of frequency v/s power dissipation. Upper encircle point shows frequency and lower encircle point shows power dissipation. Next reading from table 1.5 shows 2.996 µw power dissipate at 500 MHZ frequency by using 32nm technology, which is compared with already design 12T MTCMOS cell using 45 nm technology i.e 5.192 µw at 500 MHZ. It concludes that our memory cell design is better than previous one. For higher frequency our proposed cell consumes less power.

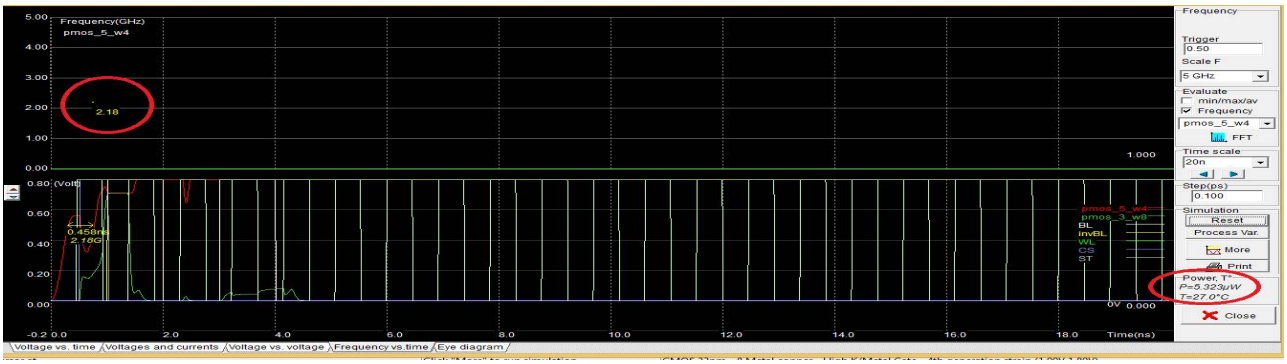

Fig.3.Simulation Result at 2 GHz with power

Above fig. shows third case of simulation result of frequency v/s power dissipation. Upper encircle point shows frequency and lower encircle point shows power dissipation. Next reading from table 1.5 shows 5.323 µw power dissipate at 2 GHZ frequency by using 32nm technology, which is compared with existing 12T MTCMOS cell using 45 nm technology i.e 6.673 µw at 2 GHZ. It concludes that for higher frequency our proposed cell consumes less power.

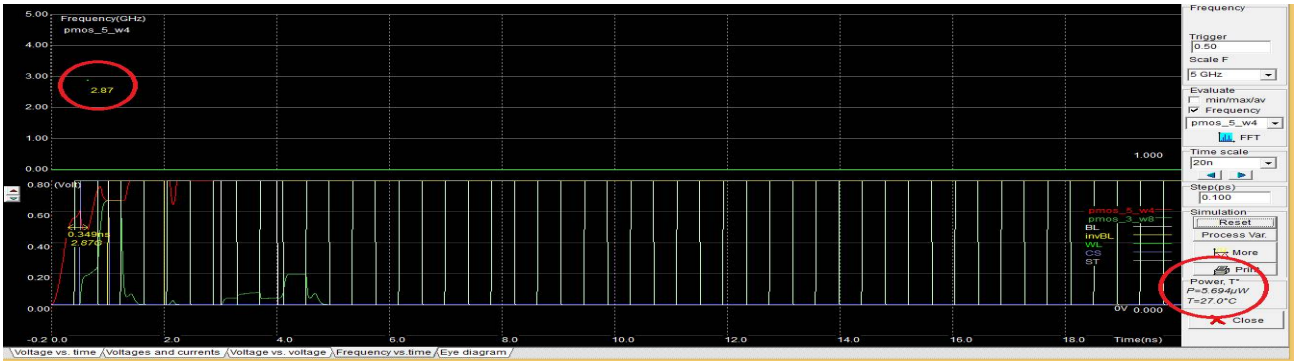

Fig 4. **Simulation Result at 3 GHz with power**

Above fig. shows fourth case of simulation result of frequency v/s power dissipation. Upper encircle point shows frequency and lower encircle point shows power dissipation. Next reading from table 1.5 shows 5.694 µw power dissipate at 3 GHZ frequency by using 32nm technology, which is compared with existing 12T MTCMOS cell using 45 nm technology i.e 7.013 µw at 3 GHZ. It concludes that for higher frequency our proposed cell consumes less power.

Table 5.1 Dynamic Power Dissipation at Different Frequencies

Frequency	12T MTCMOS(µw)	Proposed 12T MTCMOS(µw)
200MHZ	4.827	2.869
500MHZ	5.192	2.996
2GHZ	6.673	5.323
3GHZ	7.013	5.694

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Table 5.2: Comparision of Various Parameters of Different Memory Cell using 32nm CMOS Technology

Parameters	6T SRAM Cell	7T NOR MCAM Cell	12T MTCMOS Cell
No. of NMOS transistor used	4/2000	7/2000	10/2000
No. of PMOS transistor used	2/2000	0/2000	6/2000
No. of electrical nodes used	10/3000	13/3000	27/3000
Width of layout size (µm)	2.5µm (121 lambda)	1.8µm (98 lambda)	11.9µm (594 lamda)
Height of layout size (µm)	0.8µm (42 lambda)	1.9µm (105 lambda)	7.0µm (351 lamda)
Chip Area (μm^2)	2.0 μm^2	3.3 μm^2	83.4 μm^2
No. of transistors used	6	7	12
Write op. voltage (V)	0.35 V	0.35 V	0.35V
Read op. voltage (V)	0.35 V	0.35 V	0.35 V
Type of Memory	Volatile	Non-Volatile	Volatile
Power consumption	3.314µW	50.006 µW	1.407µW
No. of NMOS transistor used	4/2000	7/2000	10/2000
No. of PMOS transistor used	2/2000	0/2000	6/2000

Table 5.2 shows comparison of different memory cell on the basis of different parameters such as No of Pmos and Nmos transistors, No. of electrical nodes, write and read output voltage, height and width of layout, power consumption, type of memory. Below table provided the simulation result in the tabular form. It shows the complete design parameters.

VI. CONCLUSION AND FUTURE WORK

The proposed Memory models are designed and simulate using 32nm CMOS/VLSI technology with Microwind 3.5 EDA tool. This Software used in a program allows us to design and simulate an integrated circuit at physical description level Here we estimated and presented simulation results by implementing the circuit layouts in32 nm technology. The simulation results pointed out that structures designed and simulated almost eliminate leakage and reduction in leakage between 45%- 70% depending on the control voltage used. We also simulate the parametric analysis on the design in order to get the cell stability by varying the cell input frequency with respect to the change in power. The cells are very stable and yield the stable power with respect to the change in AC analysis. From the analysis of various parameters of various SRAM and MCAM CELL shown in fig. 5.2; it is observed that the power consumption parameter of 12T MTCMOS Cell is very low. Hence, 12T MTCMOS TYPE SRAM CELL having low power consumption is of 1.407µW is more preferable as compare to other memory models. The same layout design of

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32nm technology can be used in increasing technology such as 22nm, 11nm and so on. Memristor based Content Addressable Memory is used for high performance future search engines

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BIOGRAPHY

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