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Review on Different Embedded Platform Based LP Localization Methods

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ABSTRACT: This paper compares the DSP embedded platform with FPGA, for license plate localization on the basis of detection rate, time and image size. Number plate localization is a very important stage in an Automatic Number Plate Recognition (ANPR) system and it is comparatively intensive task. The algorithm for plate localization is targeted to be of low complexity and high detection rate. The FPGA based system can be implemented and tested using a Mentor Graphics RC240 Field Programmable Gate Arrays development board that is equipped with a 4M-gate Xilinx Virtex-4 LX40. The proposed system can achieve 98.4% of detection rate within 2.7ms at cost of only 2% of the available area in the FPGA. Whereas the system implemented on an embedded DSP platform consists of detection and a character recognition module. The detection is based on the AdaBoost approach that is given by Viola and Jones detector. By using region-based method, the detected license plate can be segmented into individual characters. Character classification can be performed with support vector classification. DSP based embedded platform can achieve 96% detection rate within 140 ms.

KEYWORDS: Automatic Number Plate Recognition (ANPR)**,** Number Plate Localization

I. INTRODUCTION

Today there is a need for intelligent traffic management systems to deal with the continuously increasing traffic on the roads. Information about current situations can be automatically extracted by image processing algorithms. Along with vehicle detection and tracking, the identification through license plate recognition is important for a variety of applications. These applications are automatic congestion charge systems, access control, tracing of stolen cars, or identification of dangerous drivers [20]. An automatic number plate recognition (ANPR) system is being applied for such type of applications. The embedded systems are cheaper than general purpose computers and suitable for deployment in tough environments due to their physical robustness. An automatic number plate recognition (ANPR) system is used for tracking, identifying and monitoring moving vehicles. [16]. An ANPR system involves various steps that are image capturing, image processing and plate recognition. In the image processing phase, two tasks are included, i.e. Plate localization and character recognition .Plate localization normally requires two major tasks. The first one is to separate number plate area from non-number plate area and the second one is plate adjustment [3]. The plate recognition stage requires a pre-processing step which is plate segmentation. In plate segmentation the symbols or characters will be separated from the NP so that only useful information is obtained for recognition where the image format will be converted into symbols or characters [2]. The detection stage of the license plate is the most critical step in an automatic vehicle identification system. [17] Much research has been carried out to overcome many of the problems faced in this area, but there is no such method used for detecting license plates in different places or countries, because of the difference in plate style or design [4].

II. RELATED WORK

Current LP methods can mainly be classified into colour-based systems has been built to detect specific plates having fixed colours [4]–[5]. External-shape based techniques were developed to detect the plate based on its rectangular shape [6]–[7]. Edge-based techniques were also implemented to detect the plate based on the high density of vertical edges inside it [8]–[9]. Research in [10] and [11] was based on the intensity distribution in the plate’s area with respect to its neighbourhood where the plate is considered maximally stable external region. The image processing algorithms requires strong computing power, so it is required to choose high performance workstations and expensive

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supercomputers. The cost, compactness and power issues are the factors that motivate the search for other platforms. Recently the improvements in computing power of programmable gate arrays (FPGAs) and digital signal processors (DSPs) have motivated researchers to consider them as low cost solution for such computationally intensive task [21]-[2]. Therefore, high performance computer workstations are necessary. An alternative solution for this problem is to choose FPGAs and DSPs [21]. These devices can be used as low cost on chip solution that allows the processing FPGA or DSP-based unit to be placed within an ANPR cameras housing to create intelligent cameras namely cameras that record and process images for sending back to a server. This paper presents a speed and area-efficient architecture based on a low complexity LP localization method that is suitable for FPGA implementation. This method uses open and close morphological operations [2].A comparison of different LP localization and recognition systems is difficult because each system is subjected to different prerequisites. Further, the lack of a common evaluation database makes evaluations and comparisons unfair. The focus is on the architecture and implementation of a complete LPR system based on embedded platform.

III. NUMBER PLATE LOCALIZATION BASED ON MORPHOLOGICAL OPERATION

3.1 Number Plate Localization Algorithm

The proposed algorithm is mainly based on two morphological operations, the first open morphological operation extracts the features of the NP, the second open operation removes noise, and the close operation is then used to fuse the pixels in the NP region together.

The proposed algorithm has two major stages:

1. Morphological operations for extracting plate features;
2. Selection of candidates region [18].

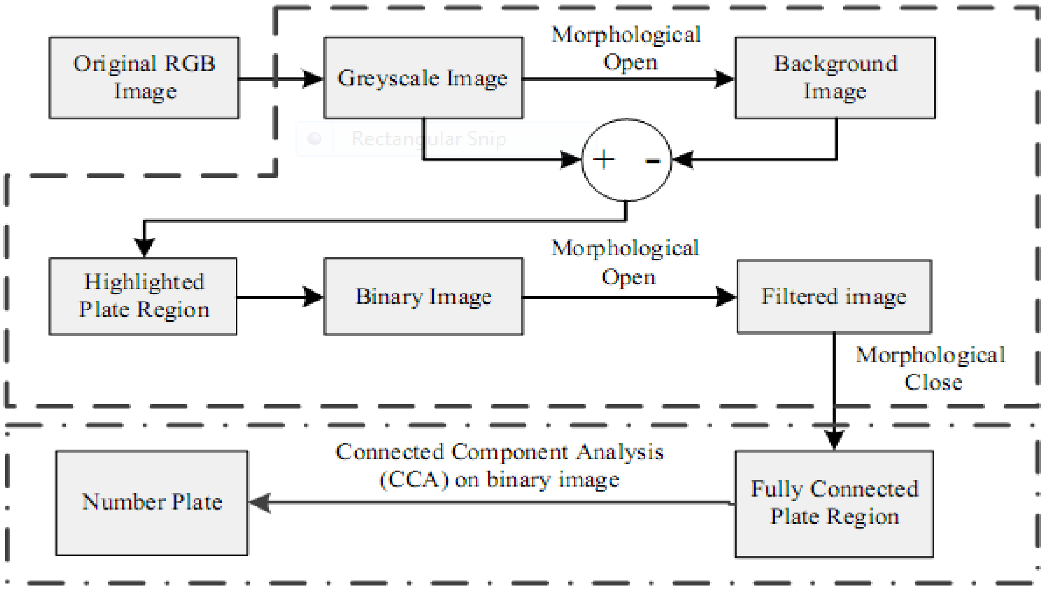

Fig. 1 shows a block diagram of the proposed NPL system [18].

1. Plate Feature Extraction

The proposed algorithm mainly uses three morphological operations to minimise the pixels of the non-plate region and to enhance pixels of the plate region. The original RGB image is first converted into a greyscale image, which will be used as an input to the following block where the first morphological open operation will be used. The morphological open operation is erosion followed by dilation and the opposite operation (i.e. close operation) is a

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dilation followed by erosion. The shape of the morphological operation depends on a suitable structuring shape employed as a probe called the Structuring Element (SE) [19]. Open and close operations can be performed as shown in (1) and (2) respectively.

Io= (I ʘ SE) Θ SE ……………………………… (Eqn1)

Ic= (I Θ SE) ʘ SE ……………………………… (Eqn2)

Where I denote a greyscale input image, Θ denotes a dilation operation and ʘ denotes an erosion operation:

2. Selection of Candidates Plate Region

The output image from the previous stage consists of a set of groups of connected pixels. A labelling algorithm CCA is used to mark these pixels. In the proposed work, the CCA uses a '4-connectivity' method, and labels them using different numbers. Once all the groups of pixels have been determined, each pixel is labelled based on the group it belongs to. Therefore, a set of potential candidates can be selected from the image using known geometrical conditions, which mainly consist of the width, height and ratio of the plate region [18].

3.2 Proposed Number Plate Localization Architecture

Morphological operations based architecture consists mainly of an image reader, three morphological operations and CCA.

Therefore, this architecture can be designed using the following modules:

- Memory Reader Module;
- Converter Module;
- Morphological Operations Module; and
- CCA Module. [18]

The structure of the proposed architecture is shown in Fig. 2

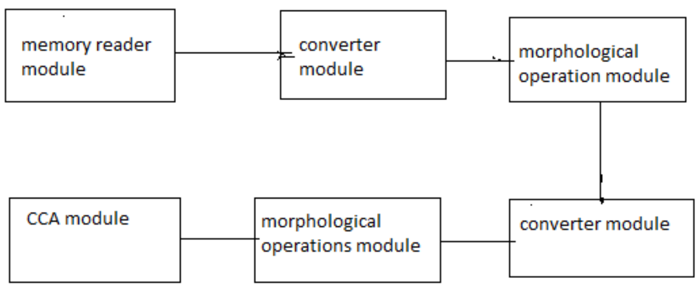

Fig.2. shows Proposed Number Plate Localization Architecture [2]

Memory Reader and Converter Module:-

The first module in the proposed architecture is the memory reader and converter. The memory reader part of the module is used to read the RGB values for each pixel from the original RGB image which has a size of 640*480 and to assign a position coordinate [18].

Morphological Operations Module:-

The morphological operations module consists of the morphological open and the morphological close sub-modules. According to the equation (3) and (4), the morphological open operation and the morphological close operation can be divided into two sub-filters respectively, i.e. the morphological dilation and the morphological erosion sub-filters, where the order in each case decides whether the morphological operation is open or close. The grayscale dilation

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calculates the maximum pixel value in a specific SE. On the contrary, the grayscale erosion calculates the minimum value in a specific SE [18].

CCA Module:-

The CCA module is used to mark and select a candidate plate region from the entire binary image. Generally, the pixels of the input pixel stream are divided into several groups or blobs by the CCA module. The grouping is based on the pixels' connectivity [18].

IV. LICENSE PLATE DETECTION AND RECOGNITION USING DSP EMBEDDED PLATFORM

4.1 License Plate Detection

The detection module consists of three parts: the detecting, the tracking and the post-processing step. All parts and their interaction are described in the figure 3.

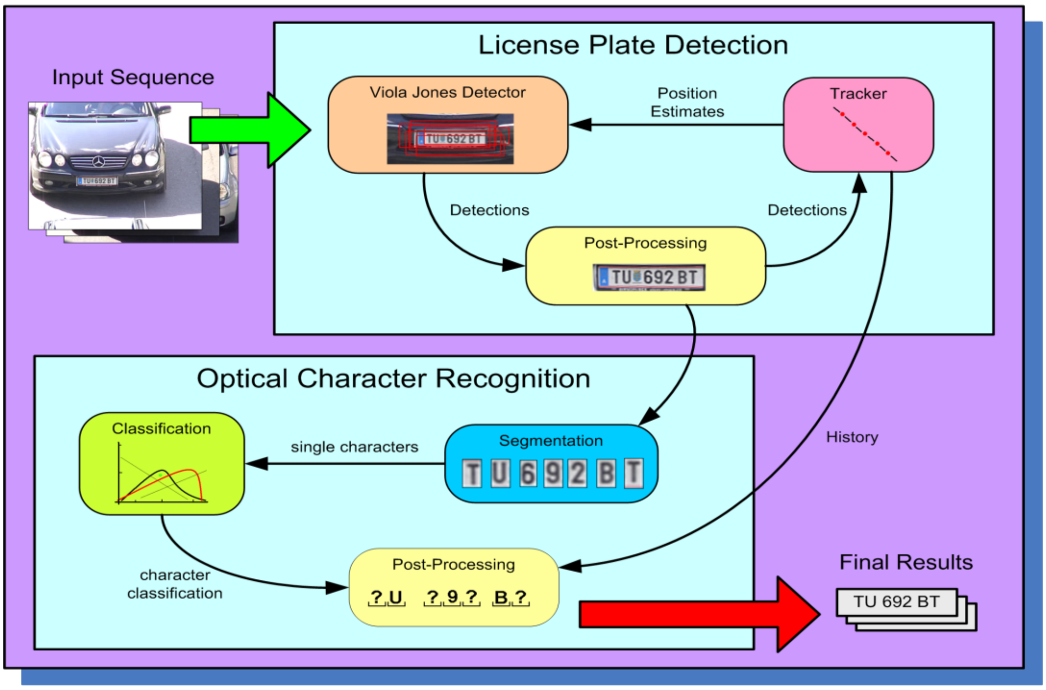

Fig.3. shows .the system contains two main modules. Given an image sequence as input, the first module, the detection module, applies algorithms for detecting and tracking of license plates. In the second module, segmentation and, subsequently, character recognition is performed to generate the final result [20].

*Detector***:**

The license plate detector depends upon the framework proposed by Viola and Jones [15]. Viola and Jones detector introduce a fast object detection system that is obtained by combining the AdaBoost-algorithm [13] with Haar-like features, a classifier cascade and the integral image for fast feature computation.

Post-processing:

The exhaustive search technique of the Viola and Jones detector results into multiple detections for a single license plate. Thus, post-processing methods can be applied in order to merge those detections. For this purpose the

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simple non-maximum suppression is used. The non-maximum suppression merges the multiple detections, considering the confidence value of each detection. But the final detection does not only contain the license plate but parts of the surroundings also [20].

*Tracker***:**

A Kalman tracker[14] is integrated into the system that is used to limit the search of the detector to certain areas of the input image. This requires a rough calibration of the scene. For each new detection a Kalman tracker is initialized, which predicts the new object's position on the next frame. This allows for scanning only within a small area around the estimated position [20].

4.2 License Plate Character Recognition

License plate character recognition consists of three separate parts as shown in Figure 3: First, characters are isolated with a region-based approach, secondly character classification is done using a support vector machine (SVM) and finally, during post-processing a prior knowledge about the expected license plates and information provided by the tracker is used to improve the classification result [20].

Segmentation

A region-based approach is used for character segmentation. Due to dark characters on white background, region-growing seeded with lowest intensity values is applied. A region descriptor consisting of compactness, entropy of the greyscale histogram, and central invariant statistical moments. The descriptors are classified using support vector classification[20].

*Classification***:**

Character classification can be done using support vector classification. Segmented regions are scaled to a common patch size. The feature vector comprises of direct pixel values. Since character recognition is a multi-class problem so the combination of binary classifiers is required [20].

Post-Processing

In this step previous knowledge about the structure of license plates is used i.e. spacing between subsequent characters and furthermore the syntax of the final character string. Not necessary to mention that this applies only in cases where the nationality of the license plate is known in advance or can be derived before. Additionally, classification results of subsequent frames are combined using the history provided by the tracking module. A simple majority voting individually for each position within the character string is applied. The character achieving the highest count is selected [20].

V. SUMMARY:

5.1 FPGA Implementation

The proposed architecture for NPL can be simulated in PAL Virtual Platform (PALSim) [16]. After simulation, the architecture can be implemented and verified using the Mentor Graphics RC240 FPGA development board equipped with a 4M-gate Xilinx Virtex-4 LX40 [17]. Handel-C and Pixel Streams, which is a library that can be used for rapid development of video image streaming applications, can be used for the hardware description of the proposed architecture [18]. The original RGB image is stored in an external memory on the RC240 board. The external memory data width is 32 bits, which means every pixel value can be saved on a single memory location. Every clock cycle one data pixel is passed from one block to the next. The results show a similar performance compared to the software implementation in terms of NPL rate where the entire overall rate is 97.8%.

5.2 DSP Embedded Platform Implementation

The Viola-Jones detector is very popularly used for License Plate Detection. To detect a sub region of an object in motion, the simple motion detection algorithm is not sufficient to accomplish this task. Therefore the usage of the Viola-Jones detector is justified. Its application can be seen in searching license plates on cars in a urban traffic surveillance video. Further OCR (Optical Character Recognition) can be performed on the license plates detected, thus

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there are some minimum requirements for the size of the detections. The detection algorithm was applied to a full 352x288 frame using a classifier. Due to the detector with high accuracy, a simple non-maximum suppression algorithm served sufficiently for post-processing [20]. Referring to the table1, the average time for processing a single frame is about 140ms.

Processor	**DSP C6414 and FPGA**	**FPGA Virtex-4**
Clock speed (MHz)	**600**	**149.120**
Image size (pixels)	**352*288**	**640*480**
LP location time (ms)	**140**	**2.7**
Success rate of LP location (%)	**96**	**98.4**

Table 1.shows the comparison between the processor used for LP localization [3].

VI. CONCLUSION

An embedded platform is capable of performing high-level computer vision tasks such as vehicle and license plate detection in real-time. It is seen that it is possible to build a flexible and robust embedded vision system that can be applied for wide area of applications by using a modular and flexible software design for embedded device. But to get additional gain performance and accuracy concentration on further algorithm for quality improvement and a better mapping to the underlying DSP architecture is required. Referring to the table1 it can be said that detection algorithm can be applied to a full 352x288 frame using a classifier and the average time for processing a single frame is about 140ms with success rate of LP localization is 96%.Whereas Mentor Graphics RC240 Field Programmable Gate Arrays (FPGA) development board that is equipped with a 4M-gate Xilinx Virtex-4 LX40 can achieve 98.4% detection rate within 2.7ms at the expense of only 2% of the available area in the FPGA.

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