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InAlAs/InGaAs Insulated Gate with Different Gate Dielectrics for Improved DC and RF Performances

N.Anbuselvan [1], K.Prabhakaran[2], R.Kalaiyarasi[3]

Associate Professor, Department of Electronics and Communicaton Engineering, SKP Engineering College Tiruvannamalai, Tamilnadu, India[1]

Assistant Professor, Department of Electronics and Communicaton Engineering, SKP Engineering College Tiruvannamalai, Tamilnadu, India [2, 3]

ABSTRACT: Compared with the conventional pseudomorphic High Electron Mobility Transistor (pHEMT), the metal – oxide – semiconductor (MOS) pHEMT or IG pHEMT has several advantages such as lower gate leakage current, higher drain current and the better restrain of current collapse, numerous times higher breakdown voltage and channel current. In this paper the performance of InAlAs/InGaAs IG-pHEMT for DC and RF characterization can be improved by reducing the gate length to deep sub-micrometer. By optimizing the gate devise to the improvement in RF performance. The effects of the thickness of gate dielectric on the characteristics of Si_3N_4 IG pHEMT are also deliberate. The thicker dielectric can decrease the gate leakage current. Nevertheless it cannot provide larger g_m because the permittivity of Si_3N_4 is not elevated, Several promising alternatives of gate dielectrics (Al_2O_3,ZrO_2,HfO_2) are presented in this paper.

KEYWORDS: Gate leakage, insulated gate, PHEMT, InAlAs/InGaAs, Si_3N_4.

I.INTRODUCTION

The HEMT stands for High Electron Mobility Transistor, and is also called heterostructure FET (HFET) or modulation-doped FET (MODFET). The basic structure of a HEMT is shown in Figure 1, which is having similarity with MOSFET due to its gate, source, drain and substrate terminals.

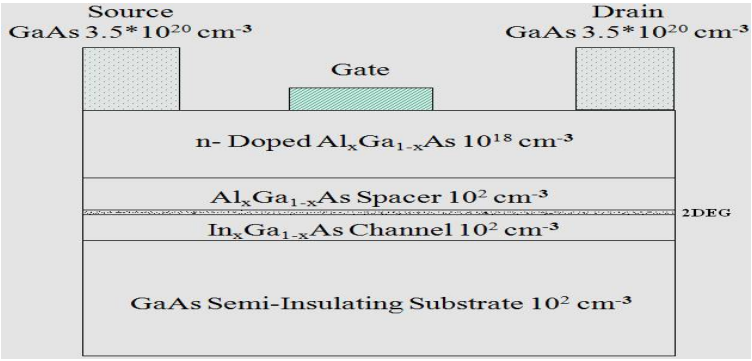

Fig.1. Basic Structure of HEMT

In the above conventional pHEMT, it has a Schottky gate (SG) structure which tends to cause the following problems high DC leakage currents, low breakdown voltage, poor RF power all of which are due to the low and unstable barrier height at the Schottky interface as well as to forward conduction inherent in the Schottky gate[1],[2]. To solve these problems, use of an insulated gate (IG) structure is a shows potential approach. However, understanding of a good IG structure on III–V compound semiconductors has been known to be complicated due to strong Fermi level pinning which takes place at the insulator-III–V compound semiconductor interface due to high-density interface states [3], [4].

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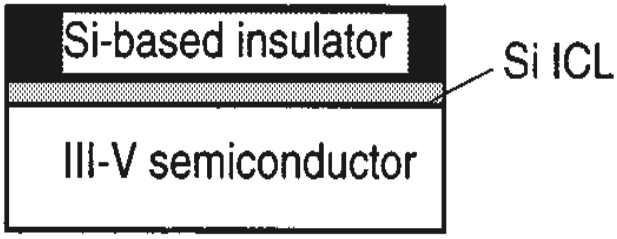

Fig. 2. A basic insulator-III–V semiconductor structure utilizing Si ICL.

Compared to a conventional pHEMT of similar design, the IG pHEMT exhibits the several orders of magnitude lower gate leakage and several times higher breakdown voltage and channel current. In addition, it will improved the device characteristics performance, as compared with the conventional (pHEMT).On the other hand, insertion of the Si ICL dramatically improved the DC performance, showing excellent gate control and complete channel pinch-off [5]. The maximum drain currents became 4 times larger than those of the IG-PHEMT without Si ICL. A maximum transconductance was achieved at V_G=0 V. This is 20 times larger than the IG-PHEMT without Si ICL. All these improvements are due to the removal of the Fermi level pinning.

A).DIFFERENT DIELECTRICS IN InAlAs/InGaAs INSULATED GATE PHEMT

The gate leakage current is an important factor that limits the performance and dependability of conventional pHEMTs. The introduction of a thin insulator layer between the gate metal and the InAlAs barrier layer can increase barrier height and restrain the gate leakage current. An additional advantage of MOS HEMT is that the material used as the gate dielectric can also be used as a surface passivation layer and reduces the current collapse. The dielectric constants and band gap of various gate dielectric materials have been shown in the following Table 1 [12].

Table.1. Dielectric constants and energy gap of some gate dielectric materials

Gate dielectrics	Dielectric constant	E_g(Energy gap)
SiO_2	3.8~3.9	8.0
Si_3N_4	7.0~7.6	5.1
ZrO_2	15~30	7.8
HfO_2	45~150	5.65
Al_2O_3	9~12	8.9
Ta_2O_5	15~25	4.2

The references show that Si_3N_4 has the larger dielectric constant and the superior interface characteristics than SiO_2. Si_3N_4 dielectric has the enhanced passivation effect and the transconductance of Si_3N_4 IG pHEMT can be improved obviously. Otherwise, some high-k dielectrics, such as Al_2O_3 (k~9-12), ZrO_2 (k~15-30) and HfO_2 (k~45-150), are being used as a gate dielectric in order improve transconductance.

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II.DEVICE STRUCTURE AND SIMULATION

The cross-sectional structure of the novel InP-based IG-PHEMT is shown in Fig.3.

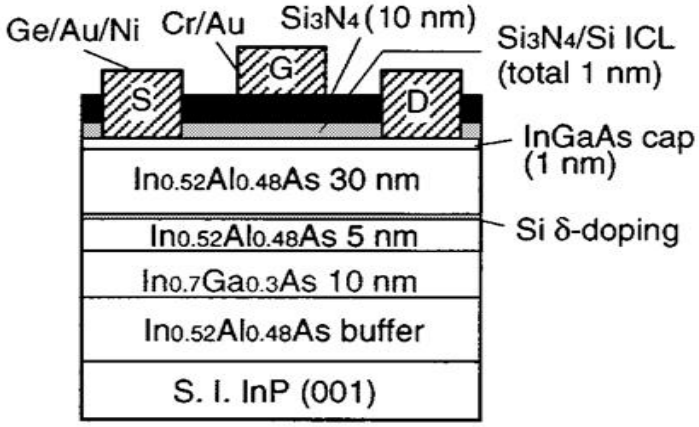

Fig.3.Cross-sectional structures of an InAlAs/InGaAs insulated gate (IG)-PHEMT.

The energy band diagram of two dissimilar materials is shown in Figure 4, in which the quantum well formation has been shown.

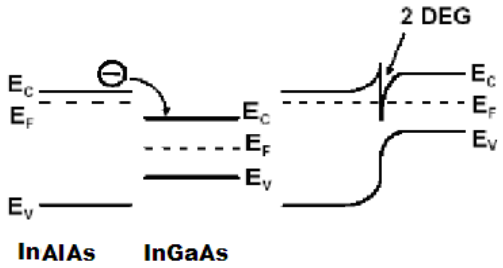

Fig.4. Energy Band diagram of HEMT showing 2DEG

In Figure.4 the 2DEG (two Dimensional Electron Gas) or quantum well is shown that formed at the interface in between InAlAs and InGaAs due to their bandgap difference. The high frequency behaviour is due to the separation of the carrier electrons from their donor sites at the interface between the doped InAlAs and undoped InGaAs layer, where these are confined to a very narrow layer in which motion is possible only parallel to the interface. The 2DEG or plasma is of very high mobility, up to $1.9*10^{12}$ cm^{-2}.

In the above InAlAs/ InGaAs pHEMT the channel layer was a 10 nm pseudomorphic $In_{0.7}Ga_{0.3}As$ layer whose Hall mobility and sheet carrier density were 7700 cm^2/Vs and $1.9*10^{12}$ cm^{-2} respectively. A 10 nm gate insulator was deposited to reduce the gate leakage current as well as to improve the I_D and g_m. A 10 nm Cr/100 nm Au gate electrode was formed to control the device performance. A 1 nm Si interface control layer was deposited to avoid the Fermilevel pinning problem and to decrease the surface state effects. The deposition of Si ICL is also used for reduce the current collapse, drain current drift and kink effects as well as to improve the device reliability.
The 1 nm InGaAs cap layer was developed for avoid the electron traps in the device. The 30 nm $In_{0.52}Al_{0.48}As$ wideband gap layer was formed and that same material 1 nm thin layer was developed for Si delta doping to improve the carrier concentration. The 5 nm $In_{0.52}Al_{0.48}As$ spacer layer was deposited to avoid the electron scattering. The 10 nm $In_{0.7}Ga_{0.3}As$ narrow bandgap layer was formed and used as a channel. The 10 nm $In_{0.52}Al_{0.48}As$ buffer layer was formed to avoid the substrate effects in the device. The devices had gate length L_G of 1 μm. In future T-gate will be designed for to reduce the parasitic element effects and to improve the RF performance.

III. RESULTS AND DISCUSSIONS

Fig. 5(a) shows I_{DS}–V_{DS} characteristics of the IG-PHEMTs with and without Si ICL. The insulated gate devices without Si ICL were very fragile.Thus, they could be characterized at only small drain voltages. Without Si ICL, the IG-PHEMT shows very poor gate controllability and small drain currents. The channel could not be pinched off either.

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These are due to existence of strong Fermi level pinning. The obtained maximum transconductance,g_m, of the device without Si ICL was 7 mS/mm.

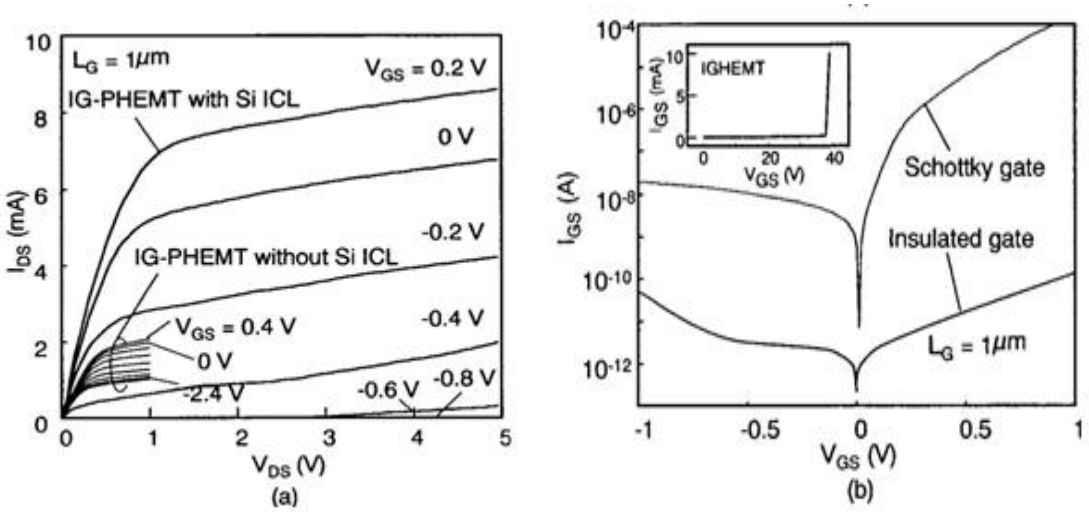

Fig. 5. (a) I_{DS} –V_{DS} characteristics of IG-PHEMTs with and without Si ICL.I_{DS}: drain current, V_{DS}: drain to source voltage, V_{GS} : gate to source voltage, and (b) gate leakage current characteristics of the IG- and SG-PHEMTs

On the other hand, insertion of the Si ICL dramatically improved the DC performance, showing excellent gate control and complete channel pinch-off. The maximum drain currents became 4 times larger than those of the IG-PHEMT without Si ICL. A maximum ransconductance of 197 mS/mm was achieved at V_G=0 V. This is 20 times larger than the best value of 7 mS/mm of the IG-PHEMT without Si ICL. All these improvements are due to the removal of the Fermi level pinning.Gate leakage currents of the IG-PHEMT with Si ICL and a SG-PHEMT are compared in Fig. 5(b).The best values of g_m of the conventional Schottky gate (SG)-HEMTs reported in the literature [7], [8] is 210–377 mS/mm for L_G= 1μm. Thus, the g_m value of 197 mS/mm obtained in the IG PHEMT device for L_G=1 μm is comparable to that of the SG-HEMTs.

The device showed high transconductance of 197 mS/mm even for a gate length of 1μm. As compared with the conventional Schottky gate PHEMTs, the gate leakage current was reduced by 4 orders of magnitudes and the gate breakdown voltage was increased up to 45 V. Well-behaved RF characteristics with the current gain cutoff frequency, f_T, of 12 GHz and the maximum oscillation frequency, f_{max} , of 45 GHz were obtained for the 1μm-gate-length device[9].

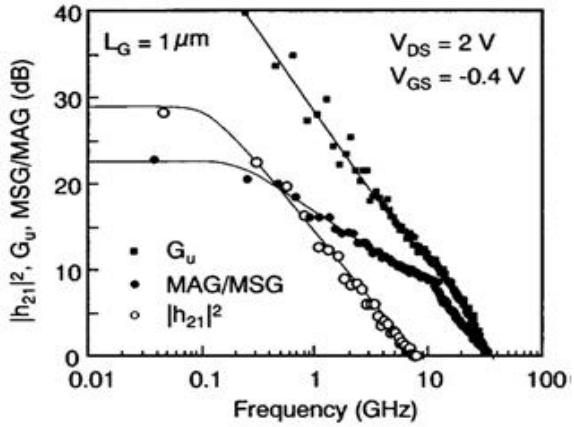

Fig.6.RF characteristics

Fig.6. shows the RF characteristics of the IG-PHEMT with Si ICL. The current gain cutoff frequency, f_T , was 12 GHz and the maximum oscillation frequency, f_{MAX} , was 45 GHz at V_G=-0.4V and V_{DS}=2V, respectively. Further

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improvement of RF performance should be also achieved by reducing the gate length to sub-micrometer and optimizing the gate design and insulator thickness.

A).EFFECT OF DIELECTRIC THICKNESS ON Si_3N_4 IG pHEMT

Fig.7. shows the measurement results of capacitance and the gate leakage current. The gate leakage current is decreased and the breakdown voltage is enhanced with increase of Si_3N_4 thickness.

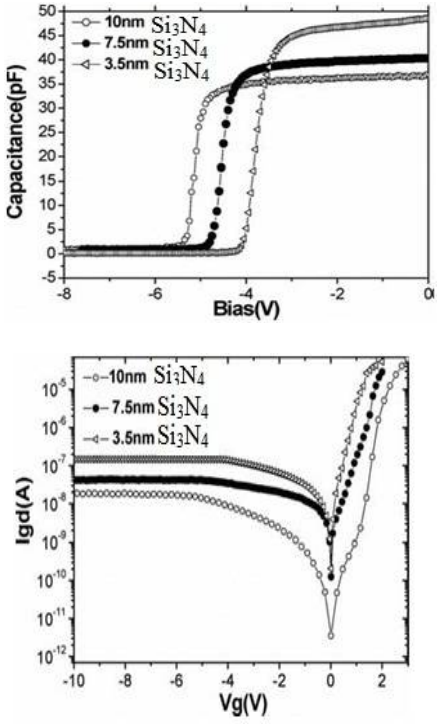

Fig.7.Effect of dielectric thickness on IG pHEMT

With an increased insulator thickness and decreased InAlAs thickness, where the gate capacitance is kept constant, a high transconductance was successfully obtained. Based on measurement results, the Si_3N_4 MOSHEMTs exhibited the best electrical characteristics, including the lowest gate leakage current, the lowest noise spectra density, and the high power performance. Through further decreasing the thickness of the gate oxide and optimizing the device with maximum transconductance was produced. In order to improve the performance of IG pHEMT many dielectrics have been used such as Al_2O_3,HfO_2,ZrO_2, HfSiON, HfAlON[12].

IV. CONCLUSIONS

In conclusion,a novel InAlAs/InGaAs insulated gate pseudomorphic HEMT (IG-PHEMT) utilizing a silicon interface control layer (Si ICL) was lucratively studied and its DC and RF performances were characterized. Gate leakage currents of the IG-PHEMT with Si ICL and a SG-PHEMT are compared. By introducing of Si ICL the on-state breakdown voltage increases substantially. The model will then be validated with simulation using tools such as TCAD. Further increase of g_m values to those comparable with commercial sub-micron SG-HEMTs seems potential by reducing the gate length. This paper also presents the research progress of gate dielectrics in IG pHEMT. The effects of thickness of gate dielectric on the characteristics of Si_3N_4 IG pHEMT are investigated. The thicker dielectric can decrease the gate leakage current.

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