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PWM Generator using Xilinx Vivado for IoT Applications

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ABSTRACT: Pulse width modulation (PWM) in power electronics control systems is not new, there are different approaches for developing pulse width modulation. Many digital circuits can generate PWM signals, but what is interesting is, to generate pulse width modulation using Hardware Description Language (VHDL) and implementing it on FPGA. PWM is used in many applications, ranging from communications to power control and conversion. PWM is commonly used to control the speed of electric motors, the brightness of lights, in ultrasonic cleaning applications, and many more. A pulse width modulation (PWM)generator component for use in CPLDs and FPGAs, written in VHDL. The component outputs PWM signals based on the duty cycle set by our logic. The center of each pulse occurs at the PWM frequency, and the pulse width varies around the center. To implement a PWM in VHDL, we need a simple counter. The PWM period is defined as the number of clock counters we want the counter count before restarting counting. When the counter value is less than PWM-width value the PWM output is high, else is low.

KEYWORDS: PWM, VHDL, FPGA, CPLD.

I. INTRODUCTION

PWM is a fundamental concept for control in power systems. Ideal PWM signals with zero delays of rise and fall times provide the best way of driving modern semiconductor power electronic devices. Precision and protection are important parameters in DC motor speed control and they can be achieved by using PWM. The width of the pulse controls the speed of the motor shaft by regulating its energy. Based on the PWM concept, if the duty cycle is changed to a sinusoid, a sinusoidal voltage will be generated at the output.

Some PWM methods are aimed at making better use of the DC bus voltage and thus increasing the modulation index. The pulse-width modulator is also an integral part of the feedback control loop andneeds to be properly modeled for control design.

The important property of PWM is that it has low power loss in switching devices and a high frequency that affects the device which uses power. Based on the property of PWM the following technique is adopted to implement PWM on a digital device.

PWM uses rectangular pulses where width is modulated by carrier signal resulting in the variation of the average value of the waveform. Figure 1 demonstrates the PWM concept where the width of the modulated signal is maximum when the carrier signal amplitude is maximum. Here the carrier signal is arbitrary but for the realization, a sine signal is used.

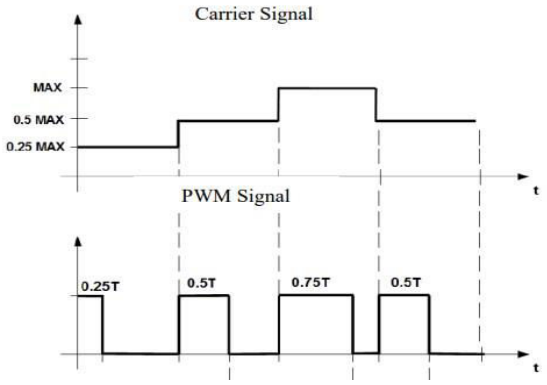

Figure 1. PWM Signal Representation

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Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects.FPGAs canbe reprogrammed to desired application or functionality requirements after manufacturing. This feature distinguishes FPGAs from Application Specific Integrated Circuits (ASICs), which are custom manufactured for specific design tasks. FPGA-based devices have less delay, flexibility in design, reduction in hardware, and more importantly, it is re-programmable.
Due to their programmable nature, FPGAs are an ideal fit for many different markets.

II. LITERATURE SURVEY

The architecture of the PWM Modulator is shown in fig.2 It consists of Digital Sine Generator, Frequency trigger, and FSM Module.

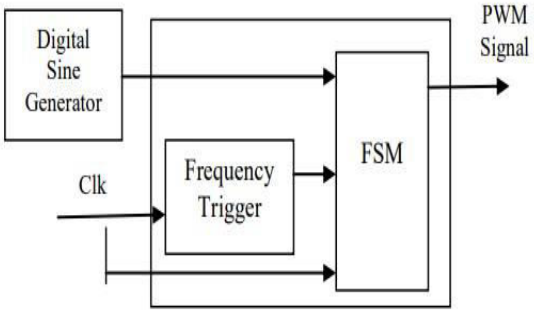

Figure 2. Block diagram for PWM Modulator[1]

A Digital Sine generator is used to generate digital values of the analog sine waves. A Frequency trigger is used to generate analog sine waves and is used in digital sine generators. The same module is used again to generate a higher frequency to get a proper PWM signal. FSM is a finite state machine that is the key module for generating variable pulse width.
Initially analog sine wave is generated and its digital representation is stored using a clock signal. Depending on the sine values the FSM will modulate the width of the pulse. VHDL programs are written for digital sine generators, frequency triggers, and FSM. Finally, a top-level module which is a PWM module is written comprising the above modules.

DIGITAL SINE GENERATOR

This module will generate a digital representation of an analog (sine) signal with desired frequency. It will use the counter values as addresses to fetch the next value of the sine wave from the ROM. In this paper, a VHDL package with a parameterized sine signal is designed. To represent sine wave 256 unsigned amplitude values are used for one sine period that will be stored in a ROM array. VHDL package is a way of grouping related declarations that serve a common purpose. Each VHDL package contains a package declaration and package body.

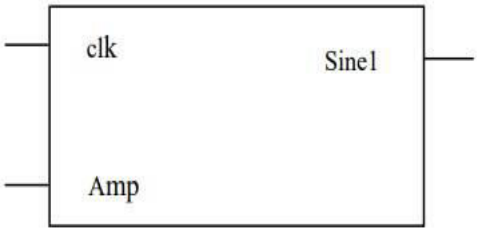

Figure 3. Block diagram for Digital Sine Generator[1]

FREQUENCY TRIGGER

This module is used in a digital sine generator and used separately before FSM to generate a PWM signal. The main purpose of this module is to generate a sine signal of the desired frequency.

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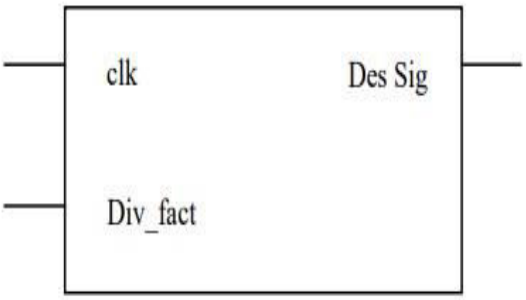

Figure 4. Block diagram for Frequency Trigger[1]

The same frequency trigger is used before FSM to generate higher frequencies to regulate the PWM output.

FSM

The FSM module will generate the PWM signal. It will generate the PWM signal with the correct duty cycle for each period PWM Digital Signal Sine Generator FSM Frequency Trigger Clk clk Div_fact Des Sig clk Amp Sine1. FSMs are important to specify sequential machines with states, inputs, and outputs. FMS can be a Mealy or Moore machine. Design can be carried out easily if the system is defined in terms of FSM.

III. PROPOSED METHODOLOGY

The architecture of the PWM Modulator is shown in Figure 2. It consists of a 4-bit Counter internally to increase or decrease the duty cycle.

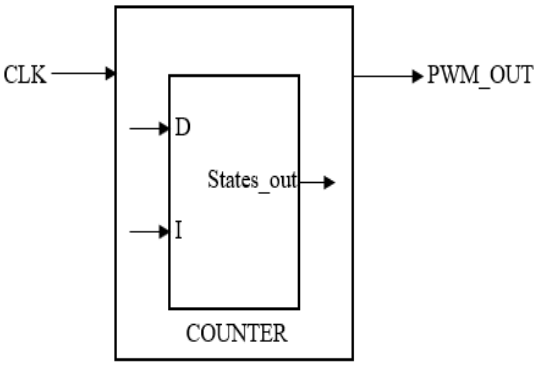

Figure 5. Block Diagram for PWM Modulator

VHDL program is written for Counter. Finally, a top-level module which is a PWM module is written comprising the above modules.

COUNTER

Initially, we generate a 4-bit counter that gives the output of a square wave with a certain period. This counter is placed internally inside the PWM Generator consisting of two inputs (I & D) as inc_width and dec_width and an output States_out. When we apply input 1 to the dec_width the period of the square wave pulse decreases and on further applying input 1 to the dec_width the perioddecreases accordingly. when we apply input 1 to inc_width the period of the pulse increases accordingly. we can't decrease or increase the period continuously, if we need to decrease or increase, we need to provide input 0 before the action is performed.

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STATES

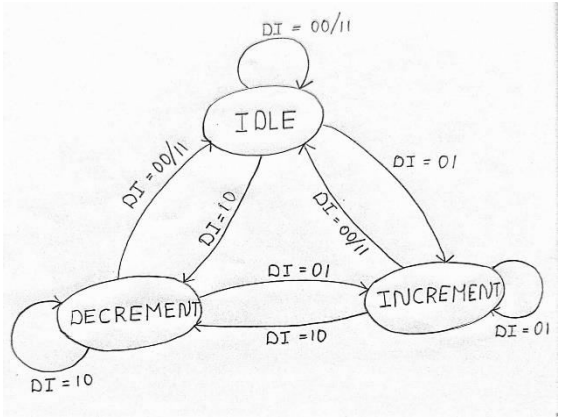

Figure 6. State diagram

```
case state is
when idle=> if d='0' and i='1'then next_state<=inc;
elsif d='1' and i='0' then next_state<=dec;
else
next_state<=idle;
end if;
when inc=> if d='0' and i='1' then next_state<=inc;
elsif d='1' and i='0' then next_state<=dec;
else
next_state<=idle;
end if;
when dec=> if d='0' and i='1' then next_state<=inc;
elsif d='1' and i='0' then next_state<=dec;
else
next_state<=idle;
```

IMPLEMENTATION

The entire system is realized using the Xilinx tool. Initially, VHDL programs are written for counter and top-level modules for PWM. Then constraints file with the pin out and area constraints and timing constraints is added to the top module file. All the files are simulated and finally, the top module is verified for its functionality.

The simulated top module file along with the constraints file is synthesized for generating a gate-level netlist. The RTL schematic and Technology schematic files are used to interpret the design. Then the synthesized file is translated, mapped, and routed according to the device. At each step of synthesis and implementation, reports are generated to describe the hardware structure of the FPGA device. Later bitstream file is generated and dumped into the FPGA. The functionality of the module in FPGA can be verified by using chip scope pro. If the target device is changed then the entire process is to be repeated from synthesis. Synthesis is a device-specified process. It generates reports based on the target user.

IV. RESULTS

The Design entry of PWM is done using VHDL and simulated using Xilinx Vivado. The design is synthesized using the Xilinx synthesis tool and implemented on FPGA Board.

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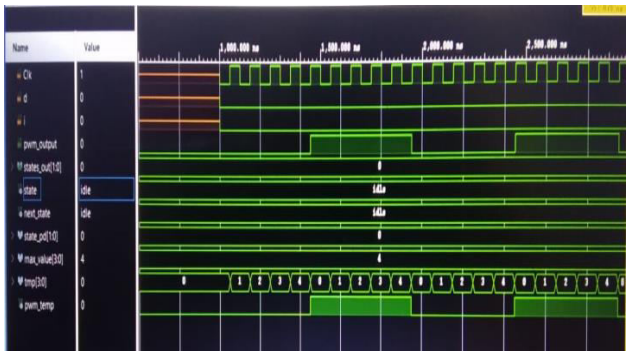

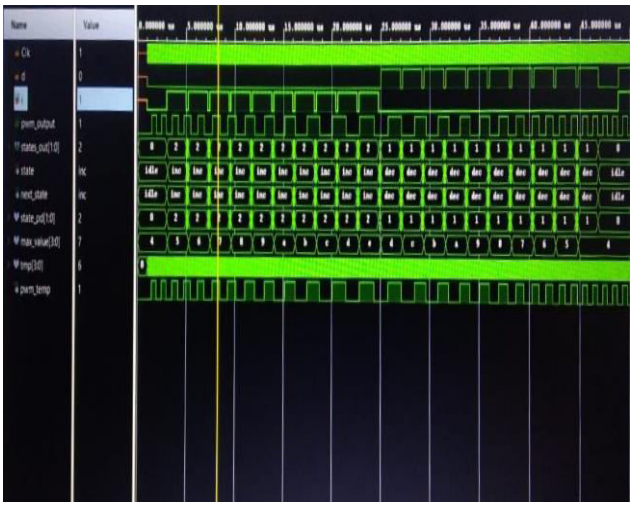

V. CONCLUSION

In this paper, a hardware realization of the PWM modulator is presented. PWM modulator has more importance in power electronics and thus needs more accuracy and flexibility in the implementation. In this paper, a VHDL code is written for PWM and the results show that accurate PWM pulses can be generated using this method.This PWM generator, as per the synthesis done, uses less LUT in an FPGA and it's a compact one. Further, it can also be concluded that the power consumption is also less as it uses fewer LUTs.

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