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Novel Design of Low Power Barrel Shifter using Reversible Logic gates for DSP Applications

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ABSTRACT: Modern Digital VLSI System Design, demands innovative design methodologies to fabricate the complex electronic circuit on a single chip. Optimizing and achieving an efficient system design requires keeping up to date with emerging VLSI technologies. And it is more important for a design engineer to optimize the performance, power, area, and cost. In the view of performance, power, and reversible logic would probably catch up to the nascent technology. Simply our project constitutes the design of a Barrel shifter by dint of the formerly mentioned technology. It's been experimented with and researched in three methodologies of which was examined using GPDK 45nm technology and the next was tried independent of technology using Xilinx Vivado. Finally, it has been implemented using Basys 3 Artix-7 FPGA board to test out the functionality of our proposed design. Reversible circuits that implement digital circuits have low latency and reduced power dissipation. It can retrieve its input back from the received output. Because of this, these are highly prevalent in Quantum Computing and Cryptography due to their reversible nature. The conventional way of designing a Barrel shifter has an array of multiplexers that are connected concerning its shift distance. Our proposed design has been tested with reversible multiplexers instead of multiplexers. The outcome of the research prevailed least power consumption.

KEYWORDS: Barrel shifter, Reversible Logic Gates, Cadence Virtuoso, Xilinx Vivado

1.INTRODUCTION

Barrel shifters are important components in Arithmetic Logic Units (ALUs) and are widely used for shift operations such as shift right logical, shift left logical, shift left arithmetic, shift right arithmetic, right rotate, and left rotate. The architecture of a barrel shifter can be designed using 2:1, 4:1, 8:1, or 16:1 multiplexer (MUX) trees. Barrel shifters are particularly critical elements in digital signal processing (DSP) applications.

To reduce power consumption, the barrel shifter is designed using MUX trees that allow for its repetitive use. The MUX trees are used to select the appropriate bit positions based on the control signal that specifies the shift distance. The input binary number is loaded into shift registers, which are connected to the MUX trees. The MUX trees control the output of the shift registers, selecting the appropriate bit positions based on the shift distance specified by the control-signal.

Barrel shifters are widely used in cryptographic algorithms such as Advanced Encryption Standard (AES) for bitwise operations on the input data. In microprocessors, barrel shifters are used to perform shift and rotate operations on binary data, such as shifting a value into a register or rotating a value to the left or right. In DSP, barrel shifters are used in signal processing applications to shift and rotate data, such as in Fourier transforms.

II. BARREL SHIFTER

An 8-bit barrel shifter is a digital circuit that can shift an 8-bit binary number by a variable number of bits in a single clock cycle. It can perform both logical and arithmetic shifts, as well as rotate operations, such as left and right rotates.

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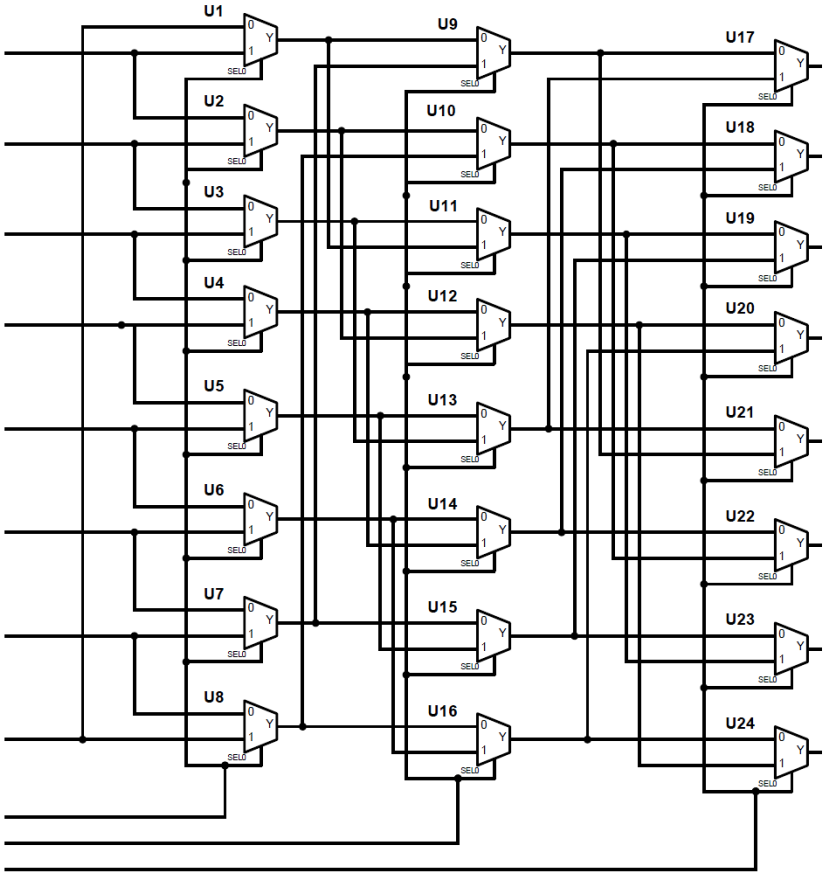

Fig.1 Design of 8-bit mux based right rotator

The shift distance is determined by a control signal, which can be either a fixed value or a value stored in a register. In digital systems, an 8-bit barrel shifter can be implemented using a combination of multiplexers and shift registers. The input binary number is first loaded into a set of 8 shift registers, one for each bit of the input. The output of each shift register is then connected to a set of multiplexers, which are used to select the appropriate bit positions based on the shift distance specified by the control signal.

Another way to implement an 8-bit barrel shifter is to use a series of 2:1 MUXes in a ripple-carry fashion. In this approach, the input binary number is first loaded into a set of shift registers. Each bit of the input is then connected to a series of 2:1 MUXes that select the appropriate bit position based on the shift distance. The output of each MUX is then connected to the input of the next MUX in the chain, allowing the shifting operation to propagate through the circuit.

III. 2:1 MUX OPERATION

A 2:1 multiplexer (MUX) is a digital circuit component that selects one of two input signals and forwards it to the output based on a control signal. The control signal determines which input is passed through to the output. "2:1" refers to the MUX has two input signals and one output signal.

The operation of a 2:1 MUX can be represented by the following truth table:

S0	Output (Y)
0	I0
1	I1

Boolean expression for the 2:1 Mux output be $Y=S_0'.I_0+S_0.I_1$

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When the control signal is 0, the MUX selects Input 1 and passes it through to the output. When the control signal is 1, the MUX selects Input 2 and passes it through to the output.
2:1 MUXes can be combined in a hierarchical fashion to create larger multiplexers with more inputs. For example, eight 2:1 MUXes can be combined to create an8:1 MUX, which can select one of eight input signals based on a three-bit control signal.

IV. REVERSIBLE LOGIC GATES

The R gate is a 3x3 reversible gate with three inputs (A, B, C) and three outputs (P, Q, R). In the reversible R gate, the output function for P is simply the input A. The output function for Q is the product of A and B, which is denoted as AB. The output function for R is a more complex function that involves two logical operations. The first operation is the complement of B, denoted as B'. The second operation is the AND operation between the complement of B and C, which is denoted as B'C. Finally, the output of this operation is added to the product of A and C, which is denoted as AC.

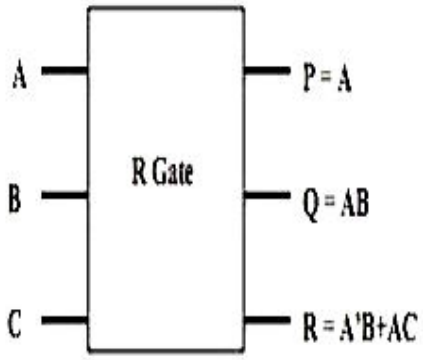

Fig.2R Gate

The output functions for this circuit are defined as P = A, Q = AB, and R = A'B + AC.

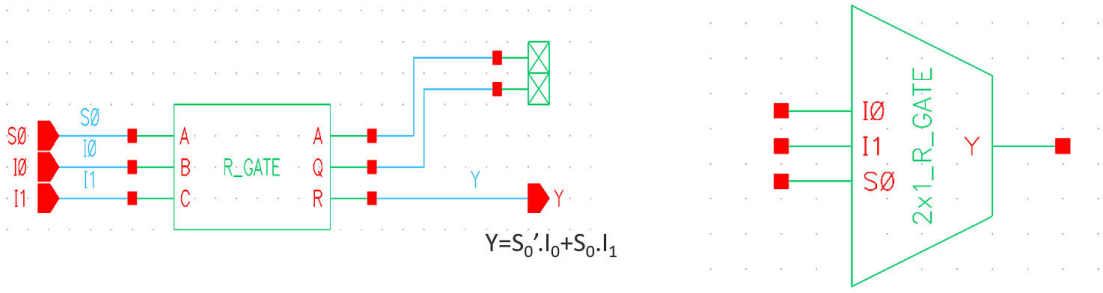

Fig.3 Design of 2:1 Mux using R gate (Rg Mux)

In the implementation of a 2:1 mux (Rg Mux) using the R gate, the conventional output of the 2:1 Mux is obtained through the reversible Rgate if and only if the first input is given by the select line(S0), next two inputs by the inputs itself.The first two outputs of the R gate (P and Q) are considered as garbage outputs, while the final output (R) is used as the output Y of the multiplexer.

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V. PROPOSED DESIGN OF BARREL SHIFTER

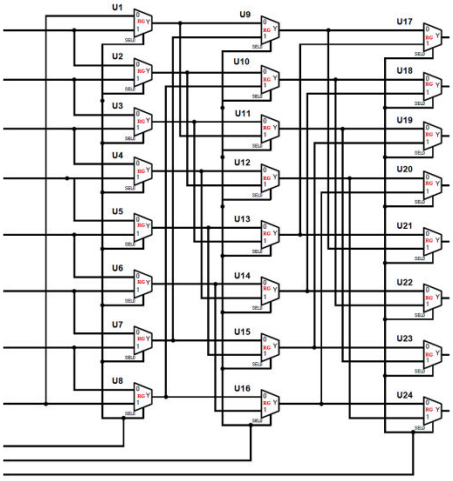

Fig.4 Design of 8-bit barrel using RgMux

As mentioned earlier the conventional barrel shifter has been replaced by the reversible Rg Mux instead of cascaded multiplexers. In this proposed design functionality doesn't change but only advantage is the input can be retrieved.

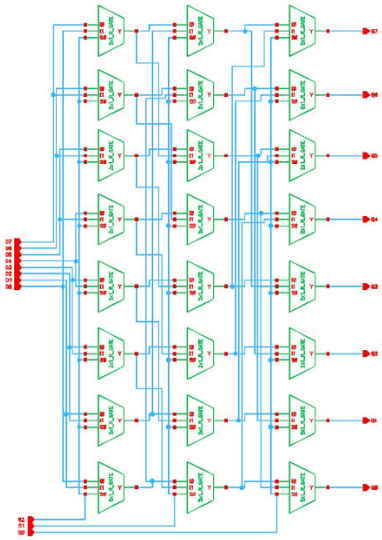

Fig.5Implementation of Rg Mux

The above figure depicts the implementation of Rg Mux based 8-bit right rotator using Cadence Virtuoso schematic edit with GPDK 45nm technology. This is been tested for validation and power has been logged for analysis.

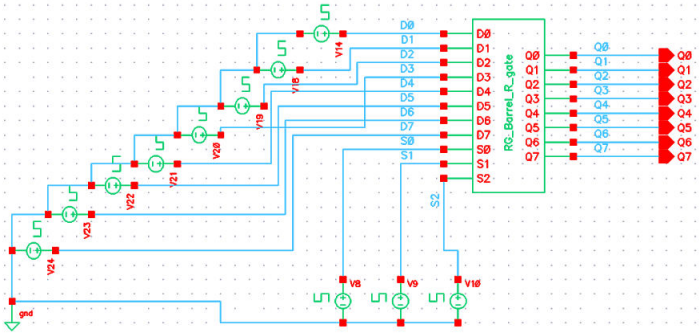

Fig.6Testbench of the Rg Mux based barrel shifter

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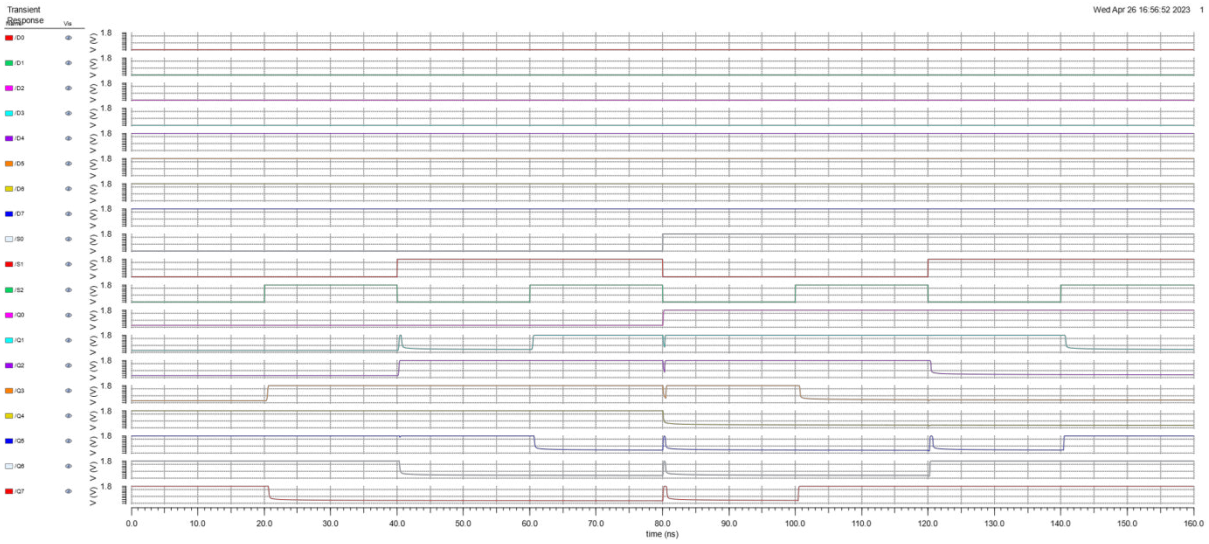
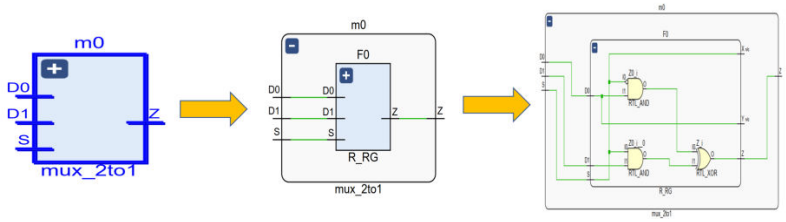


Fig.7Output waveform for the Rg Mux based right rotator

In order to spotlight the obtained result, we use Xilinx Vivado for implementing the result in the Basys 3 Artix 7 FPGA board with the help Verilog HDL, which is technology independent.



Top Module 2:1 Mux using R gate R gate

Fig.8Hierarchical representation of module top

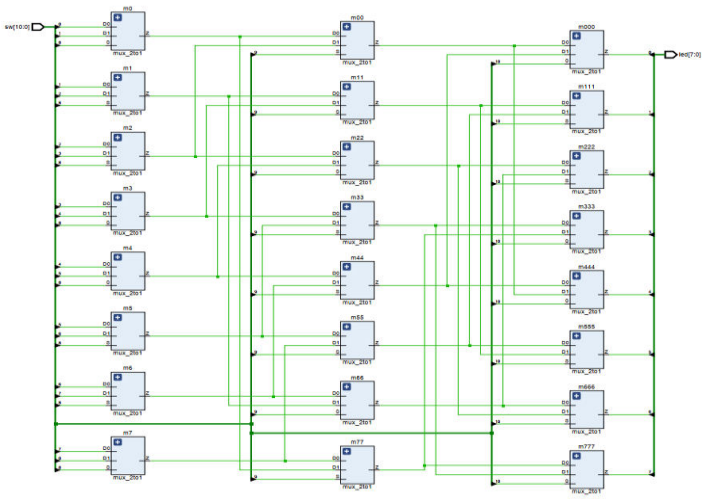


Fig.9 Schematic of 8-bit right rotator in Xilinx Vivado

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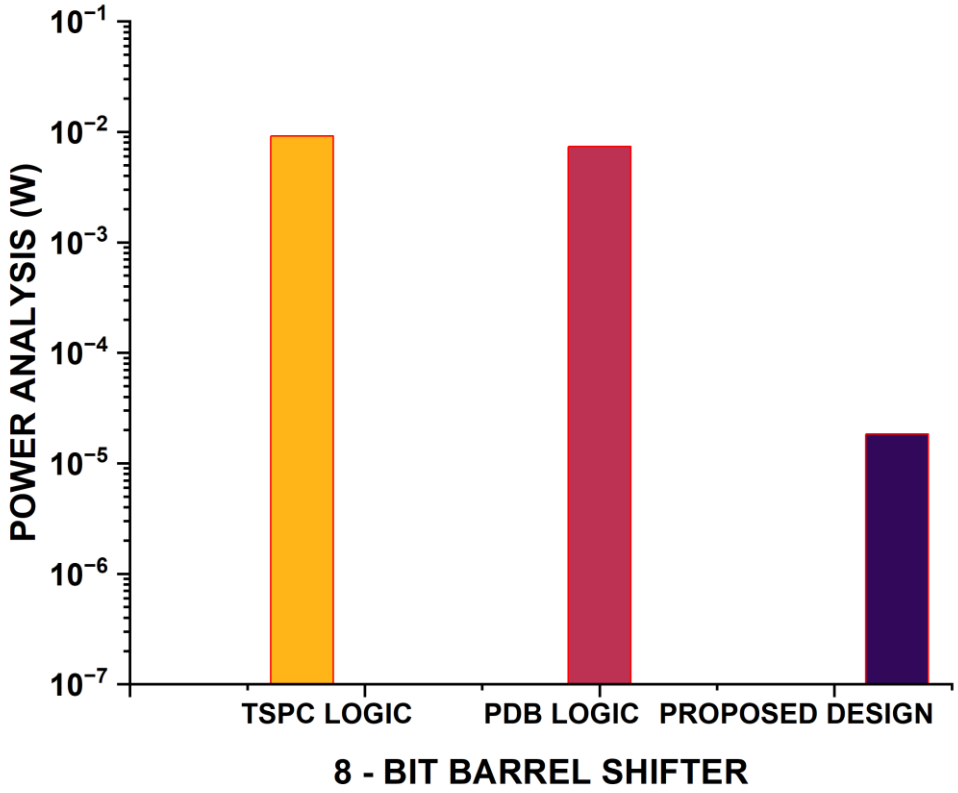
Average power analysis of existing and proposed 8-bit Barrel shifter using 45nm technology:

POWER ANALYSIS	EXISITNG		PROPOSED
	TSPC LOGIC	PDB LOGIC	
BARREL SHIFTER	9.1756mW	7.3944mW	18.41µW



VI. CONCLUSION

This paper examined the outcome of multiplexers-based barrel shifter with the help of reversible logic gates in contrast to the conventional TPSC and PDB based mux design. The result and power analysis depicts that our proposed design consumes very less power in comparison with the traditional. Our proposed design achieved 200% efficiency comparing to the existing design. Thus, this proposed design can be used in low power application in DSP application and other VLSI digital system designs.

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