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Design and analysis of Low-Power Multiplier using Fixed-width Replica Redundancy Block

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ABSTRACT: The RPR outlines in the ANT plans can work in a quick way, however their hardware complexity is excessively intricate. Therefore, the RPR plan in the ANT outline is still the most prominent configuration simplicity. However, receiving with RPR ought to even now pay additional area overhead and power utilization. In this paper, we assist proposed a simple way utilizing the altered width RPR to supplant the full-width RPR block. Performance evaluation is done using generating comparison graphs for average truncated error, power utilization and delay.

KEYWORDS: Irradiance, Output power, PV characteristics, Solar Panel, Solar energy, Temperature.

I. INTRODUCTION

Multiplication is a complex arithmetic operation, which is reflected in its moderately high signal engendering delay, high power dispersal, and expansive area necessity. To bring down the power dispersal, supply voltage scaling is generally utilized as a viable low-control procedure since the power utilization in CMOS circuits is relative to the square of supply voltage. Be that as it may, in profound sub micrometer process advancements, clamor impedance issues have raised trouble to outline the solid and productive microelectronics frameworks; henceforth, the configuration procedures to improve commotion resistance have been generally grown in any case, the RPR plans in the ANT plans are planned in a modified way, which are not effortlessly received and repeated.

The RPR designs in the ANT designs can work in a quick way; however their hardware complexity is too complex. Therefore, the RPR outline in the ANT configuration is still the most famous configuration on account of its effortlessness. Notwithstanding, embracing with RPR ought to at present pay additional region overhead and power utilization [1]. In this research work, we assist proposed a simple way utilizing the settled width RPR to supplant the full-width RPR square. Utilizing the settled width RPR, the calculation error can be remedied with lower power utilization and lower zone overhead. This asset waste could halfway be helped by having a few multipliers, each with a particular piece width, and utilize the specific multiplier with the littlest piece width that is sufficiently huge to oblige the present augmentation. Such a plan would guarantee, to the point that an augmentation would be figured on a multiplier that has been advanced as far as power and defer for that particular bit width [2].Mobile Ad Hoc Networks (MANETs) consists of a collection of mobile nodes which are not bounded in any infrastructure. Nodes in MANET can communicate with each other and can move anywhere without restriction. This non-restricted mobility and easy deployment characteristics of MANETs make them very popular and highly suitable for emergencies, natural disaster and military operations.

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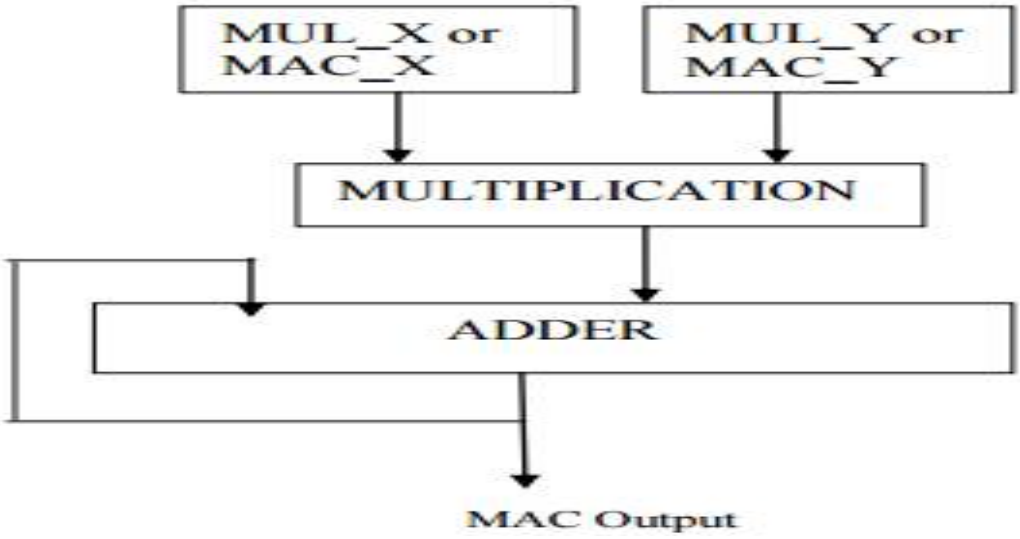

Fig.1: Multiplier architecture for RPR [3]

An ANT-based framework, Algorithmic Soft-Error Tolerance (ASET) is made out of an error control obstruct that identifies and revises errors in the fundamental capacity square has been created. Since the number arithmetic units utilized in Digital Signal Processing (DSP) frameworks depend on Least Significant Bit (LSB) first calculation, errors seem first in the Most Significant Bit (MSB), bringing about errors in a huge accuracy [3].

Choiet al (2000) proposed an idea called Partially Guarded Computation (PGC), which isolated the number-crunching units, e.g., adders, and multipliers, into two sections, and killed the unused part to minimize the power utilization. The reported result demonstrated that the PGC can decrease power utilization in an exhibit multiplier yet with area overhead [4].

Objectives of the thesis are as follows:

- To design a low power and fault tolerant multiplier using RPR.
- To define further the implementation of fault tolerance using RPR.
- To propose a multiplier design that involves significantly less area and less delay.
- The algorithms are modeled in VHDL and have been implemented in ModelSim and synthesized and simulated using Xilinx software.

II. POWER REDUCTION TECHNIQUE

Proposed approach is based on following studies:

A. SLEEP METHOD

In the rest approach, a rest" PMOS transistor is put in the middle of VDD and the draw up system of a circuit and a rest" NMOS transistor is put between the draw down system and Ground. These rest transistors turn off the circuit by removing the power rails. The rest transistors are turned on when the circuit is dynamic and killed when the circuit is unmoving. By removing the power source, this system can lessen leakage control successfully [5].

B. SLEEPY STACK METHOD

Another procedure for leakage power decrease is the stack approach, which controls a Stack impact by separating a current transistor into two half size transistors. The separated transistors build defer altogether and could confine the helpfulness of the methodology. The languid stack approach joins the rest and stack approaches. The drowsy stack procedure separates existing transistors into two half size transistors like the stack approach. At that point rest transistors are included parallel to one of the separated transistors. Amid rest mode, rest transistors are killed and

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stacked transistors smother leakage current while sparing state. Every rest transistor, set in parallel to the one of the stacked transistors, diminishes resistance of the way, so defer is diminished amid dynamic mode [6].

C. DUAL SLEEP METHOD

Another procedure called Dual rest approach utilizes the upside of utilizing the two additional draw up and two additional draw down transistors in rest mode either in OFF state or in ON state. Following the double rest segment can be made normal to all logic hardware; less number of transistors is expected to apply a specific logic circuit [7].

D. DUAL STACK APPROACH METHOD

In this area, the structure and operation of our novel low-leakage power design is depicted. It is additionally contrasted and understood past methodologies, i.e. the drowsy stack, double rest and rest transistor strategy. Here we utilize 2 PMOS in the draw down system and 2 NMOS in the draw up system. The transistors are held backward body predisposition. Subsequently their limit is high. High limit voltage causes low leakage current and henceforth low leakage power [8].

III. PROPOSED WORK

Proposed work involves major two steps as follows:

A. LAYOUT DESIGNING

In this work we have designed a new 1-bit 10-transistor full adder which consumes less power than the standard implementations of full adder cell. The proposed adder is tested and compared with the high transistor count and existing 10-transistor adders under the same conditions [9]. The addition of 2 bits A and B with C outputs a SUM and a CARRY bit. The integer equivalent of this relation is shown as

SUM = (A B).C + (A B).C --- (1)
CARRY = (A B).C + (A B).A--- (2)

The proposed adder implements equations (1) and (2) using complementary CMOS and MUX based design logic with only 10 transistors. The adder is useful in larger circuits such as multipliers despite the threshold problem. The number of direct connections from VDD to the ground is reduced in the new design to minimize the power consumption due to short circuit current. Also the generation of SUM from CARRY is avoided as in the CMOS adder. The adder uses internally generated signal (A XOR B) and (A XNOR B) to control the output transistor gates. The same (W/L=5λ / 2λ) ratio is used for all the designs and our design is compared on the same platform in 70nm technology in MICROWIND [10].

The SUM and CARRY signals are generated separately after the generation of (A XOR B) so as to reduce the delay. In the design, the second CMOS inverter in the critical path of the generation of the SUM helps in reducing the threshold loss. Performance analysis of all the adder designs is carried out in 90nm, 70nm and 50nm CMOS technology in MICROWIND. The performance is studied at power supply voltage of 1.0V for 90nm and 0.7V for 70nm at frequencies of 50MHZ [9].

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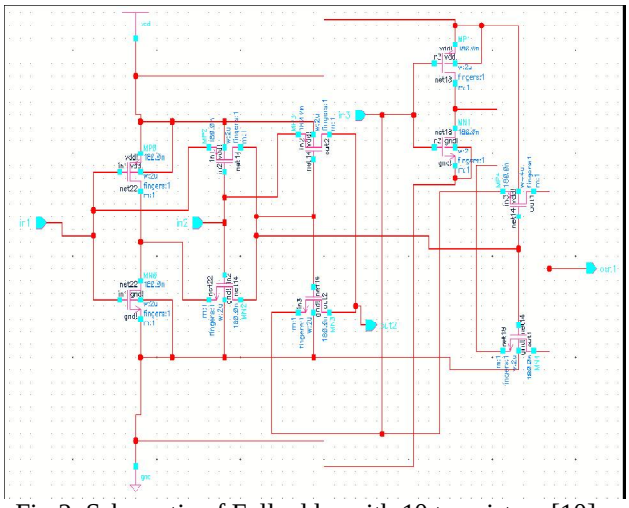

Fig.2: Schematic of Full adder with 10 transistors [10]

B. ALGORITHMIC NOISE-TOLERANCE

An ANT-based DSP framework has a principle DSP (MDSP) hinder that processes in vitality effective way however makes irregular errors [11]. It acknowledges as its info the sign z[n] + sn[n], where z[n] is the information sign and sn[n] is the info signal clamor. The uproarious output of the MDSP square is meant by y'[n]. Generally, the MDSP square gives up clamor invulnerability for vitality productivity. The EC square watches the boisterous output y'[n], and the information z[n] + sn[n] and maybe certain inward MDSP signs to recognize and remedy errors. The last revised output of the ANT-based framework is signified as ŷ[n]. The error control (EC) piece works in an error freeway yet expends fundamentally more vitality per operation than the MDSP block [12].

$$y'[n] = \sum_{k=0}^{N-1} h_k x[n-k] + \eta[n]$$
$$= y[n] + \eta[n]$$

where y[n] is the error free output and η[n] describes to the appearance of DSM clamor at the algorithmic level on a for every (output) test premise. We now portray a case to delineate the ANT concept [13].

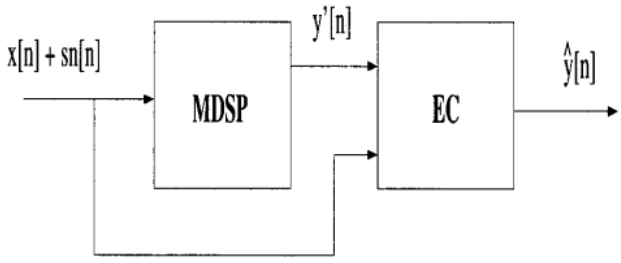

Fig. 3: ANT based DSP system [14]

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IV. SIMULATION RESULTS

Results of our proposed technology will be like following below figures:

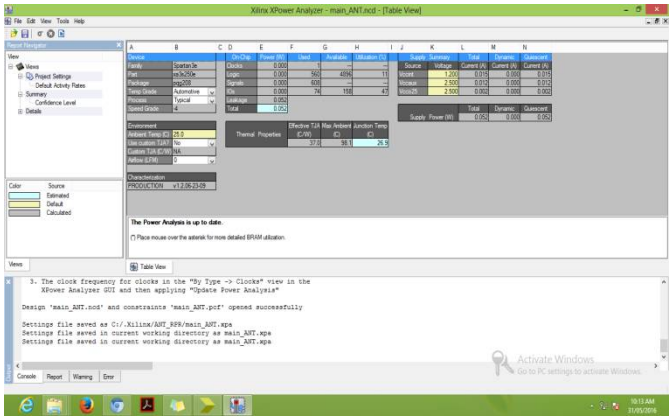

Fig. 4: ANT RPR Power calculation (P= 0.052W)

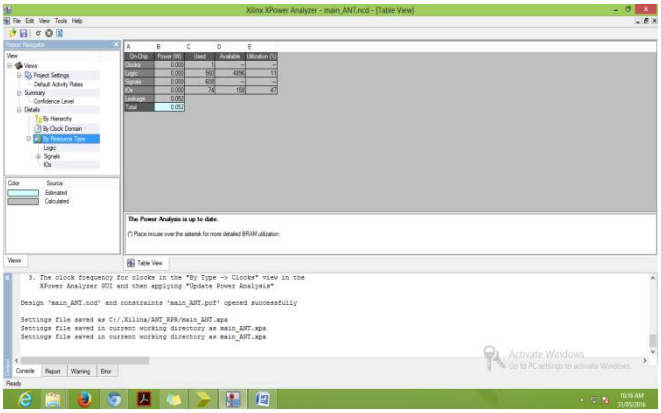

Fig.5: Logic and I/O utilization in %

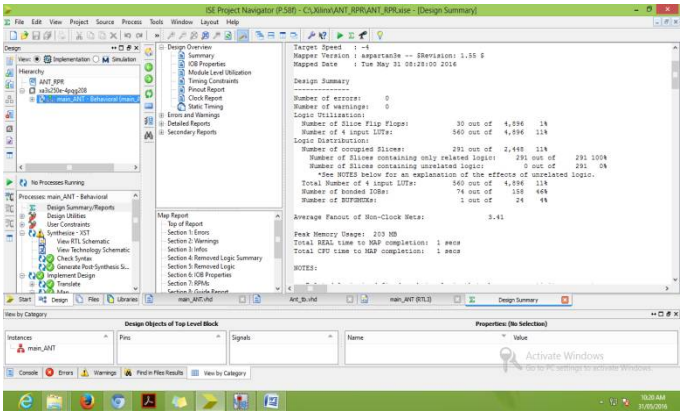

Fig.6: Design summary

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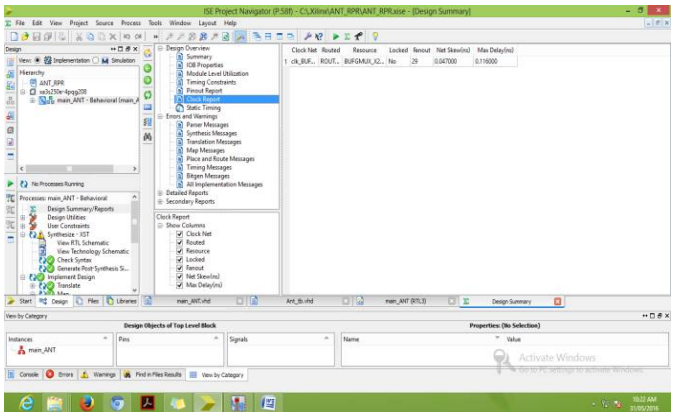

Fig.7: Maximum delay 0.116ns

Following are designs of multipliers:

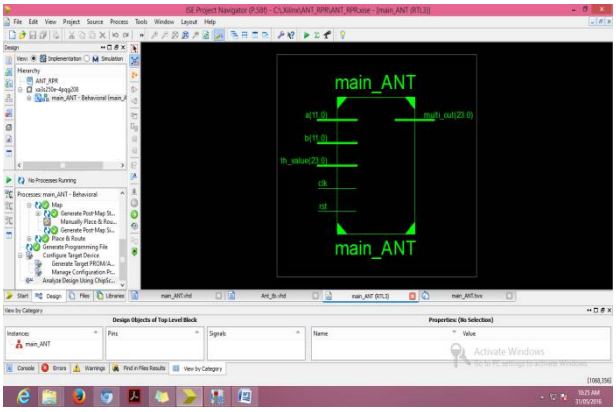

Fig.8: Main ANT architecture

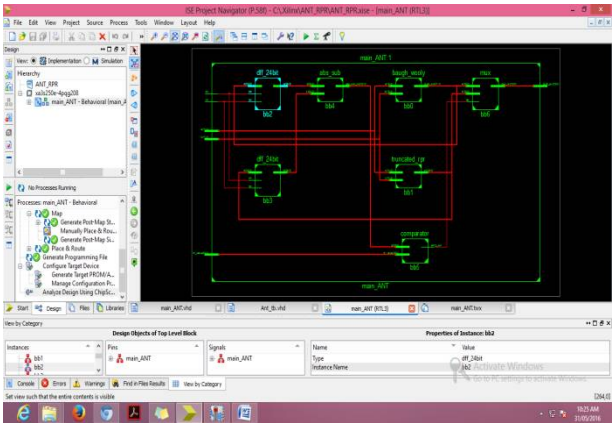

Fig.9: Inside view of ANT RPR architecture

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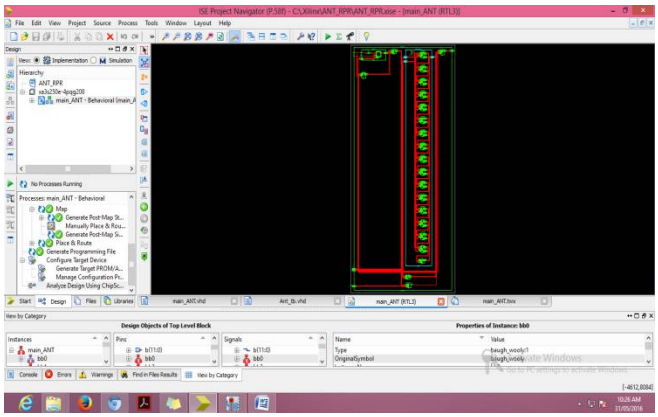

Fig.10: Bough Wooley multiplier

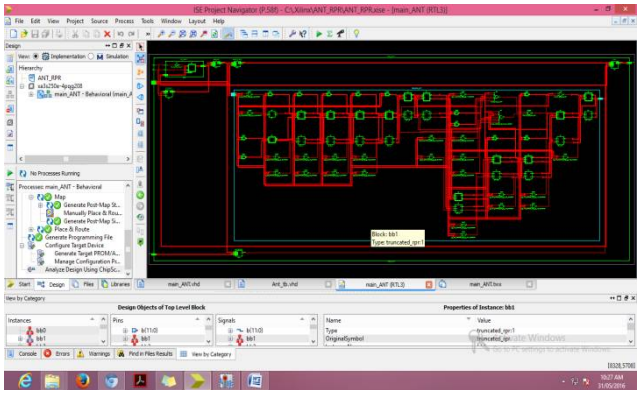

Fig.11: RPR architecture

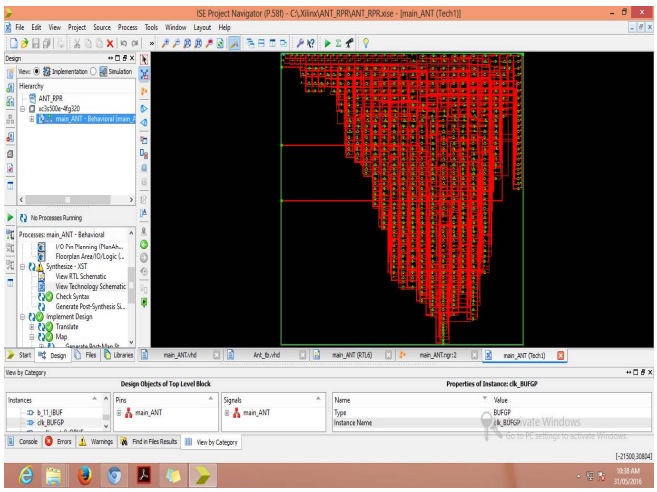

Fig. 12: Technology schematic of ANT RPR

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Performance graph:

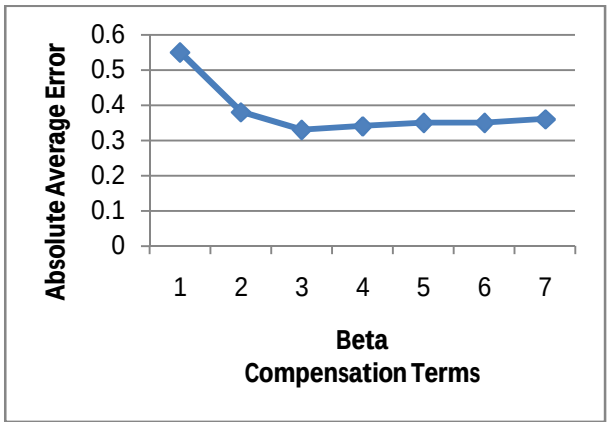

Fig. 13: Performance graph for Absolute Average error vs. Compensation terms

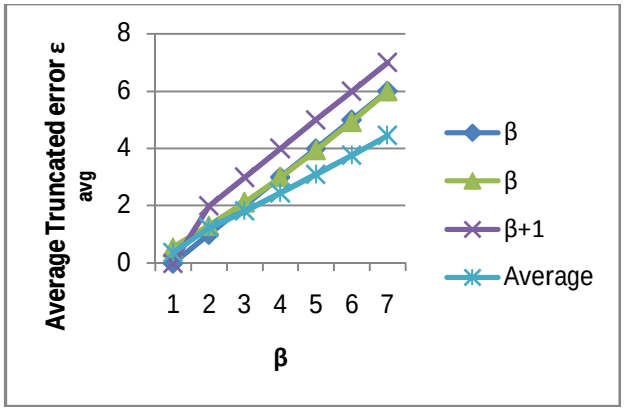

Fig.14: Performance graph for Average truncated error vs. β

Performance for power calculation is shown in table I below:

Table I: Performance for power calculation

On clip	Power calculation (P)	Used	Available	Utilization %
Clocks	0	1	0	-
Logic	0	560	4896	11
Signals	0	608	-	0
IOs	0	74	158	47
Leakage	0.052	0		

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Performance for delay calculation is shown in table II below:

Clock Net	Routed	Resource	Locked	Fanout	Net Skew (ns)	Max. Delay (ns)
Clk_BUF	ROUTE	BUFGMUX_X2	No	29	0.047	0.116000

V. CONCLUSION AND FUTURE WORK

In order to assess the execution of configuration, we need to think about the execution of this settled width RPR plan with past full width RPR outline. The outline is combined by utilizing Xilinx 8.1V.based on this alteration delicate advanced sign preparing frameworks that devour a great deal less power than frameworks working error free at basic supply voltages. As experimental results power utilization increases to 52% more and delay reduced to 33% (minimum delay calculated is 0.116 ns). Absolute truncated error decreases as per β values.

As a direction for future work, we focus on the multi-layer fault-tolerant design.In addition, RPR can be applied outside of SRAM-based FPGA systems, just as TMR has been in many instances.

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BIOGRAPHY

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