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Design of 3 Bit QCA PIPO Shift Register Using D-Flipflop Circuits

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ABSTRACT: Quantum-dot Cellular Automata (QCA) is a beyond micro scale development for better utilities to CMOS technology. QCA became more prominent as its size provided the benefit of less power consumption and fast switching compared to CMOS technology. In this paper, we have presented a new 3 –bit Parallel Input Parallel Output (PIPO) shift register using D- Flipflop circuits. The circuits are made using QCA Design software of version 2.0.3. The design presented has a total of 117 cells and has an area of 0.14um^2. Because of the small are they are likely to be the complete replacement for CMOS technology in the future where nano technology is used everywhere.

KEYWORDS: Parallel-Input-Parallel-Output (PIPO), Quantum-dot Cellular Automata (QCA), D-Flipflop

I.INTRODUCTION

According to the human needs device dimension is sinking day by day, for example we compared to first computer and present laptop. General CMOS-based transistor technology has severe obstacles because of technological physical obstacles such ultra-thin gate oxides, short channel effects, leakages and excessive waste of power at nano-scale regimes. A completely different computer platform for the design of digital logic systems is needed for the present society, Quantum Dot Cellular Automata is an alternative quantum phenomenon, with a quantum dot confined to the possibility of efficiently processing and transferring information nanoplate. Quantum-dot Cellular Automate (QCA) is the technique of computing. Its benefits are highly tempting, for example smaller sizes, reduced energy usage and faster speed.

QCA is extremely small and may be carried out in a wide range of material systems. It is now best alternative to VLSI CMOS. In traditional numerical systems, data is conveyed by electrical current from one location to another whereas QCA cells transmit information through the propagation of the state of polarization. This project provides a comprehensive design and modelling of basic D- flop and 3-bit parallel in parallel out (PIPO) circuits for quantum dot cellular automata. The objective is to optimize the circuit density and to concentrate on a minimum cell architecture. In addition, unlike the preceding constructions, these designs do not require crossover wire. QCA designer is used to evaluate and simulate the suggested circuits, typical QCA layout and verification tool.

II.OVERVIEW ABOUT QCA

2.1 QCA CELL

QCA is mostly based on a cell. Appropriate load setup is provided in each cell. It consists of 4 quantum points and 2 charges of electrons. The power of Colombia's repulsion can only diametrically oppose the two electrons to two quantum locations.

A QCA cell has four points and one electron each is diametrically opposite in two of four places. This asks why electrons occupy the opposing or diagonal corner of quantum points In response to this question, it is sufficient to have a concept of Coulomb's repulsion principle, which is less effective when in neighboring quantum points with regard to electrons. The points are linked via tunnel crossings.

This allows two configurations to be highlighted by the internal impact of a cell, each using a binary state "0" or "1." A QCA topology is a QCA pavement. The cell contact allows information to be sent which allows the physical connections of

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devices to be replaced. From the input into the output of the QCA cell only the information (logic 0 or logic 1) may transmit by using the repellents force.

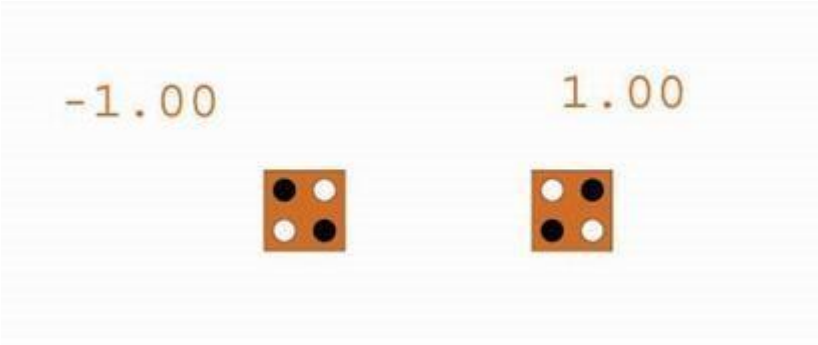

Fig1: QCA cells with -1 and +1 polarities respectively

2.2QCA GATES

2.2.1 QCA GATES – INVERTER GATE

The physical interactions between cells and cell-cell coupling can be utilized to achieve basic Boolean logic functions. A wire is formed by connecting cells in a straight line. The input polarization is fixed, as is the polarization, and the remainder of the cells' polarization is permitted to rest as well by reducing the barriers. An inverter is formed when the cells of a wire are rotated 45 degrees from the input cell.

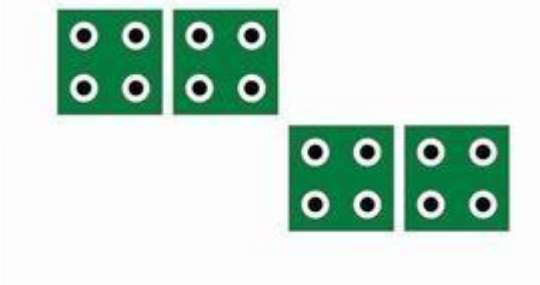

Fig2: QCA Inverter Gate

2.2.2 QCA GATES – MAJORITY GATE[12]

The polarity of the center cell is determined by the input cells of the Majority Voter, and the output generated is the Majority Voted Polarity. The universal gate of QCA Logic is the majority gate. By setting the input polarity of one input to +1 and -1, it may be utilized as an OR and AND gate respectively.

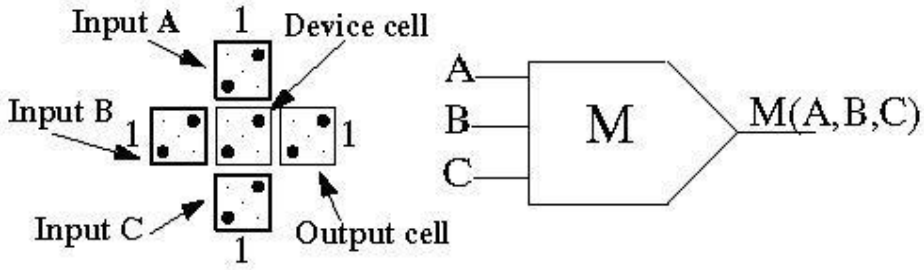

Fig3: QCA Majority Gate

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3.QCA D-FLIP FLOP[10]

Flip Flop D (or delay) is a digital electrical circuit that allows the change of output signal status (Q) to be delayed until an upward clock timing signal arrives on the following edge.

INPUTS		OUTPUT
CLOCK	D	Q
0	0	Previous state
0	1	Previous state
1	0	0

Table1: Truth Table of D Flipflop

The QCA D-Flipflop uses majority gate concept in which the maximum number of three inputs given to a majority gate are observed as outputs. For suppose, if we are using the inputs as A,B,C and Q is the output, we get the output Q= M(A,B,C), that is if the inputs are A=0,B=0 and C=1 then the output is Q=0 and if the inputs are A=1, B=0, C=1 then the output is Q=1. This majority gate logic is used in designing all the gates in the QCA with which we design the circuits.

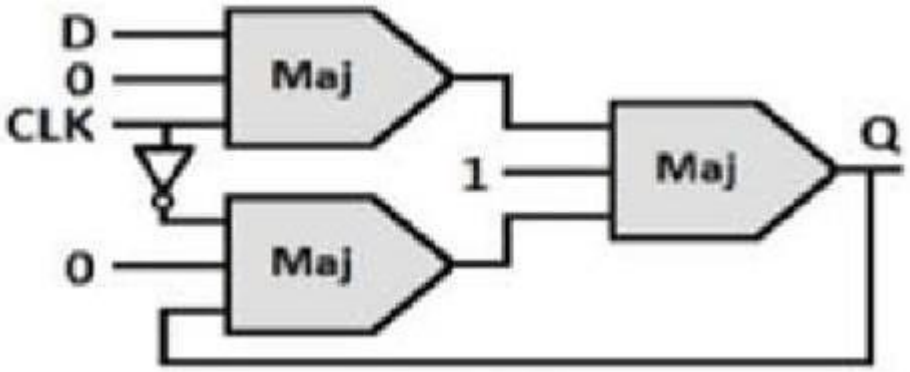

Fig4: QCA D-Flipflop design using Majority gates

3.1 Existing D-Flipflop model[10]

As D-Flipflops are used almost everywhere as buffers, delay circuits ,mostly in processors and RAMs, there are many proposed D-Flipflop models in existence. We have shown interest in designing a D flipflop and have come with a design as shown in Fig5c. Fig5a represents the existing models of D-Flipflops.

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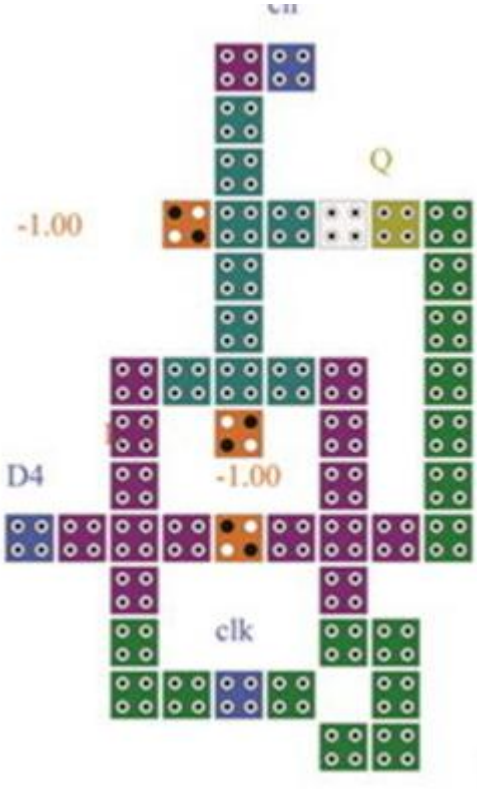

Fig5a: D-Flipflop in existence

Proposed D-Flipflop model for designing 3 bit shift register[11]

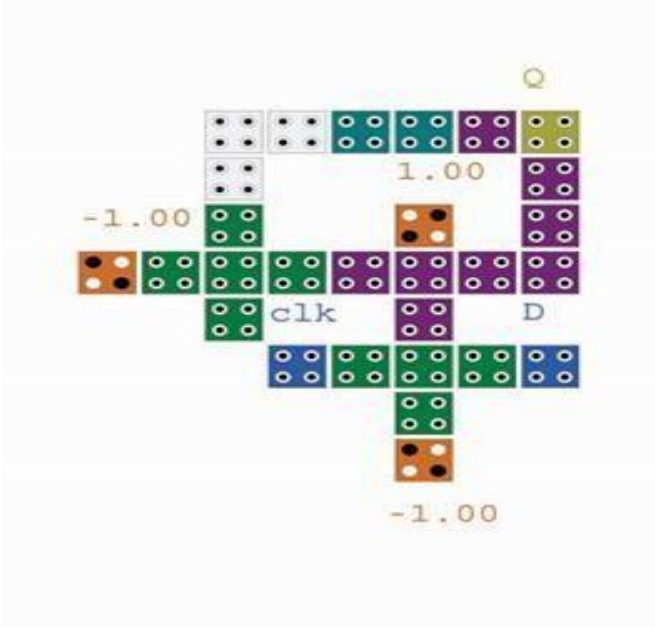

Fig5c: Proposed D-Flipflop model

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The above D flipflop has a total of 27 cells with four clocks (clock0, clock1, clock2, clock3) used to connect various majority gates to make the output. The clocks are used as required to provide the delay to the inputs and results.
The proposed D flip flop design is better than the existing designs. Furthermore, proposed D flipflop is more efficient in the matter of of area, cell counts and latency. It is foremost design in this section using conventional three input majority gate. QCADesigner 2.0.3. software is used for design realization & evaluation.
When there is a clock input, the input D varies with the clock and when the clock is absent or LOW then the previous value is retained that is , the D flipflop stores the value until the clock input is again made HIGH. This switching action makes the D-Flipflop brings to the use in buffers and RAMs and other memory cells.

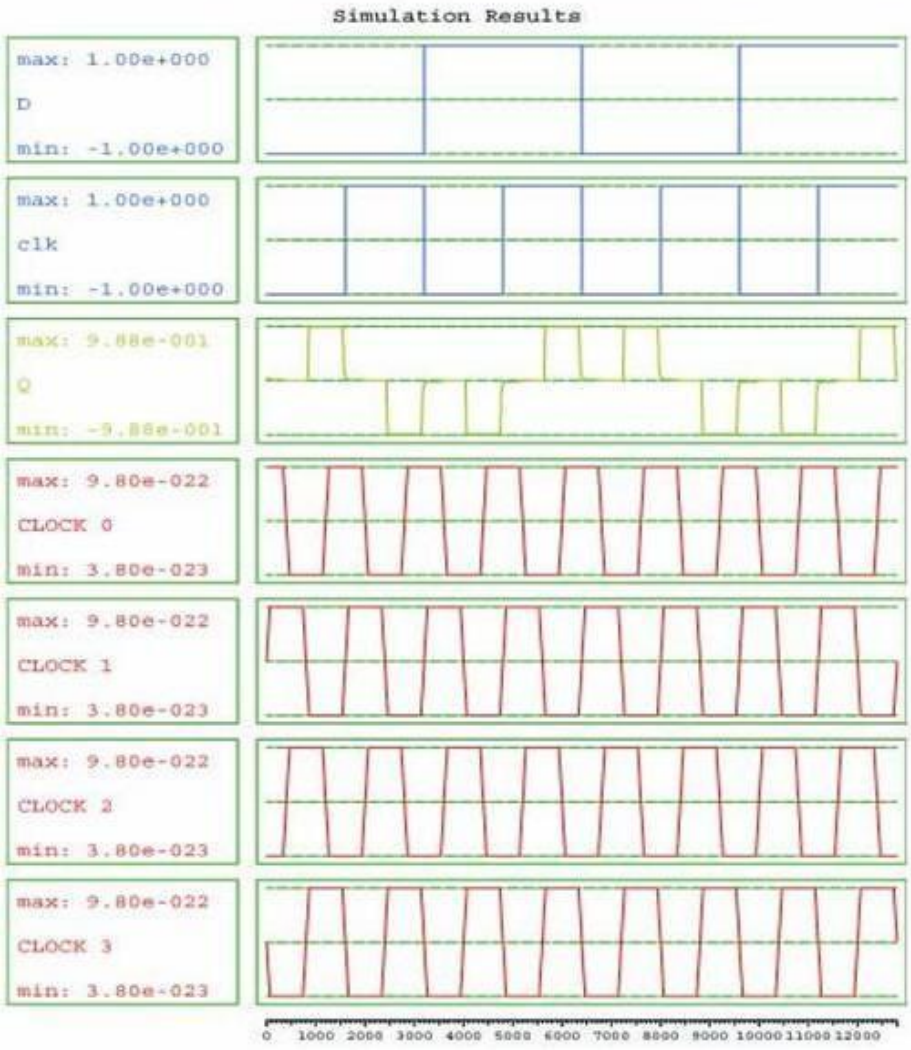

Fig5d: Simulation results for the proposed D-Flipflop

The D-Flipflop results areshown in simulation results. The output is logic high only when Clock input (clk) is high and input D is high. Though D is high when clk is 0, the output Q retains the previous state value and when clk Is high and D is low, the Q is logic low. We can observe the results by looking into Table1 above.

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3 SHIFT REGISTERS

A Shift Register is a kind of sequential logic circuit in digital circuits, especially for storing digital data in an electronic manner that has its inputs connected to the output in such a way that when the circuit is triggered, the data is shifted back down the line.

3.2 TYPES OF SHIFT REGISTERS

a. Serial In − Serial Out shift register (SISO).
b. Serial In − Parallel Out shift register (SIPO).
c. Parallel In − Serial Out shift register (PISO).
d. Parallel In − Parallel Out shift register (PIPO).

In this paper, we have designed a 3-bit Parallel Input- Parallel Output (PIPO) shift register using 3 D-Flipflop circuits as shown in Fig6a using QCA Designer software version 2.0.3. The model is a working model and the simulations are shown in the Fig6b.

Design

The 3-bit PIPO shift register presented is designed with 3 D-Flipflop circuits synchronized using a single clock with varying delays. The model consists of a total of 117 cells and has an area of 0.14um^2. The inputs CLK and D are of Clock0 and the output Q is Clock1. As we know the characteristic equation for a D-Flipflop is **Q_{n+1}=CLK*D + not (CLK) *Q_n.**

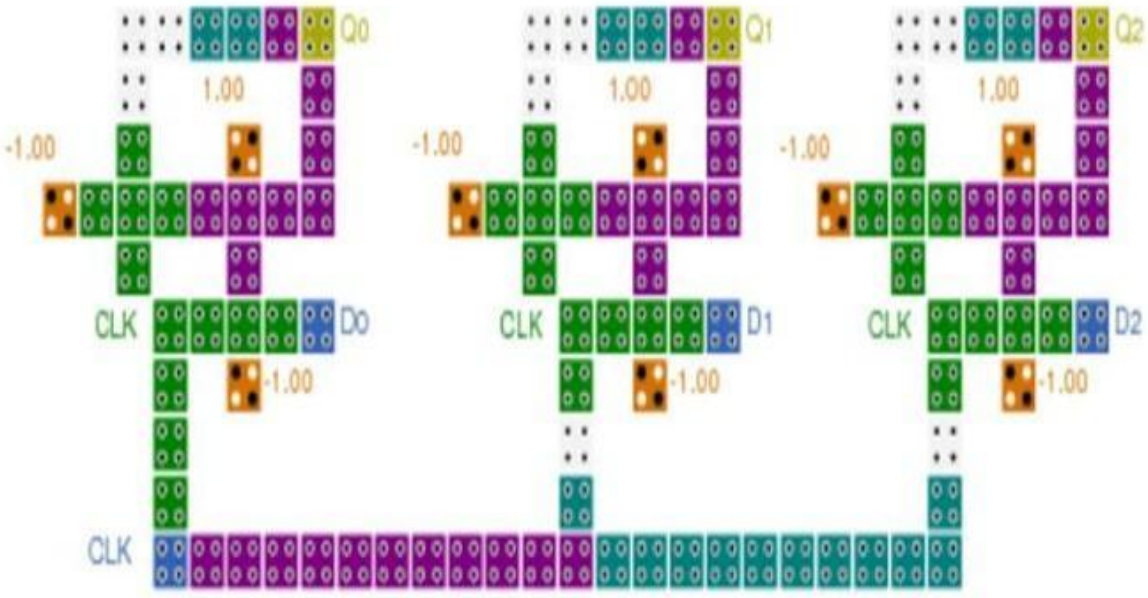

Fig6a: 3-bit PIPO shift register using D-Flipflop circuits

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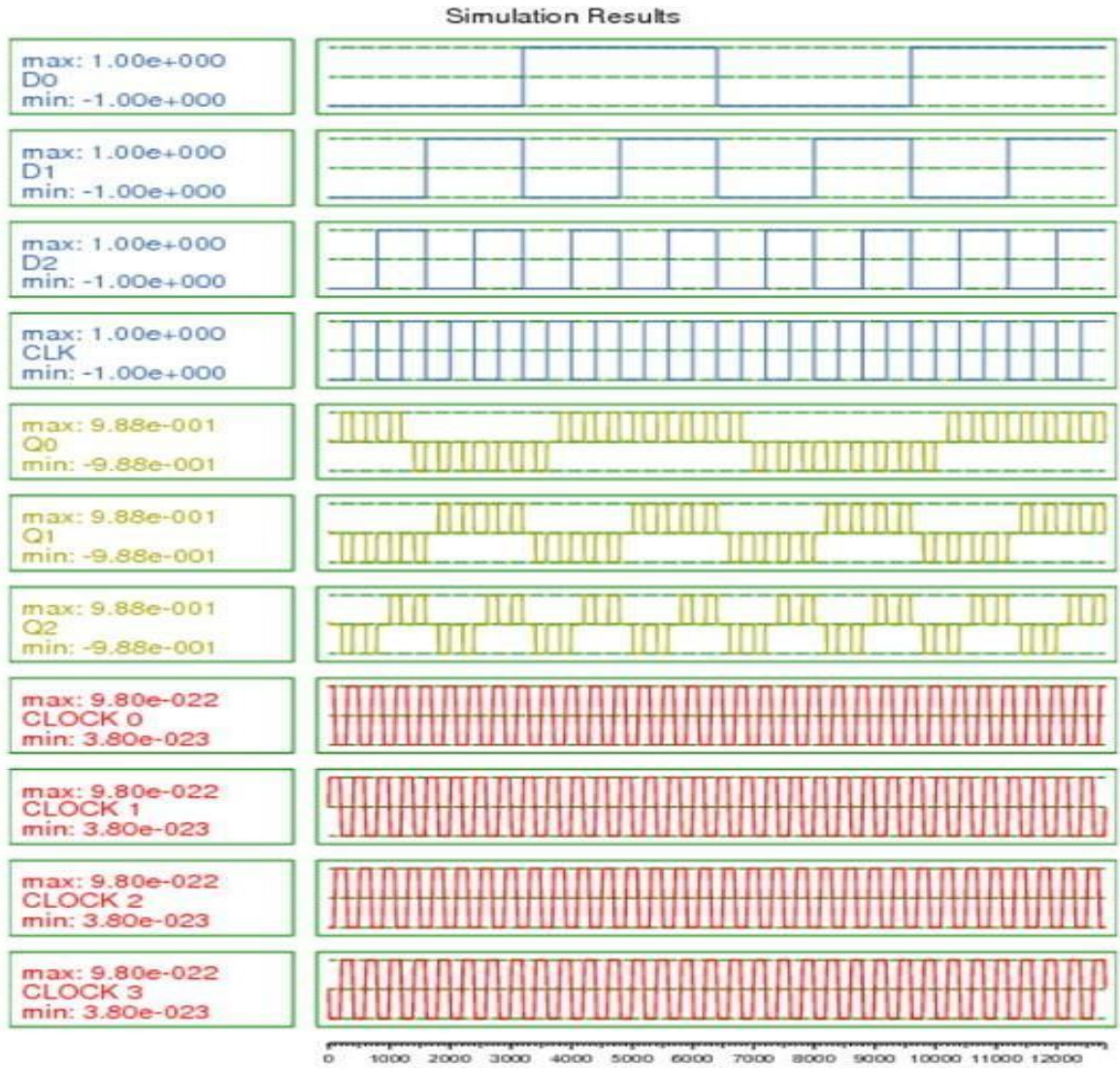

Fig6b: Simulation results for 3-bit PIPO Shift Register using DFF circuits

From the simulation results, we can observe that the outputs follow the D Flip Flop principles and ouputs are high or low in 2 situations:

1. when the CLK input is HIGH/LOW and D input is High/LOW, Q is HIGH/LOW
2. When the CLK input is LOW and no matter whether D is HIGH or LOW, the previous value of D is retained as output.

III.CONCLUSION

One of the most important QCA circuit in the digital circuits design is the PIPO shift register. So, this paper presented and evaluated novel and efficient circuit for the 3-bit QCA PIPO shift register. The proposed circuit for the 3-bit QCA PIPO shift register was implemented in 7 layers based on three QCA D-FF circuits. The proposed 3-bit QCA PIPO shift register consists of 117 cells and 0.14 μm2 area. We utilized QCA Designer tool Version 2.0.3 to implement the proposed circuits. The results showed that the proposed circuits provide improvements in comparison with other circuits in terms of area.

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