# Analysis of Low Power D Flip-Flop and Latches for Reduced Power

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**ABSTRACT:**Shift register is sequential logic path to store the digital data, also basic construction block in VLSI path. It is used in many uses, such as digital filters, communication receivers, and image processing ICs. As the size of the image data residues to rise due to the high request for high quality image data. Due to the latches it causes more power and delay, shift register is designed by using D-Flip flop that the existing connections are performed through the second layer and by the second type of metal and its area and power has been calculated and also the simulation results shows in table.

**KEYWORDS**:D-flip-flop, D latches.

## I. INTRODUCTION

In a digital circuit, a shift register is a cascade of flip flops sharing the clock, in which output of each flip flop are connected to data input of next flip-flop in a chain, Shift registers are normally used in various applications, such as digital filters, message receivers, and image processing ICs. Flip-flop" is the common name given to two-state devices which offer basic memory for sequential logic operations. Flip-flops are heavily used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data. Latches are asynchronous – which means, the output of the latch depends on its input; on the other hand, today, most computers are synchronous – which means, the outputs of all the sequential circuits change simultaneously to the rhythm of a global clock signal.

## II. LITERATURE SURVEY

The low-power and area-efficient shift register using pulsed latches is suggested, the area and power consumption are compact by exchanging flip-flops with pulsed latches. This technique solves the control problem between pulsed latches through the use of various non-overlap delayed pulsed clock indicators in its place of the predictable single pulsed clock signal.[1]This paper presents new techniques to assess the energy and delay of flip-flop and latch plans and shows that no single present design makes well across the wide range of operating rules present in complex systems we reduce total flip-flop and latch energy by over 60% without increasing cycle time[4]] VLSI technology hasbeen growing to the large extent. All credit for this goes to the increasing usage of integrated circuits for every embedded system, mobile technologies, increasing systems, etc. Increasing growth and use of knowledge has increased the thirst for low energy or power consumption [2].The condition has changed and now developing of different circuit methods for low power circuit design is an important research area. This situation has changed and now developing of different circuit techniques for low power circuit design is an important research area [5].

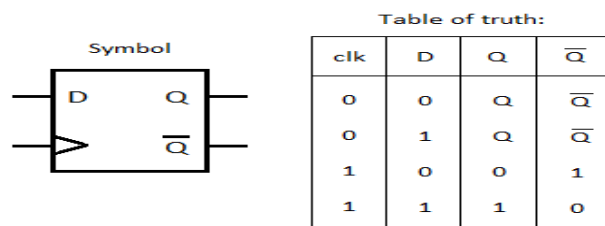III. TANNER SCHEMATIC

[1] **D flip-flop**

**D Flip-flop**



Fig1. D flip-flop

The D flip-flop tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. A D flip-flop can be made from a set/reset flip-flop by tying the set to the reset through an inverter, the result may be clocked [1].

The flip flop is a basic building block of sequential logic circuits. It is a circuit that has two stable states and can store one bit of state information. The output changes state by signals applied to one or more control inputs. [5].The basic D Flip Flop has a D (data) input and a clock input and outputs Q and Q (the inverse of Q). Optionally it may also include the PR (Preset) and CLR (Clear) control inputs.
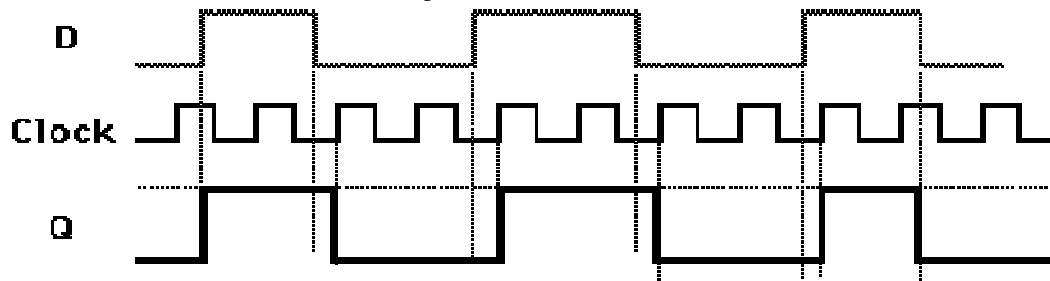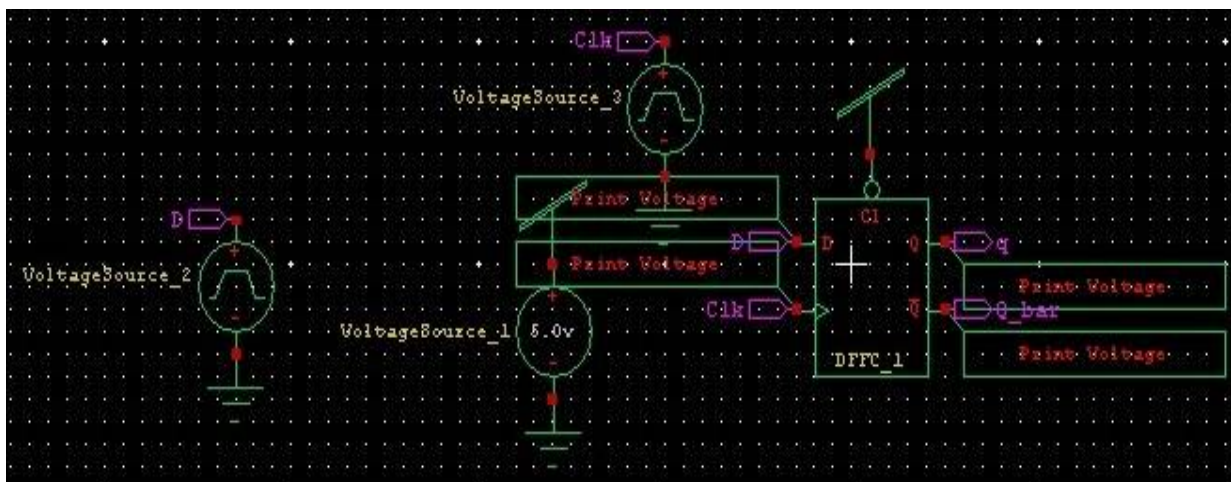


Fig 2. Waveforms of D flip-flop



Fig 3. Schematic design of D flip-flop

The schematic diagram of D flip-flop are shown at tanner tool software. The basic D flip-flop are implemented at the tanner tool which the voltage, current, power are should be calculated. The basic wave forms are to be calculated as follows.
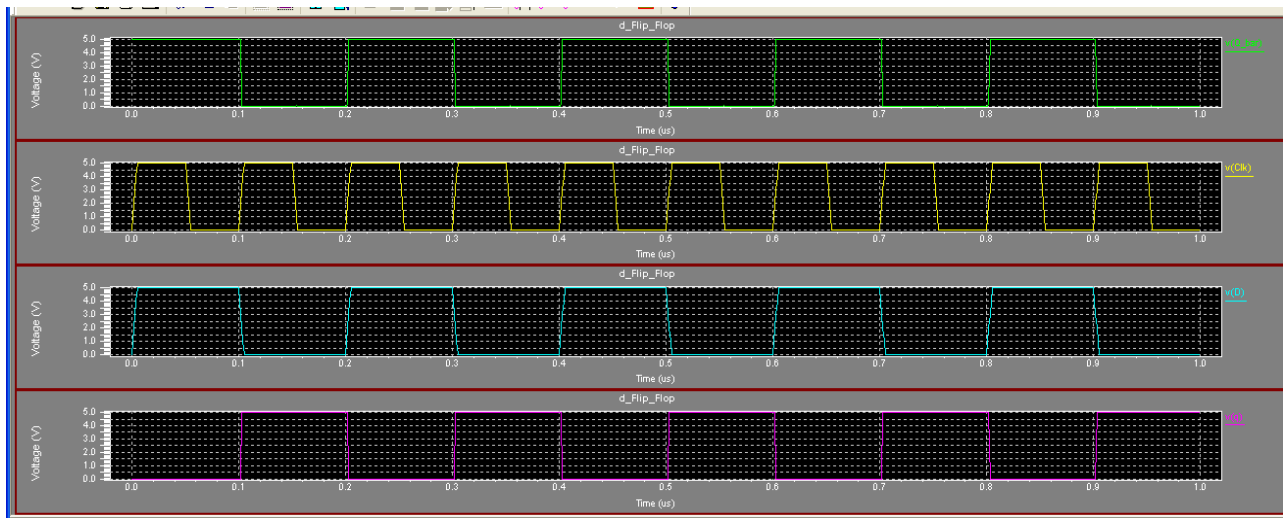


Fig 4. Output waveforms of D flip-flop

## IV. LATCHES

Latches are made by two investors hold in a bit as long as power is applied and storage is a new memory temporally break the feedback path.[1]Latches are asynchronous – which means, the output of the latch depends on its input; on the other hand, today, most computers are synchronous – which means, the outputs of all the sequential circuits change simultaneously to the rhythm of a global clock signal. Shift register designs are not achieved with the use of master-slave flip flops. Performance parameters such as area and power can be reduced with use of pulsed latches. Hence master-slave using two latches are can be replaced by pulsed latch consisting of latch with pulsed clock signal which is shown in fig.
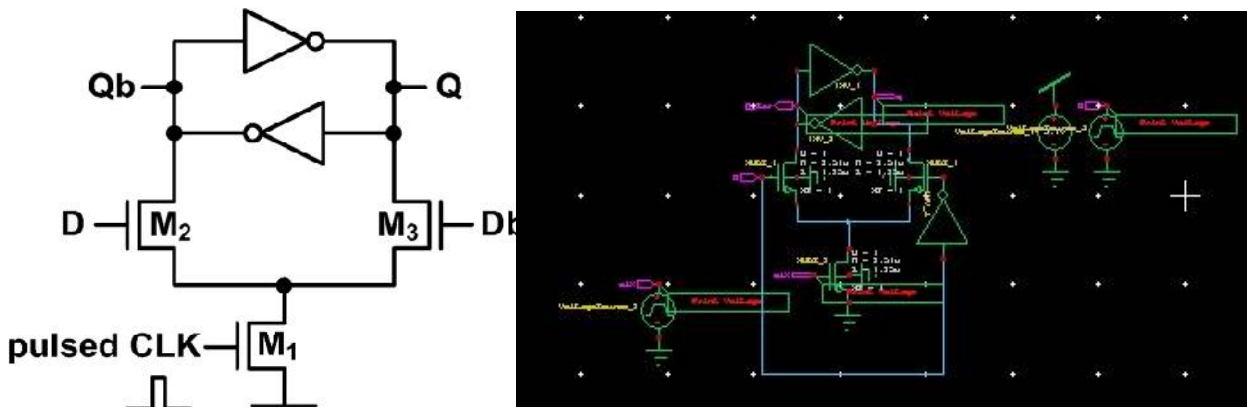


Fig 5. static differnetial sense amplifier shared pulse latch

The original SSASPL (static difference sense amplifier shared pulse latches)with 9 transistors is modified to the SSASPL with 7 transistors [4] by removing an inverter to generate the complementary data input (Db) from the data

input (D). In the proposed shift register, the differential datainputs (D and Db.) of the latch come from the differential data outputs (Q and Qb) of the previous latch. The SSASPL uses the smallest number of transistors and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal [4]. The SSASPL updates the data with three NMOS transistors and it holds the data with four transistors intwo cross-coupled inverters

The figure shows that the schematic of D latches which consist of the basic invertors that are which are follow by the one by one and the transistors that used in that schematic .the voltage source and current source are applied to the invertors for the calculation of power, voltage and current.
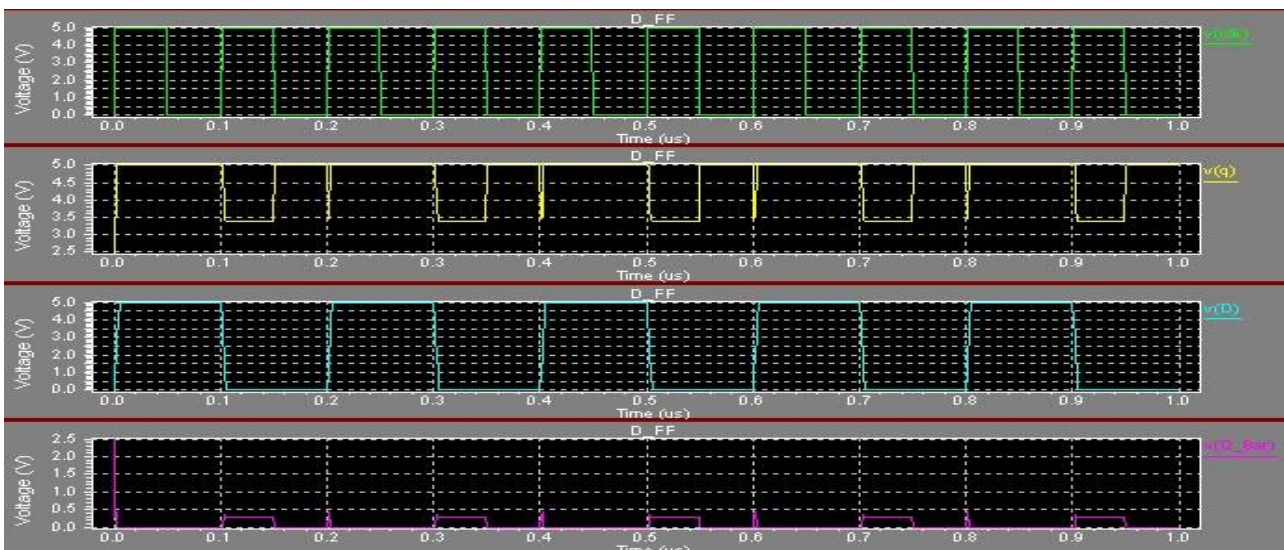


Fig 6. output waveforms of SSASPL

The waveforms of SSASPL i.e. static difference sense amplifier shared pulse latches which is shows the output waveforms that the firstly the signal clock period given to the circuit. The D and Db that input given to the circuit that the 0 is given to the circuit that if clock pulse is 1 then output of waveforms that changes to shows v(q) because of invertors is used in the circuit for the output changes waveforms show in second waveforms.as the wave deflected it can't complete whole circuit because of this invertors. As the input given to other side the second invertor works that the wave tilted at half of the circuit which shown in waveforms v(q).the v(q) bar waveforms that exactly opposite of the above v(q)waveforms.

## V.  RESULTS

|  | D flip-flop | D- latches |
|---|---|---|
| Voltage | 5 v | 5 v |
| Current | 0.672m amp | 3.025m amp |
| Power | 3.369m watt | 15.12m watt |
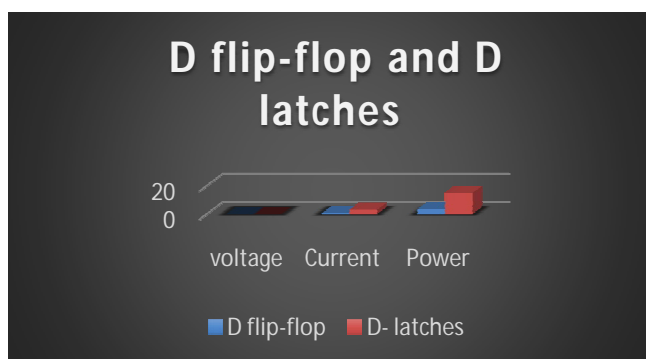
The analysis of D flip-flop and latches for low power which will be calculated as above chart show, in this the current and power which required as much low in flip-flop rather than latches. The same voltage source which will be applied to both the flip-flop and latches. The power consumption was very low i.e. flip-flop is better than latches. Now here in chart same voltage current and power are factor shown accordingly to that the same flip-flop is better result than latches which will be shown in graphically.

## VI. CONCLUSION

The shift register reduces area and power consumption replacing flip-flops with pulsed latches. The implementation of D flip-flop and D latches are work will reduced power and current of the shift register problem, by using it will reduced power and current consumption.

## REFERENCES

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