ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 6, June 2017

Survey and Comparisons of Low Power Multiplier Design in Term of Area, Power, Delay

Poonam P.Kokate , Prof V.G.Raut

Department of Electronic & Telecommunication, Sinhgad College of Engineering, Pune, Savitribai Phule University Pune, India

ABSTRACT: framework for designing a reliable low power multiplier by using algorithmic noise tolerant architecture with the fixed width multiplier to build the reduced precision replica redundancy block (RPR).As compared with fixed width RPR design ,the proposed fixed width RPR not only perform with higher SNR but also with lower area and lower power consumption. It diminishes i.e. reduces the truncation mistake and after that develops a lower blunder settled width baugh-wooley array multiplier. It is proficient for VLSI implementation. The ANT method having high precise, low power utilization and region productivity. The Fixed width designs are usually applied in DSP application to avoid infinite growth of bit width.They compare low power multiplier in terms of delay, power, area.

KEYWORDS: Algorithmic noise tolerant (ANT), fixed-width multiplier, reduced-precision replica (RPR).voltage overscalling(VOS).reduced number system (RNS).significance driven computation (SDC)

I. INTRODUCTION

Portable and wireless computing systems are widely growing nowadays. This establishes a need for low power systems. To lower the power dissipation, supply voltage can be thought to scale down, since the power consumption in CMOS circuits is directly connected to the square of supply voltage. However, in deep- submicrometer process technologies, noise interference problems occur. This have increased difficulty to design the reliable and efficient microelectronics systems, hence such design techniques to enhance noise tolerance have been widely developed.[5]A low-power technique, referred to as voltage over scaling (VOS), was proposed to lower supply voltage below critical supply voltage so that throughput is not sacrificed. However, VOS leads to severe degradation in signal-to-noise ratio (SNR). Another technique involves algorithmic noise tolerant (ANT) technique along with VOS main block with reduced-precision replica (RPR), which combats soft errors and helps achieve significant energy saving. However, the RPR designs in the ANT designs are designed in a special manner, which are not easily adopted and repeated . Multiplication is the most critical operation in every computational system. Multiplication is the most important operation in every computational system .Graphics and Process control are two areas where in the multiplier performance plays a crucial role. In this research work ,they assist proposed a simple way utilizing the settled width RPR to supplant the full-width RPR square. Utilizing the settled width RPR, the calculation error can be remedied with lower power utilization and lower zone overhead .In this paper, they proposed a lower power DSP scheme via stochastic logic protection. The main module is implemented with TCS circuit. The stochastic logic is used as EC module.[2] In this paper, they apply the VOS technology to RNS based DSP system design and implementation to achieve higher power efficiency than traditional RNS-based methods.[1]Wallace Tree CSA structures are used to sum the partial products in reduced time. Speed can be increased by incorporating compressors with wallace tree technique . Therefore, minimizing the number of half adders used in a multiplier which will reduce the circuit complexity.[6]. In this paper,they propose logic complexity reduction at the transistor level as an alternative approach to take advantage of the relaxation of numerical accuracy.they design architectures for video and image compression algorithms using the proposed approximate arithmetic units and evaluate them to demonstrate the efficacy of our approach**.[7]**

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 6, June 2017

II. ANT ARCHITECTURE DESIGN

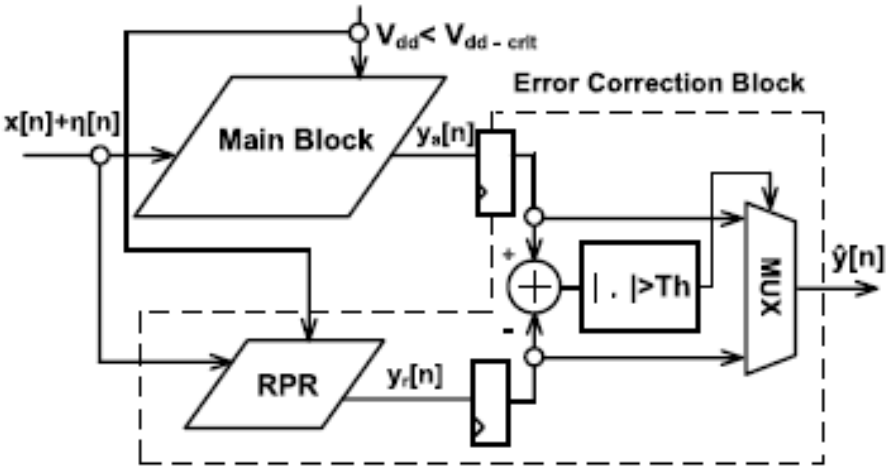

Fig1: ANT block diagram

The ANT technique includes both main digital signal processor (MDSP) and error correction (EC) block, as critical path delay Tcp of the system becomes greater than the sampling period Tsamp, the soft errors will occur. Under VOS, many input-dependent soft errors in its output ya[n]; however, RPR output yr [n] is still correct since the critical path delay of the replica is smaller than Tsamp. Therefore, yr [n] is used to detect errors in the MDSP output ya[n]. Error detection is calculted by comparing the difference |ya[n] − yr [n]| against a threshold Th. Once the difference between ya[n] and yr [n] is larger than Th, the output ˆy[n] is yr [n] instead of ya[n].

As a result, ˆy[n] can be expressed as:

y[n] = ya [n] , if |ya [n] − yr [n]| ≤ Th
yr [n], if |ya [n] − yr [n]| >Th…….. (1)

Threshold (Th) is determined by

Th = max |yo [n] − yr [n] ……. (2)

Where,yo[n] is error free output signal. In this way, the power consumption can be greatly lowered while the SNR can still be maintained without severe degradation.

In this research work, they assist proposed a simple way utilizing the settled width RPR to supplant the full-width RPR square.[5] Utilizing the settled width RPR, the calculation error can be remedied with lower power utilization and lower zone overhead. This asset waste could halfway be helped by having a few multipliers, each with a particular piece width, and utilize the specific multiplier with the littlest piece width that is sufficiently huge to oblige the present augmentation. Such a plan would guarantee, to the point that an augmentation would be figured on a multiplier that has been advanced as far as power and defer for that particular bit width [2].Mobile Ad Hoc Networks (MANETs) consists of a collection of mobile nodes which are not bounded in any infrastructure. Nodes in MANET can communicate with each other and can move anywhere without restriction. This non-restricted mobility and easy deployment characteristics of MANETs make them very popular and highly suitable for emergencies, natural disaster and military operations.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 6, June 2017

Major two steps as follows:

A. LAYOUT DESIGNING

In this work we have designed a new 1-bit 10-transistor full adder which consumes less power than the standard implementations of full adder cell. The proposed adder is tested and compared with the high transistor count and existing 10-transistor adders under the same conditions. The addition of 2 bits A and B with C outputs a SUM and a CARRY bit. The integer equivalent of this relation is shown as

SUM = (A B).C + (A B).C --- (1)
CARRY = (A B).C + (A B).A--- (2)

The proposed adder implements equations (1) and (2) using complementary CMOS and MUX based design logic with only 10 transistors. The adder is useful in larger circuits such as multipliers despite the threshold problem. The number of direct connections from VDD to the ground is reduced in the new design to minimize the power consumption due to short circuit current. Also the generation of SUM from CARRY is avoided as in the CMOS adder.
The adder uses internally generated signal (A XOR B) and (A XNOR B) to control the output transistor gates. The same (W/L=5□ / 2□) ratio is used for all the designs and our design is compared on the same platform in 70nm technology in MICROWIND [10].

The SUM and CARRY signals are generated separately after the generation of (A XOR B) so as to reduce the delay. In the design, the second CMOS inverter in the critical path of the generation of the SUM helps in reducing the threshold loss. Performance analysis of all the adder designs is carried out in 90nm, 70nm and 50nm CMOS technology in MICROWIND. The performance is studied at power supply voltage of 1.0V for 90nm and 0.7V for 70nm at frequencies of 50MHZ .

B. ALGORITHMIC NOISE-TOLERANCE

An ANT-based DSP framework has a principle DSP (MDSP) hinder that processes in vitality effective way however makes irregular errors [11]. It acknowledges as its info the sign z[n] + sn[n], where z[n] is the information sign and sn[n] is the info signal clamor. The uproarious output of the MDSP square is meant by y'[n]. Generally, the MDSP square gives up clamor invulnerability for vitality productivity. The EC square watches the boisterous outputy'[n], and the information z[n] + sn[n] and maybe certain inward MDSP signs to recognize and remedy errors. The last revised output of the ANT-based framework is signified as ŷ[n]. The error control (EC) piece works in an error freeway yet expends fundamentally more vitality per operation than the MDSP block [12].

$$y\,'[n] = \sum_{K=0}^{N-1} hk^{x}\,[n-k] + \eta[n] = y[n] + \eta[n]$$

where y[n] is the error free output and □[n] describes to the appearance of DSM clamor at the algorithmic level on a for every (output) test premise. We now portray a case to delineate the ANT concept.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 6, June 2017

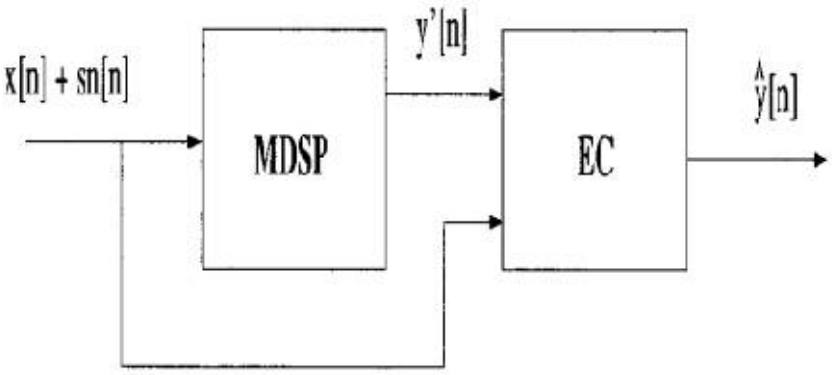

Fig. 2: ANT based DSP system

In this paper,they proposed a lower power DSP scheme via stochastic logic protection. The main module is implemented with TCS circuit. The stochastic logic is used as EC module. The advantage of proposed scheme is that the TCS circuit will guarantee the computation precise and the stochasticlogic based EC module is error tolerant, which can reduce the soft errors in the main module. According to the case study of FIR filter, When the power saving achieves 65%, the proposed method outperforms 6dB than traditional methods. In this case, the proposed method only has 2dB SNRperformance loss. The stochastic based EC moduleoutperforms 20dB than other methods when the correct probability of each logic gate pk=0.999, and the advantage of proposed method is larger as pkdecrease.

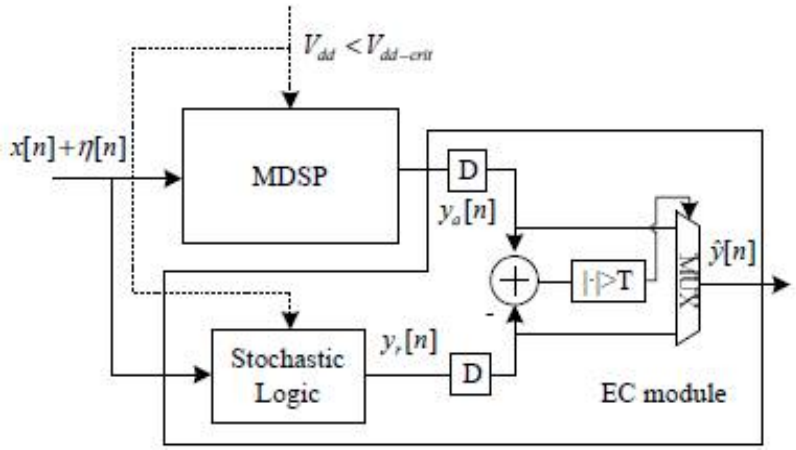

Fig. 3 The Scheme of Stochastic Logic Based System

The stochastic logic is used in EC, which has simplerstructure and shorter critical path than TCS. Thus, stochastic logic based EC is more robust than TCS in low voltage regime. Meanwhile, stochastic is no-weighted number system. That is, stochastic logic based system is more error tolerant than TCS in noise environment caused by deep submicron processing technology, voltage and temperature. In this paper, they focus on the soft error caused by voltage reduction. The proposed method can be used to mitigate the error introduced by the other reasons.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 6, June 2017

In this paper, they apply the VOS technology to RNS based DSP system design and implementation to achieve higher power efficiency than traditional RNS-based methods. Due to the nonlinear relationship among the independent processing channels of RNS, the soft errors caused by VOScan lead to significant performance degradation of RNS. In order to mitigate the influence of the soft errors in RNS, we propose a new method called joint RNS-RPR (JRR). The JRR method combines the information from RPR and RNS to achieve higher soft-error-correction performance than RPR.[1]

Compared with the redundancy-RNS (RRNS)-based method, JRR requires less hardware cost and power consumption, since the redundant information in JRR comes from the RPR module instead of the residue channels. Since JRR inherits all properties of RNS, the power consumption of JRR is lower than the methods in, and In this paper, a 28-tap finite-impulse response (FIR) filter with 0.25-μm 2.5-V CMOS technology is used for case study, from which we find JRR has higher energy efficiency and lower hardware complexity than that of and Simulation results also show that JRR can achieve higher energy efficiency than RRNS under the same signal-to-noise ratio (SNR) performance. The same conclusions can be drawn for other DSP system designs. Thus, we provide a new way to design and implement the error-tolerable DSP systems with high energy efficiency.

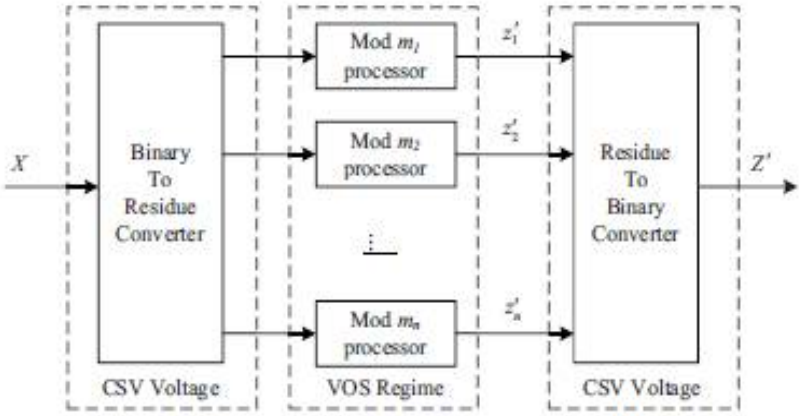

Fig4 :RNS scheme in VOS

They consider application-specific integrated circuit implementations of error-resilient applications like image and video compression. We target the most computationally intensive blocks in these applications and build them using approximate hardware to show substantial improvements in power consumption with little loss in output quality. Few works that focus on low-power design through approximate computing at the algorithm and architecture levels include algorithmic noise tolerance (ANT) significance driven computation (SDC) andnonuniform voltage overscaling (VOS). All these techniques are based on the central concept of VOS, coupled with additional circuitry for correcting or limiting the resulting errors. In, a fast but "inaccurate" adder is proposed. It is based on the idea that on average, the length of the longest sequence of propagate signals is approximately log n, where n is the bitwidth of the two integers to be added. An error-tolerant adder is proposed in that operates by splitting the input operands into accurate and inaccurate parts. However, neither of these techniques target logic complexity reduction. A power-efficient multiplier architecture is proposed in that uses a 2 × 2 inaccurate multiplier block resulting from Karnaugh map simplification. This paper considers logic complexity reduction using Karnaugh maps.[7]

They establishes designing multipliers that are of high-speed, low power, and regular in layout are of substantial research interest. Multiplier speed can be increased by reducing the generated partial products. Many attempts are done to reduce the number of partial products generated in a multiplication process. One of them is Wallace tree multiplier. Wallace Tree CSA structures are used to sum the partial products in reduced time. Speed can be increased by incorporating compressors with wallace tree technique . Therefore, minimizing the number of half adders used in a multiplier which will reduce the circuit complexity. Basically multiplier consists of three parts 1. Partial product generation 2.partial product addition and 3.final adding part. A multiplier essentially consist of two operands, a multiplicand "Y" and a multiplier "X" and produces a product . Initially x & y are multiplied bit by bit to generate the partial products product .Second stage is the most important,because it consists most complicated and determines the speed of the overall multiplier to add these partial product to generate the Product "P". Modification will be focused on the optimization of this stage, it contains the addition of all the partial products. In case speed is not of main concern then partial products can be added serially,it reduces the circuit complexity. However, in high- speed design,in the Wallace tree construction method addition of partial

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 6, June 2017

products occur in a tree like fashion that produces two rows of partial products which can be added in the final stage. Although fast, since its critical path delay is directly in proportion with the logarithm of the number of bits in the multiplier, the Wallace tree introduces other problems suchas layout area wastage and increased complexity. So compressor trees are used to perform high speed addition with less area complexity. In the last stage, addition can be performed by using high-speed adder for example carry save adder to generate the output result.[6]

Under the case of six-bit fixed-width RPR multiplier design, the chip area occupied by total logic cells can be saved by 44.55% as compared with the six-bit full-width RPR design. Comparison is as shown in the table.

Table I Performance for power calculation

SYSTEM	POWER
Using Adder system	69.32%
Reduces no system	67.5%
stochastic logic	65%

Table II Comparison of 6 bit fixed width multiplier and full width multiplier

Functions	Existing method	Proposed method
Time delay	41.488ns	10.032 ns
Area	5145	750
Power	97mW	23mW

Table III :delay comparison

	Fixed width RPR	RPR with compressor tree
Minimum period	41.488 ns	10.032 ns
Minimum input arrival time before clock	4.736 ns	4.376 ns
Maximum output time after clock	6.140 ns	7.157 ns
Maximum combinational path delay	No path found	No path found

Table IV: Area Comparison

	Fixed-Width RPR	RPR with compressor tree
Number of slice flip flops	132 out of 13.824	294 out of 13.824
IOB flip flops	36	12
Total equivalent gate count for design	4671	4032
Peak memory usage	138 MB	152MB

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 6, June 2017

III. CONCLUSION

Since the stochastic computation based system has simple logic structure, the supply power can be reduced more than traditional TCS based EC methods. When consider the soft error for each logic, the SFIR is more error tolerant than traditional methods. Hence, when the EC module is implemented by stochastic computation based scheme, the system can be more energy efficiency and more error tolerant.In this They, a low-error and area-efficient fixed-width RPR-based ANT multiplier design is presented. The proposed 12-bit ANT multiplier circuit is implemented in TSMC 90-nm process and its silicon area is 4616.5 μm2. Under 0.6 V supply voltage and 200-MHz operating frequency, the power consumption is 0.393 mW. In the presented 12-bit by 12-bit ANT multiplier, the circuitry area in our fixed-width RPR can be saved by 45%, the lowest reliable operating supply voltage in our ANT design can be lowered to 0.623 VDD, and power consumption in our ANT design can be saved by 23% as compared with the state-of-art ANT design.

REFERRENCES

[1] J. N. Chen and J. H. Hu, "Energy-efficient digital signal processing via voltage-overscaling-based residue number system," IEEE Trans.Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 7, pp. 1322–1332, Jul. 2013.
[2] J. N. Chen, J. H. Hu, and S. Y. Li, "Low power digital signal processing scheme via stochastic logic protection," in Proc. IEEE Int. Symp. CircuitsSyst., May 2012, pp. 3077–3080
[3]N. Petra, D. D. Caro, V. Garofalo, N. Napoli, and A. G. M. Strollo, "Truncated binary multipliers with variable correction and minimum mean square error," IEEE Trans. Circuits Syst., vol. 57, no. 6, pp. 1312–1325, Jun. 2010.
[4] Gopalakrishnan "low power truncated binary multiplier using replica redundancy block" , volume 4 issue 3, march 2015
[5]PriyankaBhardwaj, JyotiAhlawat" Design and analysis of Low-Power Multiplier using Fixed-width Replica Redundancy Block" ,Vol. 4, Issue 10, October 2016
[6] Mariya Stephen1, Vrinda2 " Design for Low Power Multiplier Based On Fixed Width Replica Redundancy Block & Compressor Trees"Volume 4 Issue 10, October 2015
[7]Vaibhav Gupta, DebabrataMohapatra, AnandRaghunathan, Fellow, IEEE, and Kaushik Roy, Fellow, IEEE "Low-Power Digital Signal Processing Using Approximate Adders", VOL. 32, NO. 1, JANUARY 2013