Low-Power and Area-Efficient Shift Register Using Pulsed Latches

Jacob B Cacko, Gajendra Sujediya

Assistant Professor, RIET Jaipur, Rajasthna, India

Research Scholar, RIET Jaipur , Rajasthna, India

ABSTRACT: This paper proposes a low-power and area-efficient shift register using pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 256-bit shift register using pulsed latches was fabricated using a 0.18 $\mu{\rm m}$ CMOS process with ${\rm V}_{\rm DD}=1.8{\rm V}$. The core area is $6600 \mu{\rm m}^{2}$. The power consumption is 1.2 mW at a 100 MHz clock frequency. The proposed shift register saves 37% area and 44% power compared to the conventional shift register with flip-flops.

I. INTRODUCTION

The clock network is one of the large consumers of dynamic power. Therefore, reducing power in the clock network can impact the overall dynamic power significantly. Designers already use a variety of techniques to reduce the clock power using smaller clock buffers, reducing the overall wiring capacitance, employing clock gating to reduce the dynamic power, and de- cloning to move the clock buffers at higher levels of hierarchy . Even with these techniques, the dynamic power of clock network can be large since registers are used as state elements in the design. In general, a flip - flop is used as the register or you can say sequential circuits. For mobile devices, where power consumption is the prime concern with high speed of operation, there is requirement of low power flip- flops in designs. Many other applications where shift registers are commonly utilized such as digital filters ,communication receivers and image processing IC's. In particular, edge- triggered sequential circuits

PULSED LATCH TECHNIQUE
Flip - flop is the most common form of sequencing elements. Flip - flop synchronization with the clock edge is widely used because it is matched with static timing analysis, however, high sequencing leads to overhead in terms of delay, power and area. A latch is quite simple and at the same time consumes much less power than that of the flip- flop. However, it is little difficult to apply static timing analysis with latch design because of the data transparent behavior. A latch is capable of capturing data during the time duration determined by the width of clock waveform. This time duration is known to be very sensitive to its operation.
It is possible to trigger a latch using pulse clock waveform. A latch synchronized by a pulse clock is known as pulsed latch and its behavior is similar to an edge triggered flip - flop because the rising and falling edges of the pulse clock are almost identical in terms of timing. In a pulsed latch technique, the setup times of pulsed latch are expressed with respect to the rising edge of the pulse clock and hold times are expressed with respect to the falling edge of the pulse clock. Thus timing models of pulsed latch is very similar to that of the edge - triggered flip - flop.

The first component is the energy dissipated when the flip-flop is clocked while the data of the flip-flop is unchanged. The second component is the additional energy required to write a different data value into the flip-flop. In a typical flip-flop, the two energy components are comparable. However, in most systems, the data rate of a flip-flop is typically much lower than its clock rate. This means that identical data value is being loaded with very high probability. Thus, the power saving techniques for flip-flops mostly concentrates on the clock energy reduction.

Many different circuit techniques for latches and flip-flops have been explored for various needs.

The low power requirement merely adds another factor to the trade-off during the design process.

Referring to the power equation

$$P = CV^2f$$

Where C= capacitance

V=Voltage

f=Frequency

The techniques for low power flip-flops are obvious. We will not discuss voltage reduction techniques because they are fairly straightforward when applied to flip-flop circuits. Some techniques attempt to reduce the gate capacitance connected to the clock signal. Others attempt to reduce or increase the transistor count to reduce power by minimizing unnecessary internal node switching. Various implementations of CMOS latches were introduced. Each circuit provides a different trade-off among setup time, hold time, data-to-output and clock-to-output delay. The use of NMOS pass transistors instead of transmission gates reduces the loading capacitance of the clock pin at the cost of reduced speed. This eliminates the need for a two-phase non-overlapping clock on the system or a phase splitter inverter that consumes power inside the cell. When logic 1 is propagated through the NMOS pass transistor, threshold voltage loss occurs in circuit.

Reduced Swing Clock

Referring to the golden power equation, the most attractive parameter to attack is the voltage swing *V* due to the quadratic effect. Generally, it is difficult to reduce the load capacitance or frequency of clock signals due to the obvious performance reasons. We will discuss some power reduction techniques for clock signals based on voltage swing reduction.

One such idea proposes to reduce the clock swing by half. Notice that in CMOS design, a clock signal is only connected to the gate of a transistor when it reaches a sequential element. The clock signal is seldom connected to the source or drain of a transistor. Inside a sequential cell, the clock signal is used to turn on or turn off transistors.

Consider a 5V digital CMOS chip with an N-transistor threshold voltage of O.8V. For a 5V regular full swing clock signal, an N-transistor gated by the clock will turn on if the clock signal is above O.8Y. Therefore if we limit the swing of the N-transistor clock signal from zero to 2.5V (half swing), the on-off characteristics of all N transistors remain digitally identical. Similar

Exchange of flip-flop with proposed pulsed latch

Pulsed latch retain the advantage of both flip-flop (simple timing model) and latch (fast and small). Replacement of flip-flop with pulsed latch can save appreciable amount of power consumption. In pulsed latch, the setup time is expressed in terms of rising edge of pulse clock, while hold time is expressed in terms of falling edge of pulse clock. This means timing model of pulsed latch is similar to that of flip-flop. Regardless of master slave configuration of latch in flip-flop, pulsed latch eliminates one latch from each cycle and clock's complement. The other difference between the flip-flop and pulsed latches would be explained in following sections. In figure 3.6, D latch using NAND gate is shown. Pulsed latch using this D latch and basic pulse generator has been implemented to get similar functionality as D flip-flop.

II. PULSED LATCH ISSUES AND OPTIMIZATION

If pulse generators and pulsed latches are not placed properly, timing violations might occur. A pulse generator generates a brief clock signal to each connected latch, after receiving the clock waveform from the clock source. Latches can share the same generator with the same pulse width. A pulse generator is a combinational circuit itself. The output load capacitance would also affect the delay and driving capability of a pulse generator [8]. If a pulse generator and latches are not placed properly, the wire length might become too long and thus make the generated pulse width distorted causing serious timing violations. In Figure 4.1, load capacitance and the pulse width are inversely proportional to each other. Therefore, after circuit placement, the pulse-width degradation might cause timing constraint violations, e.g., setup/hold time violations. A multilevel pulsed latch prevents pulse width degradation.
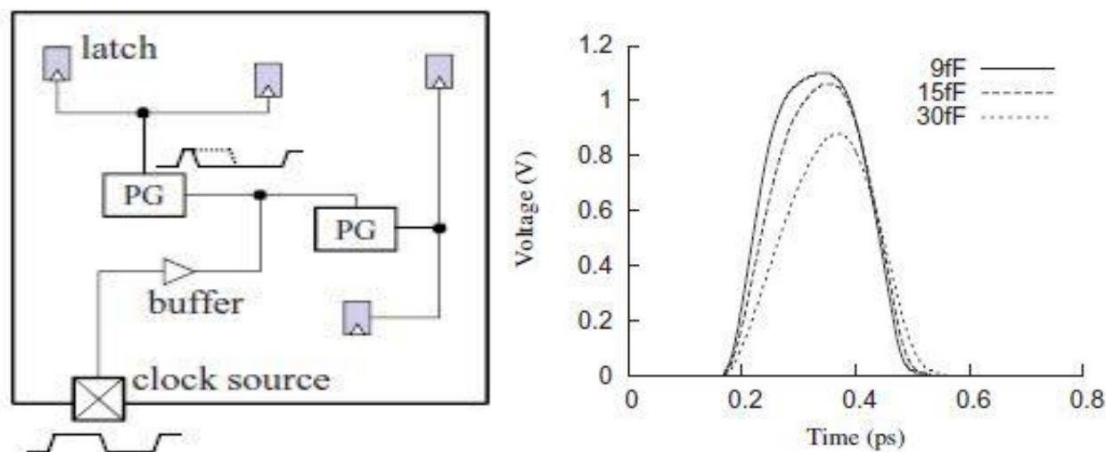

Fig. 1 Multilevel PL & Pulse width distorts as CL increases

III. PROPOSED APPLICATIONS OF PULSED LATCH

There are wide range of applications for pulsed latches. Pulsed latches could be used in portable devices where low power consumptions is necessary like the applications where flip-flops could be replaced with pulse latches i.e. in pipelining or as sequencing element or as register.

Johnson Counter using pulsed latch

An interesting variation of the Ring counter is obtained if, instead of the output, we take the invert of the output of the last stage and feed it back to the first stage. This circuit is known as Johnson Counter. Since four latch or four states of counter being utilized hence also known as mod-4-counter. An *n*-bit counter of this type generates a counting sequence of length 2*n*. For example, a four-bit counter produces the sequence 0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000, and so on. Note that in this sequence, only a single bit has a different value for two consecutive codes.
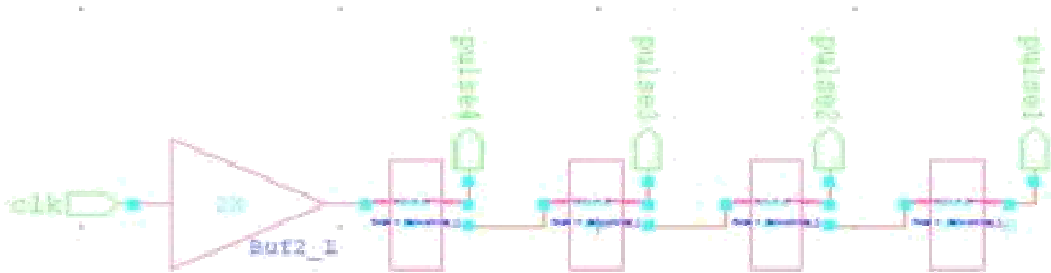
Fig. 2 Johnson counter using pulsed latch

IV. SIMULATION RESULTS

Simulations of all the circuits were performed in Tanner tools v14.1 using 180 nm technologies. Figure 6.1 to figure 6.12 shows the schematic and waveform of proposed circuits implemented in the tool. The waveform depicts the working of application using pulsed latch. Results of simulation are listed from table 6.2 to table 6.7. Table 6.1 provides the performance comparison between the D flip-flop and pulsed latch. Table 6.2 to 6.7 provides the comparative study of different applications using pulsed latch and different application using conventional D flip-flop i.e. SISO, SIPO, PISO, PIPO, Ring counter, Johnson counter respectively.
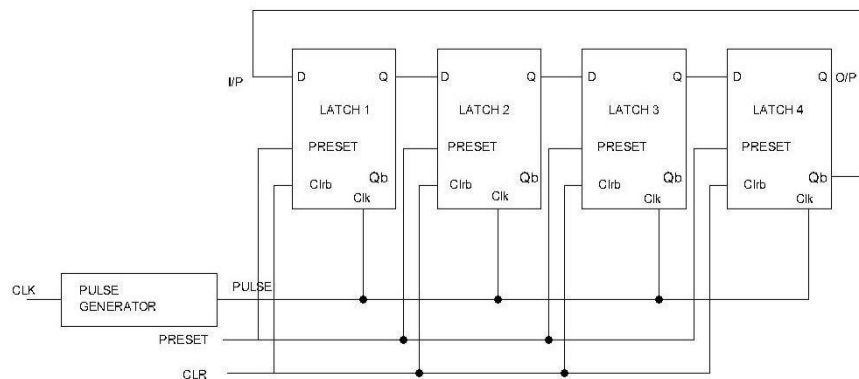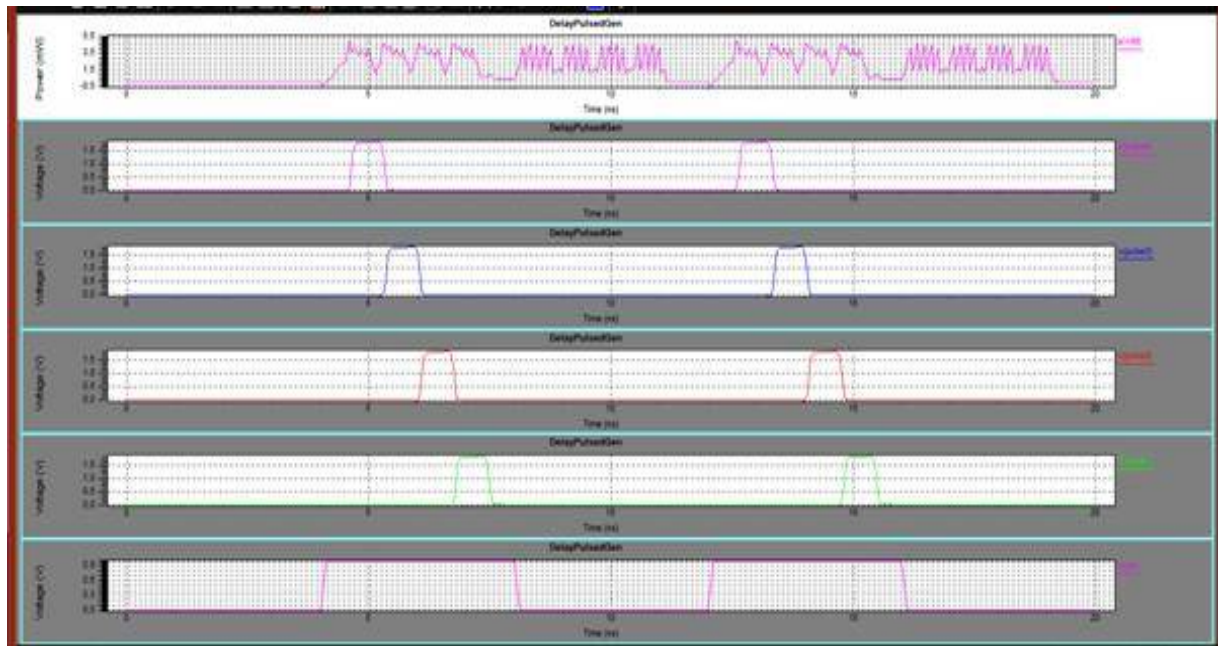

Fig. 3 Schematic of Delayed pulse clock generator

Fig. 4 Delayed pulse clock generator output waveform

Johnson counter using pulse latch

The Johnson counter is an alteration of Ring counter. In Johnson counter, the inverted output of the last stage flip-flop is feedback as the input of first flip-flop. If we use n flip-flops to design the Johnson counter, it is known as 2n bit Johnson counter or Mod 2n Johnson counter.

Johnson counter requires only half number of flip-flops as compared to a Ring counter to design the same Mod counter. It is also an important advantage of it.

The main difference between the 4 bit Ring counter and the Johnson counter is that, in Ring counter, we connect the output of last flip-flop directly to the input of first flip-flop where as in Johnson counter, we feedback the inverted output of last stage to the first stage input. The Johnson counter is also called Twisted Ring Counter, with a feedback. It is also known as switch tail Ring counter.
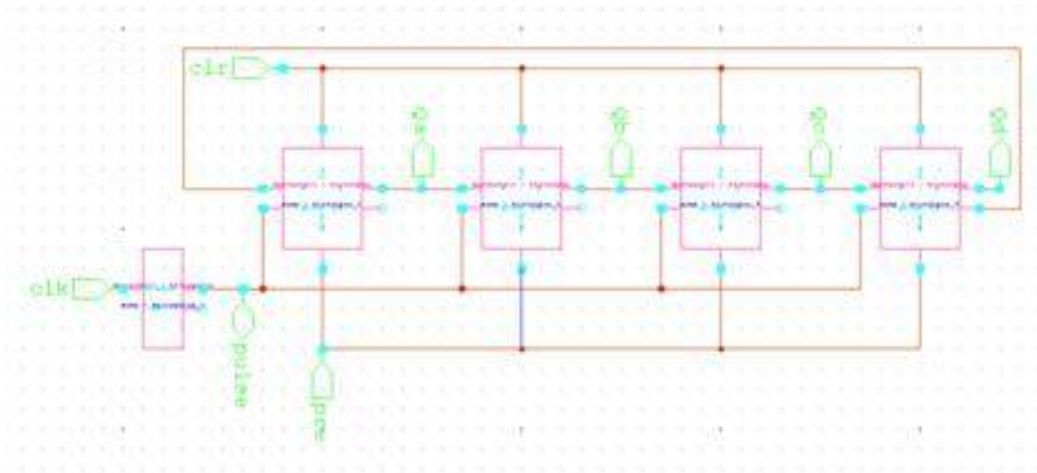
Fig. 5 Johnson counter using pulsed latch

V. CONCLUSIONS

The requirement of replacement element for flip-flops in recent trend, led to migration from flip-flops to the pulsed latch for low power consumption, less area and delay applications. In this thesis, we have proposed different applications of pulsed latch using 180nm technology in Tanner tool v 14.1 and performance is compared with application using flip-flop. The number of transistors utilized in pulsed latch is less than that of flip-flop, hence area is significantly reduced. Pulsed latch circuit saves power consumption and power delay product in comparison with flip-flop circuit hence it can be inferred from the results that the circuits using the pulsed latches can be used instead of flip-flop for low power, less area and high speed applications. It also eliminates one latch per cycle and doesn't require clock complement. Other advantages include minimised sequencing overhead**,** easier timing verification**,** lower delay and time borrowing capability. The trading towards applications using pulsed latches from conventional flip-flop circuits in heavy pipelining, mobile devices or in low power ASIC circuits is immense achievement in field of VLSI designin

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