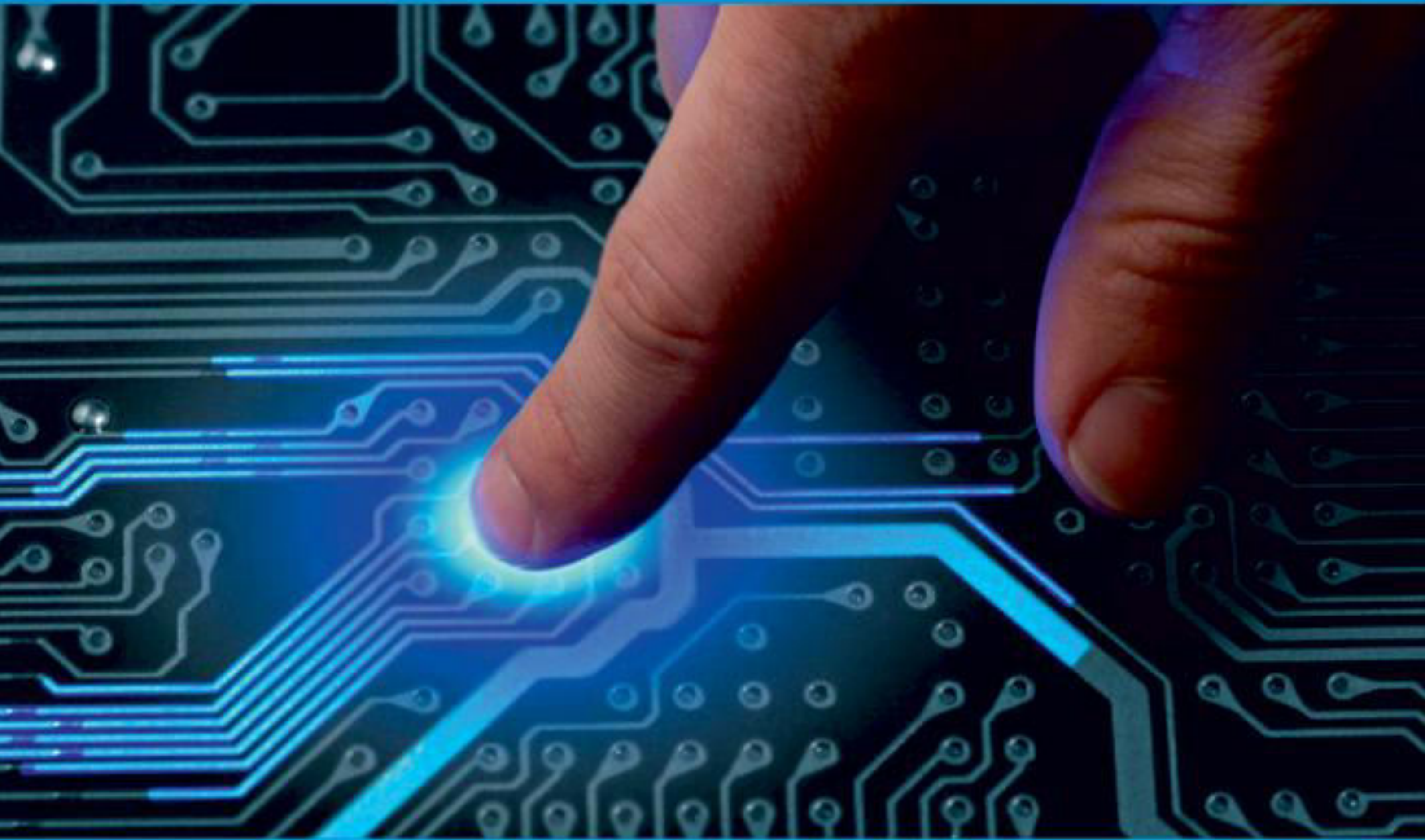
IJIRCCE

e-ISSN: 2320-9801 | p-ISSN: 2320-9798



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN COMPUTER & COMMUNICATION ENGINEERING

Volume 9, Issue 8, August 2021

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

Impact Factor: 7.542

International Journal of Innovative Research in Computer and Communication Engineering

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.542

|| Volume 9, Issue 8, August 2021 ||

| DOI: 10.15680/IJIRCCE.2021.0908033 |

A (15, 5, 7) BCH Encoder AND Decoder for Data Transmission

Rakesh B Shettar, Ravi Hosamani , Praveen Kumar Y G

Asst. Professor, Dept. of Electronics & Communication Engineering, KLE Institute of Technology, Hubballi, Karnataka, India

Asst. Professor, Dept. of Electronics & Communication Engineering, KLE Institute of Technology, Hubballi, Karnataka, India

Asst. Professor Dept. of ECE, Sri Siddhartha Institute of Technology, SSAHE, Tumkuru, India

ABSTRACT: This paper describes the design of (15,5,7) BCH encoder and decoder using mathematical derivation BCH code is one of the most important cyclic block codes. where 15, 5 and 7 represents the block length(n), data length(k) and maximum number of correctable errors(t) respectively. A brief introduction to the BCH code is given. The objectives fulfilled are written. Reference papers and texts are mentioned. The procedure to obtain minimal polynomials for a given code specification of n and d (or t), is explained for (15, 5) code with d=7. The generator polynomial is then obtained with LCM of M1(x)M3(x)M3 (x). Decoding method is explained with the help of an example for one combination of received words. BCH decoding procedure using PGZ (Peterson Gorenstein Zierler) is explained. Syndrome calculation is presented and decoding steps are discussed. Results of BCH encoding and decoding are tested using built-in functions in Matlab for n=15, k=7, 2-bit error-correcting code.

KEYWORDS: Bose Chaudhuri Hocquenghem (BCH), BCH Encoder, BCH Decoder .

I. INTRODUCTION

A cyclic code is a block code, where the circular shifts of each codeword give another word that belongs to the code. They are error-correcting codes that have algebraic properties that are convenient for efficient error detection and correction.

In coding theory, the BCH codes or Bose–Chaudhuri–Hocquenghem codes form a class of cyclic error-correcting codes that are constructed using polynomials over a finite field(also called Galois field). BCH codes were invented in 1959 by French mathematician Alexis Hocquenghem, and independently in 1960 by Raj Bose and D. K. Ray-Chaudhuri. The name Bose–Chaudhuri–Hocquenghem (and the acronym BCH) arises from the initials of the inventors' surnames (mistakenly, in the case of Ray-Chaudhuri[1][2]).

One of the key features of BCH codes is that during code design, there is precise control over the number of symbol errors correctable by the code. In particular, it is possible to design binary BCH codes that can correct multiple bit errors. Another advantage of BCH codes is the ease with which they can be decoded, namely, via an algebraic method known as syndrome decoding. This simplifies the design of the decoder for these codes, using small low-power electronic hardware [1].

Given a prime number q and prime power q^m with positive integers m and d such that $d \leq q^m - 1$, a primitive narrow-sense BCH code over the finite field (or Galois field) GF(q) with code length $n = q^m - 1$ and distance at least d, is constructed by the method mentioned in the next paragraph-

Let α be a primitive element of GF(q^m). For any positive integer i, let $m_i(x)$ be the minimal polynomial with coefficients in GF(q) of α^i. The generator polynomial of the BCH code is defined as the least common multiple $g(x) = \mathrm{lcm}(m_1(x),\ldots,m_{d-1}(x))$. It can be seen that g(x) is a polynomial with coefficients in GF(q) and divides $x^n - 1$. Therefore, the polynomial code defined by g(x) is cyclic [2].

II. RELATED WORK

In [1] K. Rajani C. Raju, in "Design and Implementation of Encoder for (15, k) Binary BCH Code Using VHDL", BCH codes are excellent error-correcting codes among codes of short lengths. They are simple to encode and relatively simple to decode. Due to these qualities, there is much interest in the exact capabilities of these codes. The speed and device utilization can be improved by adopting parallel approach methods. Samir Jasim Mohammed in

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.542

|| Volume 9, Issue 8, August 2021 ||

| DOI: 10.15680/IJIRCCE.2021.0908033 |

"Implementation of Encoder for (31, k) Binary BCH Code based on FPGA for Multiple Error Correction Control", explains the design and implementation of BCH encoders using a Field Programmable Gate Array (FPGA). The proposed BCH encoders have been designed and simulated using Xilinx-ISE 10.1 Web PACK and implemented in a xc3s700a-4fg484 FPGA and the results show that the system works quite well. Amit Kumar Panda, Nalini Tiwari, in "Design and Implementation of (63, 45) Binary BCH code Encoder on Spartan 3 FPGA for Noisy Communication Channel", have designed and shown excellent error-correcting codes among codes of short lengths. FPGA implementation of (63, 45) BCH encoder has simplified the design for error correction in various wireless communication networks like Wimax, Wifi, Bluetooth, etc and the results show that it can operate at a maximum frequency of 217.533 MHz by consuming less power and negligible resources of the target device. In the text 'The Art of Error Correcting Coding' by Robert H. and Morelos Zaragoza [4], BCH decoding schemes are explained with examples. From the literature survey, it is observed that BCH codes are used in applications such as compact disc players, DVDs, disk drives, solid-state drives, two-dimensional bar codes, and satellite communications [1].

The knowledge of an error-correcting code by classical means is to be known to explore the decoding schemes using deep learning methods in the future scope of the study. This is because, it is expected that there will be a paradigm shift in decoding schemes in the present and future era of exploitation of artificial intelligence, neural networks, and deep learning. Thus, knowing that it will give a future scope of research, the work is carried out with following approach on the design of the BCH error correction code[5]

- Design of (15,5,7) BCH code in Matlab is accomplished.
- Encoder, as well as decoder, are verified to work satisfactorily.
- Performance in AWGN channel is checked and Pe vs. SNR plots are obtained.

Error-correcting capacity is decided by the specification of the code. If errors are more than the designed value, error correction is not guaranteed.

In Section, I of the paper brief introduction to the BCH code is discussed.In Section II, a brief of the procedure to obtain minimal polynomials for a given code specification of n and d (or t), is explained for (15, 5) code with d=7. The generator polynomial is then obtained with LCM of($m_1(x),\ldots,m_{d-1}(x)$) and the decoding method is explained with the help of an example for one combination of received words. In Section III, results of encoding and decoding are shown. Pe (Probability of bit error) vs. SNR (Signal to Noise Ratio) in AWGN channel, with different data sizes, are presented. The report ends with conclusions in Section IV. Bibliography is given for the reader's reference.

III.METHODOLOGY

BCH Encoding- Any polynomial that is a multiple of the generator polynomial is a valid BCH codeword, BCH encoding is merely the process of finding some polynomial that has the generator as a factor. The BCH code may be implemented either as a systematic code or not, depending on how the implementer chooses to embed the message in the encoded polynomial [2]. Binary BCH codes are defined in the following manner [5].
binary BCH code with the following parameters-

For any integer $m \geq 3$ and $t < 2^{m-1}$, there exists a binary BCH code with the following parameters-

- Block Length or code Length n<2m-1
- Number of parity digits n-k<mt $n - k \leq mt$
- Minimum distance dmin>2t+1
- Where t is the error-correcting capability of the code

This code is capable of correcting any combination of t or fewer errors in a block of length $n<2^m-1$.Hence, we call it error-correcting BCH code.

Let us consider the binary word 10001 which represents D and is placed in 7-bit of information which is then appended with a 3-bit sequence. Thus, the 15-bit sequence is divided with generator polynomial to obtain a remainder. By combining the message sequence with the remainder sequence, the codeword is obtained

$c(x)=x^{n-k}\, m(x)+r(x)$100011110101100)---equ (1)

BCH Decoding- Decoding is considerably more complicated and requires three steps after a data vector is received. Given a BCH code that can correct t errors, the steps are[5, 6]-During some of these steps, the decoding algorithm may determine that the received vector has too many errors and cannot be corrected. For example, if an appropriate value

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.542

|| Volume 9, Issue 8, August 2021 ||

| DOI: 10.15680/IJIRCCE.2021.0908033 |

of t is not found, then the correction would fail. In a truncated (not primitive) code, an error location may be out of range. If the received vector has more errors than the code can correct the decoder may unknowingly produce a valid message that is not one way we sent[2].

- **Example :**BCH(15,5,7) code has primitive polynomial *p(x)*=x^4+x+1.The received r(x)=x^7+x. Compute the syndrome and estimate the received codeword d=2t+1, 7=2t+1, t=3, three error-correcting code. 2t=6. The test results in the design of BCH decoding are presented in this section.

Testing the error correction of message = 0 0 0 1 0

Error correction is verified by making received bits as wrong shown with red color (or bold font) in 'rec'

i. Rec = [0 0 0 1 0 1 0 0 1 1 0 1 1 1 0];
no errors occurred
d = 0 0 0 1 0

ii. Rec = [0 0 0 1 0 1 0 0 1 1 0 1 1 1 **1**];
d = 0 0 0 1 0

iii. rec=[0 0 0 1 0 1 0 0 1 1 0 1 1 **0** **1**];
d = 0 0 0 1 0

iv. rec=[**1** 0 0 1 0 1 0 0 1 1 0 1 1 **0** **1**];
d = 0 0 0 1 0

v. rec=[**1** 0 0 1 0 1 0 0 1 1 0 **0** 1 **0** **1**];
d = **1** 0 0 1 0

following Observations made from the solution of previous example; (i), no error occurred gives the correct encoded bits. In (ii) (iv), errors are introduced in bit positions and marked with red color (or bold font) with reference to (i).In (ii) to (iv), three errors are corrected to make decoded same as message.In (v), errors are in more than 3 positions, therefore, output is different. Testing the error correction of message=10001

i. rec=[1 0 0 0 1 1 1 1 0 1 0 1 1 0 0];
1. no errors occured
2. d= 100 0 1

ii. rec=[1 0 0 0 1 1 1 1 0 1 0 1 1 0 **1**]
1. d= 100 0 1

iii. rec=[1 0 0 0 1 1 1 1 0 1 0 1 1 **1** **1**];
1. d= 100 0 1

iv. rec=[1 0 0 0 **0** 1 1 1 0 1 0 1 1 **1** **1**];
1. d= 100 0 1

v. rec=[1 0 0 0 **00** 1 1 0 1 0 1 1 **1** **1**];
1. d= 100 0 **0**

following Observations made from the solution of previous example; (i), no error occurred gives the correct encoded bits. In (ii) to (iv), errors are introduced in bit positions and marked with red color about (i).In (ii) to (iv), three errors are corrected to make decoded the same as a message. In (v), errors are in more than 3 positions, therefore, the output is different

IV. RESULTS AND DISCUSSION

In this chapter, results obtained by simulating programs for (15,5) BCH encoding, decoding, Pevs SNR plots with AWGN channel and with fading channel are presented. Following is the table for different message bits to encoded outputs

Table 1 Message input and Encoded output of (15,5) BCH code

Sr. No.	Message input	Encoded output
1	0 0 0 0 0	000000000000000
2	0 0 0 0 1	00001010011011 1
3	0 0 0 1 0	000101001101110

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.542

|| Volume 9, Issue 8, August 2021 ||

| DOI: 10.15680/IJIRCCE.2021.0908033 |

4	0 0 0 1 1	000111101011001
5	0 0 1 0 0	001000111101011
6	0 0 1 0 1	001010011011100
7	0 0 1 1 0	001101110000101
8	0 0 1 1 1	0 0 1 1 1 1 0 1 0 1 1 0 0 1 0
9	0 1 0 0 0	010001111010110
10	0 1 0 0 1	010011011100001
11	0 1 0 1 0	010100110111000
12	0 1 0 1 1	010110010001111
13	0 1 1 0 0	011001000111101
14	0 1 1 0 1	011011100001010
15	0 1 1 1 0	011100001010011
16	0 1 1 1 1	011110101100100
17	1 0 0 0 0	100001010011011
18	1 0 0 0 1	1 0 0 0 1 1110101100
19	1 0 0 1 0	1 0 0 1 0 0 011110101
20	1 0 0 1 1	1 0 0 1 1 0111000010
21	1 0 1 0 0	1 0 1 0 0 1101110000
22	1 0 1 0 1	1 0 1 0 1 100100011 1
23	1 0 1 1 0	1 0 1 1 0 0100011110
24	1 0 1 1 1	1 0 1 1 1 0000101001
25	1 1 0 0 0	1 1 0 0 0 0101001101
26	1 1 0 0 1	1 1 0 0 1 0001111010
27	1 1 0 1 0	1 1 0 1 0 1100100011
28	1 1 0 1 1	1 1 0 1 1 1000010100
29	1 1 1 0 0	1 1 1 0 0 0010100110
30	1 1 1 0 1	1 1 1 0 1 0110010001
31	1 1 1 1 0	1 1 1 1 0 1011001000
32	1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

A. **Decoding of (15,5) BCH code**

- The decoding is explained in section II using an example. (15, 5) BCH code with AWGN channel for data size-1000

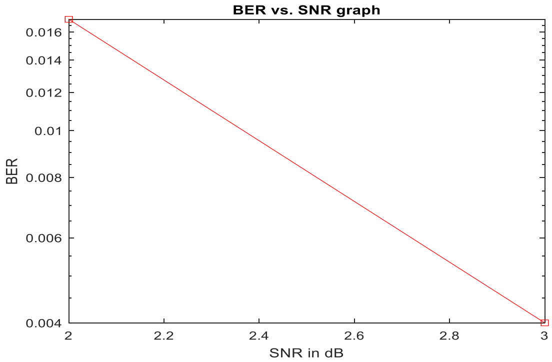


Fig.1 BER vs SNR plot for message bits of 1000

Table 2. SNR , Error bits for encoded bits 1000

SNR	23	4	5	6	7	8
Error	174	0	0	0	0	0
Encoded Bits	1000/5=200 sets of 5 bits x 15=3000 bits					

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.542
|| Volume 9, Issue 8, August 2021 ||
| DOI: 10.15680/IJIRCCE.2021.0908033 |

- (15, 5) BCH code with awgn channel for data size- 10000

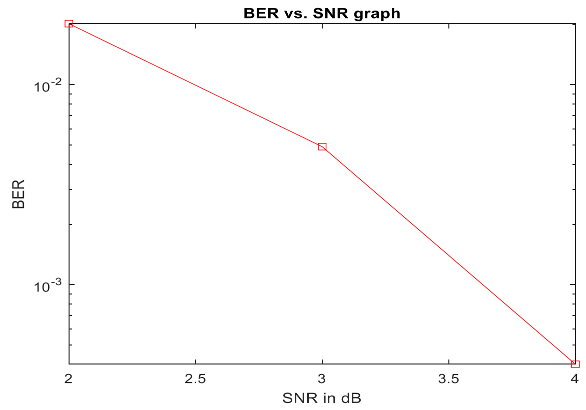


Fig.2 BER vs SNR plot for message bits of 10000

Table 3. SNR , Error bits for encoded bits 10000

SNR	23	4	5	6	7	
Error	20249	4	0	0	0	000000
Ratio 0.0202	0.0202	0.0049	0.00040	0	0	0.0049
Encoded Bits	100005=2000 sets of 5 bits x 15=30000 bits					

- (15, 5) BCH code with AWGN channel for data size- 100000

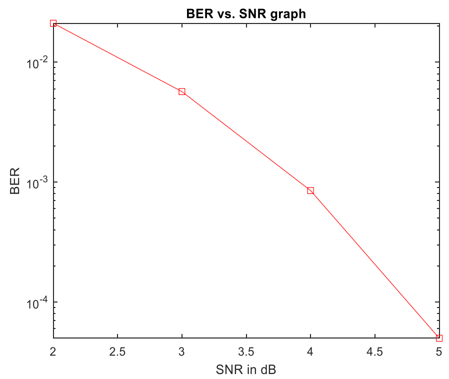


Fig.3 BER vs SNR plot for message bits of 50000

Table 4. SNR , Error bits for encoded bits 50000

SNR	23	4	56	789	10111213	
Error	1068	260	68	00	0	0
Pe0.021360.00520.0013600				00000	00	

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.542

|| Volume 9, Issue 8, August 2021 ||

| DOI: 10.15680/IJIRCCE.2021.0908033 |

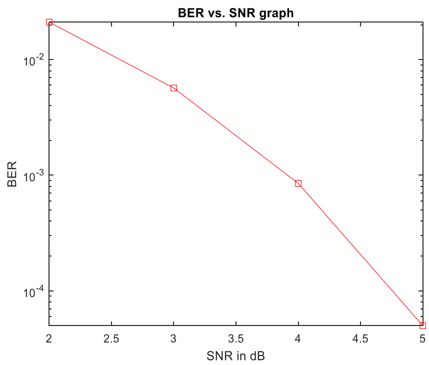


Fig.4 BER vs SNR plot for message bits of100000(1 lakh)

Table 5. SNR , Error bits for encoded bits 100000

SNR	23	4	56	789	10111213	
Error	2109	568	85	50	00000	00
Pe2.109 e-025.68 e-03 8.5 e-045.0e-0500000000						

Execution time in matlab Start time 14.16 pm; End time 14.56 pm Total 40 minutes execution time for 1lakh message bits.

IV. CONCLUSIONS

Encoder and decoder using mathematical derivation BCH code is one of the most important cyclic block codes as seen in communication system . Results of BCH encoding and decoding are tested using built-in functions in Matlab for n=15, k=7, 2-bit error-correcting codes, also results are verified with working for n=15, k=5, t=3 BCH code is given. results also verified for the same . The correct design of minimal polynomials M(x) and generator polynomial g(x), essential for decoding are verified with the reference[5]. Encoding and decoding without adding noise are tested and verified. The codes are verified to successfully correct the error in three-bit positions as verified.A performance of $Pe=10^{-5}$ is obtained for SNR of 5 dBs, in awgn channel using Matlab for different data sizes of message bits from 1000 bits to 1 lakh bits are presented.

REFERENCES

1. K. Rajani, C. Raju, Design and Implementation of Encoder for (15, k) Binary BCH Code Using VHDL, International Journal of Engineering Research & Technology (IJERT), Vol. 2, Issue 9, September 2013.
2. BCHcodes. https://en.wikipedia.org/wiki/BCH_code#cite_note
3. GaloisField(Finitefield).http://www2.siit.tu.ac.th/prapun/tcs455/ece561%2005%2001%20Polynomials%20over%20Galois%20Field.pdfPrimitivePolynomials.http://www.uobabylon.edu.iq/eprints/paper_1_17490_649.pdf
4. Shu Lin and D. J. Costelo, Error Control Coding, Second Edition, Pearson-Prentice Hall.
5. Robert H. and Morelos Zaragoza, The Art of Error Correcting Coding,Second Edition, Wiley India Edition, 2013.
6. Simon Haykin, “Communication Systems”, 4th Edition, John Wiley & Sons, Inc.
7. W.W.Peterson, “Encoding and Error-Correction procedures for the Bose-Chaudhuri Codes”, IRE Trans. Inf. Theory, IT6, p. 459-470, Sep. 1960.
8. Yunghsiang S. Han, “BCH Codes”, Graduate Institute of Communication Engineering, National Taipei University Taiwan.
9. W.W.Peterson, “Encoding and Error-Correction procedures for the Bose-Chaudhuri Codes”, IRE Trans. Inf. Theory, IT6, p. 459-470, Sep. 1960.
10. Yunghsiang S. Han, “BCH Codes”, Graduate Institute of Communication Engineering, National Taipei University Taiwan.
11. Shu Lin and Daniel J. Costello, Jr., —Error Control Coding, Englewood Cliffs, New Jersy: Prentice Hall, Chapter 1, 1983.

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.542

|| Volume 9, Issue 8, August 2021 ||

| DOI: 10.15680/IJIRCCE.2021.0908033 |

BIOGRAPHY

Rakesh B Shettar obtained his BE degree in Electronics & Communication Engineering in 2008 and Master of Technology from VTU Belgavi , Karnataka ,India 2010**.** He is currently working as assistant professor in the department of Electronics & Communication Engineering, K.L.E Institute of Technology, Hubballi, Karnataka, India. With over 11 year of teaching experience.He is a member of International Association of Engineering (IAENG). His research interest are Signal Processing, Image Processing.

Ravi Hosamani obtained his B.E. degree in Electronics and Communication Engineering In 2006 and Master of Technology from VTU, Belagavi, Karnataka, India, in 2010. He currently working as Assistant Professor in the Department of Electronic and Communication Engineering, K.L.E. Institute of Technology, Hubballi, Karnataka, India. With over 11 years of teaching experience. He is a member of IEEE,ISTE , IEI and IAENG .He has authored/co-authored articles in referred international and national journal and conference. His research interests are VLSI, Signal processing.

Y.G.PraveenKumar obtained his B.E. degree in Electronics and Communication Engineering from VTU, Belagavi, Karnataka, India in 2008 and Master of Technology in VLSI Design and Embedded Systems from the same university in 2010. He has been working as Asst. professor in the Department of Electronics and Communication Engineering, Sri Siddhartha Institute of Technol-ogy, Tumakuru, Karnataka, India for 9years. He is a life member in Indian Society for Technical Education (ISTE). He has authored Jco-authored more than 25 articles in refereed international journals and conferences. His research interests are in the areas of VLSI System Design, Low power applications, Digital Design.

INNO SPACE
SJIF Scientific Journal Impact Factor
Impact Factor: 7.542

doi crossref

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

निस्केयर NISCAIR

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN COMPUTER & COMMUNICATION ENGINEERING