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Design of Low Power IC Clock Tree

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ABSTRACT: When the reliability of the processing of varieties becomes a important issue is the wires in the clock tree Very wide to limit the oblique process to a specific acceptable value. Due to the increase in total capacity, the power dissipation in the clock-net is dramatic increased. We show that despite the buffer mismatch and an additional component of energy dissipation due to their short-circuit currents, the power of the clock tree can be significant reduced by buffer insertion provided constraint permissible dependence on process variance and maximum slope current densities (electromigration).

KEYWORDS: Energy efficient algorithm; Manets; total transmission energy; maximum number of hops; network lifetime

I. INTRODUCTION

Clock trees are generally designed to achieve minimal oblique, and sometimes reduced delay. Several algorithms [11-[3] have recently been proposed to achieve these objectives. Most Alignment algorithms expand or extend the metal interconnection, which can significantly increase the total value net clock capacity. Capacity of the clock grid can be the dominant factor for the total clock power dissipation of the clock, and even the total dissipation of the chip [9]. This The huge capacity of the tree clock is due to the large metal The width required for the main roads from the tree side electromechanical restriction and process deviation reliability point of view.

Well known fact is that the buffers in the clock They cause a jump because of differences in their characteristics. Incorrect buffering, however, is not the only sourcc process- deviation induced by deviation. Width of metal wire and The thicknesses can vary considerably within the integrated circuit because of the local and global disruption of the process. If we consider how broad Metal wires must be in order to control the process induced oblique [7] [8], total volume is increased significantly. Therefore taking into account a certain amount permissible cross section induced by change of the process we can consider compromise between buffer insertion and mesh width correction while simultaneously reducing the total power. In this document, taking into account the constant maximum change of wire Aw width and reliability criterion that the maximum tilt must be less than some acceptable tilt S ", we show Potential power reduction possible with buffered solutions. We show examples for which the power component due to Buffers increase the total power, however, the maximum Metal widths necessary for the reliability of the process variant even less. Our results show 25-50% Reduce total power dissipation by adding buffers while limiting the slope process. Similar results may be shown on the project limited electromigration. Total power can be further reduced by "disconnecting" Clock to logic parts that are inactive. Indirect The buffers again provide us with excellent ways of isolating Inactive components on the chip without affecting Delays in active ingredients.

II. POWER ESTIMATION

You can calculate the total power distributed in the clock tree by

$$P = Ef \quad (1)$$

where E denotes the total energy per cycle and also the clock frequency. Me consists of two components "- 1) charging the batter Emetnl metal connector and 2) Energy dispersed by buffers E,. The interconnect component is associated with loading / unloading the grid capacity through resistance and can be calculated as shown below:

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$$E_{metal} = \frac{1}{2} C_{tot} V_{dd}^2$$

where Vdd is the supply voltage and C is the total capacity on the Web. Buffers disperse extra power due to "Rush through" the present ingredient. Let's consider, for example The inverter shown in Fig. 1 (a). When the input is switching, both N and P transistors are conducted for a short term. Because the "resistance" of these transistors is very large small, large current flows through the transistors during this interval. The current course during switching is shown in Fig. 1 (b). Energy dispersed by the buffer The slider element is the product of the voltage and the area under the current curve:

$$E_{rt} = V_{dd} \int_0^T i_{rt}(t)\, dt$$

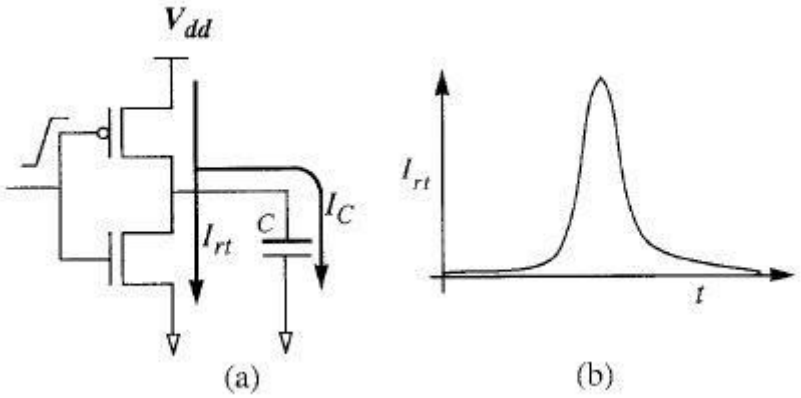

Figure 1, Rush through current in an Inverter

Z (l), (2) and (3) the total power in the clock tree of b buffers are served by

$$P = f\left(E_{metal} + \sum_{i=1}^{b} E_{rt_i} \right)$$

where the sum in (4) is above all the buffers in the clock tree. Later, we will know that buffer insertion causes small Err component increment, while significant Reduction of the Emeral component ensures a reliable appearance. BEHIND The clock can be designed to meet latency and worst case jump limitation with several possible combinations Emern / and X. The sum of these quantities is minimized by Search O (N) to determine the location of the buffer. How to search this It consists of generating several possible combinations of zeroes The intcrconnect script driven by intermediate buffers uses a linear zero-stroke jog algorithm described in [8] for design purposes connect to.

III. RELIABILITY AND WIRE WIDTHS

For typical process, peak or medium currents can change K3% of nominal value, while width The connection can vary by as much as 20% of the minimum function size in chip. Therefore, it is obvious that the tilt Due to changes in the interaction may be important. We estimate the impact of wire width fluctuations on delay to the clocked element using the Elmore delay model [4].
(See Appendix A for details). According to this model, the nominal delay for the clocked element
n, T from the root controller (tree root) by

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$$T_{D_n} = \sum_{i \in P(n)} R_i C_{d_i}$$

where P (n) is the set of branches that lie on the path root to node n. Let A denote the maximum (+ or -) change in wire width as a result of process variations. Let AR and ACi signify appropriate changes of resistance and capacitance wire i. Change the delay for each node branch and is then given by (z (5))

$$\Delta T_{D_n} = \Delta R_i C_{d_i} + \Delta C_i R_{u_i}$$

The maximum delay change AT, on the leaf n, is approximately equal the sum of the delay changes for each branch in path to the root,

$$\Delta T_n \approx \sum_{i \in P(n)} \Delta T_{D_i}$$

Process distortions in branches that do not lie in Path to root also has an effect on delay, but their effect is very large small and can be neglected. Because this change can be positive or negative worst oblique in the zero oblique clock tree is

$$S_{wc} = 2|\Delta T_{max}|$$

where ATmax denotes the greatest change in decay in the leaf collar due to differences in the process. If the maximum permissible skewness for a S net clock, we believe the net clock reliable if

$$S_{wc} \leq S_I$$

From (7) and (8)

$$\sum_{i \in P(n)} \Delta T_{D_i} < S_I/2$$

for each node n in the clock tree. If it is the worst case of slope Evenly distributed to all levels of the tree, (10) translates into a limit the minimum width [SI for each wire in the clock tree given by

$$w_j \geq \sqrt{2\Delta w r l_j C_{d_j}/S_{t_j}}$$

The equation (1 1) is an invariant real process j. For electromigration, similar minimum width limits are used considerations. From (11) it follows that ex grows as a square root Cd. Note that for a clock tree, Cd grows exponentially as one moyes with leaf nodes to the root of the number of loads increase exponentially. Therefore, in the case of uneven slope allocation S, the minimum wire width increases exponentially as one ggts closer to the root. The capacity of these wires, which is a function of their width also grows and is The main reason for increasing power. To reduce the overall It is necessary to reduce the minimum wire width reliability. Because in (1 1) every quantity except C is defined fixed to reduce the maximum width the only way decrease Cd. In the next section we discuss how you can reduce the C4 and to reduce the required wire width and thus the total power dissipation, while maintaining the same tilt scale.

Example

Consider the clock tree buffer shown in Fig. 2 (a). Let Line widths 1 and 2 should be designed to be tolerated Oblique S Without loss of generality let each load be CL and let the capacitance of each wire in the sub-trees 1 and 2 be C, For reliability, from (1 I),

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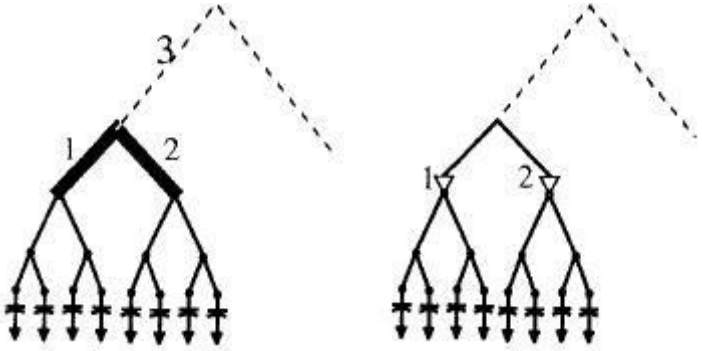

Figure 2. Clock trees with and without buffers

$$w_{1min} = \sqrt{(C_d r l_1)/S_{t_i}},\ w_{2min} = \sqrt{(C_d r l_2)/S_{t_i}}$$

where,

$$C_d = 6C_w + 4C_l$$

It is obvious that with the increase of the depth of the tree in the lower course capacity increases exponentially. Capacity Lines 1 and 2 are

$$C_1 = cl_1 w_{1min},\ C_2 = cl_2 w_{2min}$$

Wires in conduits 1 and 2 (conductor 3) will have a drop of the stream capacity

$$C_{d_3} = 2C_d + C_1 + C_2$$

Let's now consider the same clocks with buffers inserted in Nodes 1 and 2 as shown in Fig. 2 (b). With intermediate buffers The capacity of wires 1 and 2 is simple input capacitance C,. Minimum wire width 1 and 2 in this case arc

$$w_{1min} = \sqrt{(C_b r l_1)/S_{t_i}},\ w_{2min} = \sqrt{(C_b r l_2)/S_{t_i}}$$

Thc reducing the width of these wires reduces the capacity net. Total loss of capacity of wires 1 and 2 is given by

$$\Delta C_{1,2} = c\sqrt{r/S_{t_i}}\{\left(l_1^{3/2}\sqrt{C_d} - \sqrt{C_b}\right) + l_2^{3/2}\left(\sqrt{C_d} - \sqrt{C_b}\right)\} + 2C_b$$

Moreover, duc for smaller capacity, wires above 1 and 2 can now have narrow widths. Is net loss of total distributed power, if

$$\frac{1}{2}\Delta C V_{dd}^2 > 2E_{rt}$$

where AC is the total loss of network capacity because of buffer insertion. In gcncral exact effect No intermediate buffer insertion can be expected Because it is difficult to determine the actual capacity drop. In addition, buffer locations The length and width of interconnects are interdependent

This makes the problem even more complicated. In addition, you need to consider the sloping location Buffer mismatch and buffer load imbalance. We do a linear search [8], which considers these issues in order to determine effect of buffers in different places. Of all possible configures, buffers locations in the clock tree that Minimizes power for constant delay.

IV. RESULTS

We have determined the effect of buffer insertion on the total Energy dissipation in five comparative examples of deyacto presented in [11. Delay buffer and rush through power are modeled as the CL load function by a simple k factor empirically. For intra-chip modeling, We have been able to change the width of the metal by 15% From the size

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of the function thanks to topography, digestion and displacement of the mask. Similarly, the capacity of the buffer drive is assumed They differ by about 5% of the nominal value. This is very pessimistic Considering that the average peak currents are different only 3%. For the I-level clock tree with n-pins we fix everything possible combinations of buffer levels, using up to one to one stages buffering (ie possible solutions in case of clock). Table 1 shows examples of buffer insertion.

Exa-mple Ckt	width w/o buffers (µm)	width with buffers (µm)	C_{total} w/o buffers (pF)	C_{total} with buffers (pF)
r1	10.42	2.45	86.34	49.83
r2	18.96	2.57	201.27	102.14
r3	20.61	2.66	316.27	127.15
r4	24.43	2.56	767.20	279.20
r5	37.47	3.51	925.06	369.08

Table 1. Wire Widths for Reliability

presented in [11. Column 2 shows the maximum wire width in the clock tree when buffers are not inserted. Widest The wires are closest to the root because they see the maximum stream capacity down. Then we design a clock tree for identical delay and worst case of slope, but with insertion intermediate buffers. The width corresponds to the position Buffers that minimize overall power for a given delay. Note that there is a significant decrease in the maximum value wire widths when intermediate buffers are inserted. We see dramatic tenfold decrease in wire width for the biggest example. Columns 4 and 5 show the effect Reduce the width of the wires to the total clock capacity network. Assuming a clock speed of 200 MHz, we calculate the power in buffered and unbuffered clock trees. Table 2 shows Power results for these examples. Column 4 indicates reduced power due to reduced capacity inserting a buffer. Column 5 shows the power increase for additional buffers. In all cases we see that reduced The capacity has reduced the total power by more than increases due to the rush through the power in the buffers as a result net decrease in total power.

We should point out that further reduction in power can

Exam-ple Ckt	P w/o buf-fers (W)	P with buf-fers (W)	P_{metal} redu-ction (W)	P_{rt} due to buf fers (W)	Gain in P (%)
r1	0.215	0.162	0.091	0.038	24.65
r2	0.503	0.339	0.247	0.083	32.60
r3	0.790	0.414	0.472	0.096	47.59
r4	1.918	1.092	1.220	0.394	43.06
r5	2.312	1.122	1.389	0.199	51.47

Table 2. Capacitances and Power Reduction

to be obtained by appropriate determination of the chip sections The clock may be off when responding logic is inactive. We propose the following modifications estimate the power of the connection in this case:

$$E_{metal} = (C_{equivalent} V_{dd}^2) / 2$$

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Where

$$C_{equivalent} = \sum p_i C_i$$

pI is likely to have a capacity of C. Clearly CPqrrlrvrrl2P Cn, ("giving further benefits. Finally, we will show the effect of increasing the number buffer level in the clock tree in Fig. 3 for the largest example - r5. As the number of buffer levels is higher, the power decreases initially, and then begins to grow. As more and more More levels of buffers are added to the hurry thanks to the power Buffers start to dominate the charge / discharge component connections. In addition, the capacity The net also starts to increase due to the excessive number of buffers. When more buffers are added, the number of buffers and The net capacity caused by additional buffers increases both slip through the component and the metal component power.

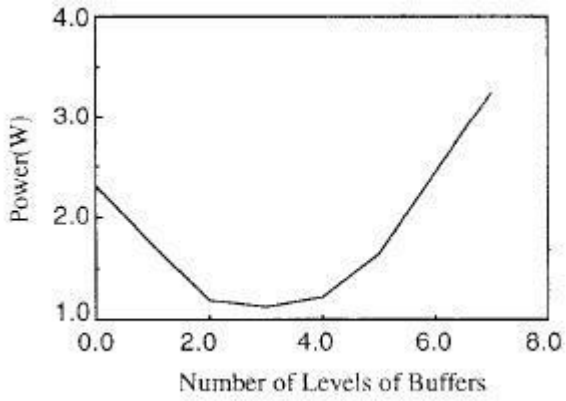

Figure 3. Effect of buffer levels on power

V. CONCLUSIONS

We have shown the effect of inserting buffers on an integer power dissipated in a reliable clock. Our results indicate The insertion of intermediate buffers can reduce power When we consider reliability as a result of process interruptions. The The maximum improvement for our examples is 50%, but we do Expect that the percentage will rise along with the clock size tree.

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BIOGRAPHY

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