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Power Analysis of Comparators at Various Process Corners

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ABSTRACT: In modern era of CMOS technology the double-tail comparators uses the dynamic method which mainly minimizes the power and voltage at a greater extent. CMOS circuit designing at a low power in Ultra Deep Sub-micrometer (UDSM) CMOS technologies becoming challenging day by day. In this paper, different types of dynamic double-tail comparators are simulated. Also the proposed dynamic double-tail comparator and modified double-tail comparator is simulated at lower supply voltages to check the validity at various process corners. The validity of model is checked on the basis of power analysis of the comparators. Pre-simulation results are shown using 0.18μm CMOS technology which confirm the results.

KEYWORDS: Double-Tail comparator, four corner analysis, clock comparator, clock gating.

I. INTRODUCTION

Comparators are the widely used elements for designing electronics components in the modern VLSI design. The accuracy of comparators depends on its power consumption and speed. The decision making response time of the comparator gets limited by the speed of conversion. The basic functionality of a CMOS comparator is to compare, whether a signal is greater or smaller than zero or to compare an input signal with a reference signal and outputs a signal which is near supply voltages based on comparison.

Comparator acts as interface between the analog and digital signal. In analog to digital conversion process, the input is first sampled (using sample and hold circuit) and is used with a combination of comparators to get the digital equivalent of the required analog signal.

Nowadays analog-to-digital converter operate at lower power dissipation, low noise, better slew rate, high speed, less hysteresis, less Offset. In ADCs typically inter-stage gain amplifiers and comparators are main performance limiting block. Dynamic comparators are being used in today's A/D (analog to digital) converters extensively because these comparators have high speed, operate at lower power dissipation, with zero static power consumption and outputs full-swing near digital valuevoltage in shorter time duration. Back-to-back inverters in these dynamic comparators provide positive feedback mechanism which converts a smaller voltage difference in full scale digital level output [1], [2].

The comparator consist of a high gain differential amplifier and regenerative latch. The differential amplifier usually implemented with two transistor circuit called a long-tailed pair of MOS. The comparator has two output states which is at near zero or supply voltage. New circuit structures which avoid stacking too many transistors between the supply rails is preferable for low-voltage operation [5]. In the comparator there is large voltage variations on the regeneration nodes which affects the input of the comparator through the parasitic capacitances of the transistors which is termed as kickback noise [4]. The settling time and accuracy of the decision significantly affect the performance of a comparator because of kickback noise [7]. In an ideal comparator, the offset voltage should be zero. In the practical comparators, input offset causes due to device mismatches or might be inherent in the design of the comparator [3].

Corners define differences due to process inaccuracies, temperature and with variation of the other parameters of MOSFET's. The simulations which takes such process variations into consideration will differ one from another. Corners in model library may describe differences due to process inaccuracies (such as variation in doping) which are

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supplied with the process kit and usually are located in models library [8]. For example the kit can include corners like fast NMOS fast PMOS, slow NMOS slow PMOS, fast NMOS slow PMOS, slow NMOS fast PMOS, typical NMOS typical PMOS. Each technology corner is different than others containing different temperature and may contain one value for every other parameter. During corner simulation all available corners are simulated and by performing such simulations we can check the influence of parameter variations on IC.

In this paper, a slight modification is done by some means of clock gating technique to reduce the dynamic power of comparator profoundly. Also the power analysis is done at various process corners.

II. CLOCKED COMPARATOR

Clocked comparators uses clock cycles for its operation. This clock can be divided into two phases which are:
1. Reset Phase and
2. Comparison Phase

This type of comparators uses positive feedback based back-to-back latch stage that determines output of the circuit. By using clocked comparator higher accuracy & lower power can be achieved. A clocked comparator structure which is also called as a latched comparator. Often latched comparators uses strong positive feedback with a regeneration phase when a clock is high and a reset phase when the clock is low.

The performance of comparator compared on the basis of parameters such as noise, kickback noise, random decision errors and offset.

A. *Proposed Double-Tail Dynamic comparator :*

The drawback of the conventional comparator is there is that only one current path that defines current for both the cross coupled latch and differential amplifier. But the Ntail1 operates mostly in triode region depend on common mode voltage which is not favorable for regeneration. In the proposed comparator the voltage difference at the first stage outputs (fn and fp) at initial time is increased so as the latch regeneration speed should be increased [1]. This proposed dynamic comparator increases the speed of the double-tail comparator by altering two important factors like the first one is that it increases the initial output difference voltage (ΔV_0) at the starting of the regeneration and the second one is that the effective transconductace (g_{meff}) of the latch is increased.

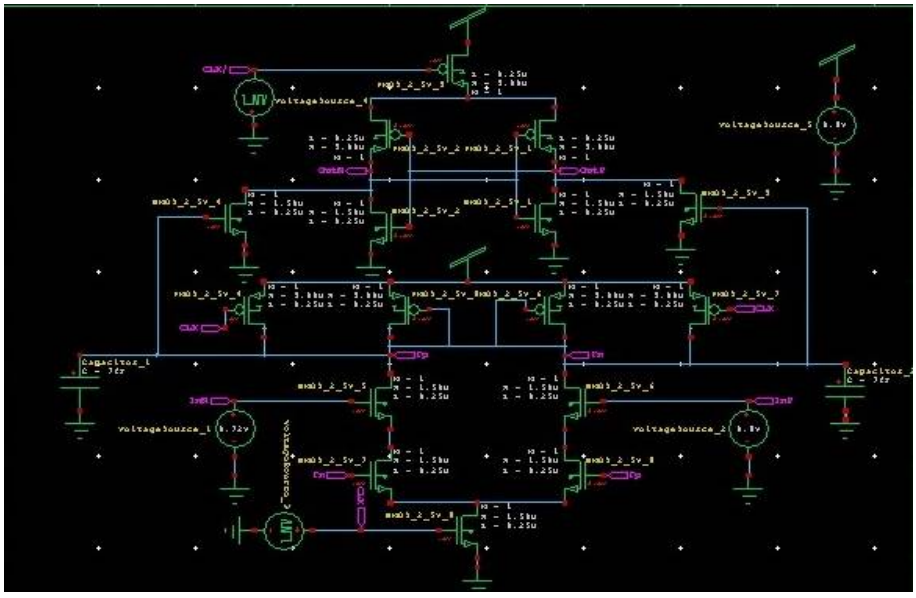

Fig. 1. Schematic diagram of the proposed dynamic double-tail comparator.

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In the proposed double–tail dynamic comparator, only one node (fn or fp) gets charged during the reset phase. This makes the dynamic double-tail comparator operating at lower power operation.

The operation of the proposed comparator shown in Fig. 1 is as follows. When CLK = 0, in the reset phase, both the tail transistors Ntail1 and Ntail2 are in off to avoid static power dissipation. Transistor N3 and N4 are in on state. N3 and N4 pulls both fn and fp nodes to V_{DD}, hence transistor NC1 and NC2 are cut off.

The circuit has two intermediate stage transistors NR1 and NR2. These transistors reset both latch outputs to ground. When CLK = V_{DD}, both the tail transistors are on, N3 and N4 transistors are off. Suppose InP>InN, thus fn drops faster than fp, the corresponding PMOS control transistor (NC1 in this case) starts to turn on, pulling fp node back to the V_{DD}, so another control transistor remains off, allowing fn to be discharged completely. The circuit has two intermediate stage transistors NR1 and NR2. These transistors reset both latch outputs to ground. When CLK = V_{DD}, both the tail transistors are on, N3 and N4 transistors are off. Suppose InP>InN, thus fn drops faster than fp, the corresponding PMOS control transistor (NC1 in this case) starts to turn on, pulling fp node back to the V_{DD}, so another control transistor remains off, allowing fn to be discharged completely.

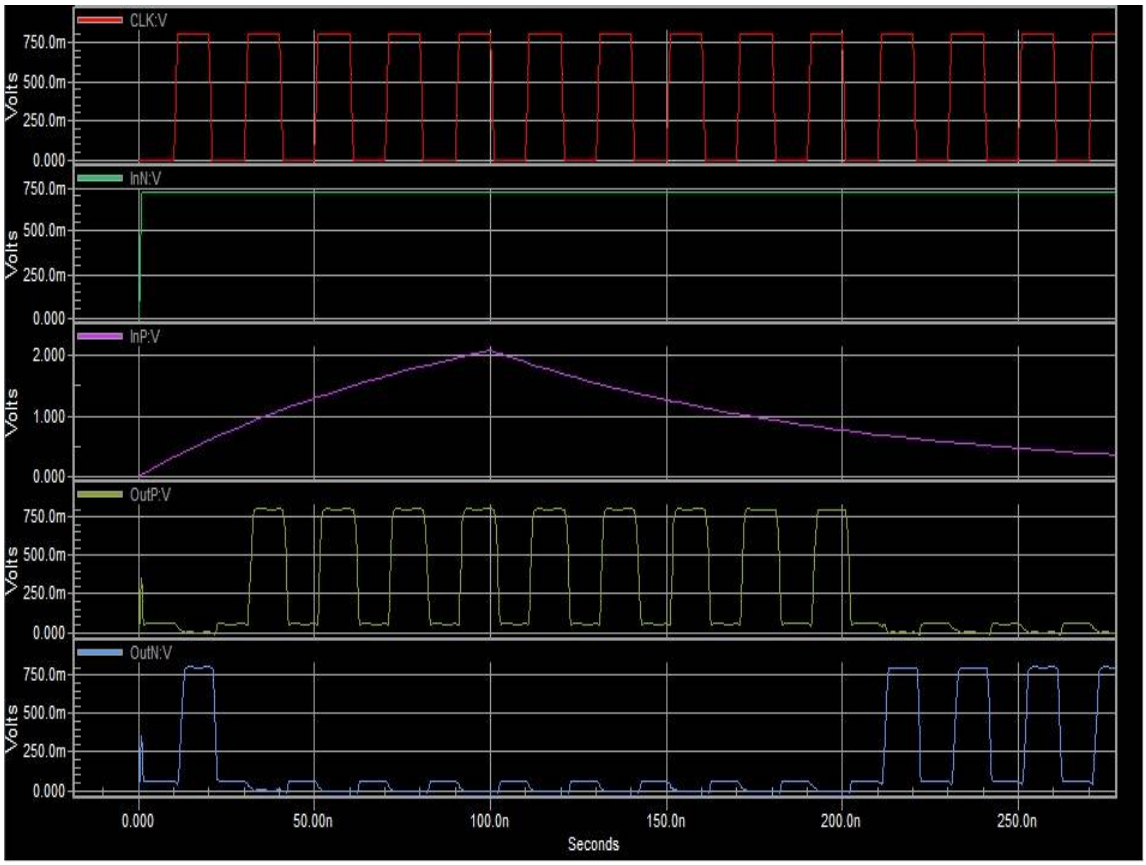

Fig. 2. Transient simulations of the proposed double-tail dynamic comparator forV_{DD}=0.8V.

B. *Modified Clock Gated Dynamic Double-Tail Comparator:*

The operation of the modified clock gated double-tale comparator is same as proposed comparator instead of adding a clocked gating technique. Nowadays in VLSI design power reduction is becoming the first consideration. Clock gating technique is used effectively in many modern VLSI designs so as to minimize the power dissipation.

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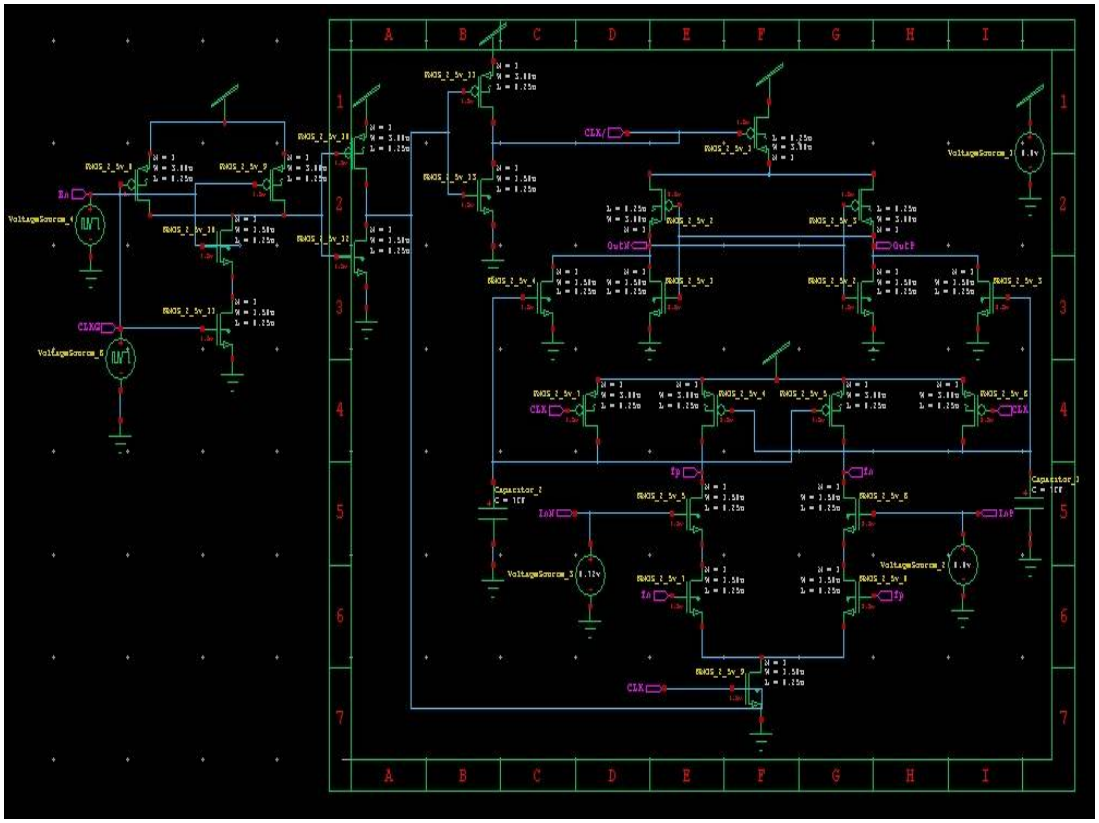

Fig. 3. Schematic diagram of the modified clock gated double-tail comparator.

Nowadays power has become a main consideration during hardware design and software design. Dynamic power can be used to save up to 40 to 60% of the total powerdissipation. Clock Gating mostly used in design methods to save dynamic and leakage power respectively. Various types of synchronous circuits uses clock gating techniques for reducing dynamic power dissipation. Clock gating technique can be used significantly to save the power by adding more gates to a circuit to reduce the power consumption.

By disabling the clock, it disables portions of the circuitry so that the transistors do not have to switch states. A NOR gate can be used as a clock gating technique to reduce the power and delay effectively [6]. AND gate is very suitable for clock gating, it performs on the positive edge of global clock and it works by taking the enable conditions. Fig. 3 shows the modified comparator it works similar as proposed comparator. Therefore it is an imperative design must contain these enable conditions in order to get benefit from clock gating. This clock gating process can save significant die area and power since it removes large numbers of unwanted noise and replaces them by clock gating logic.

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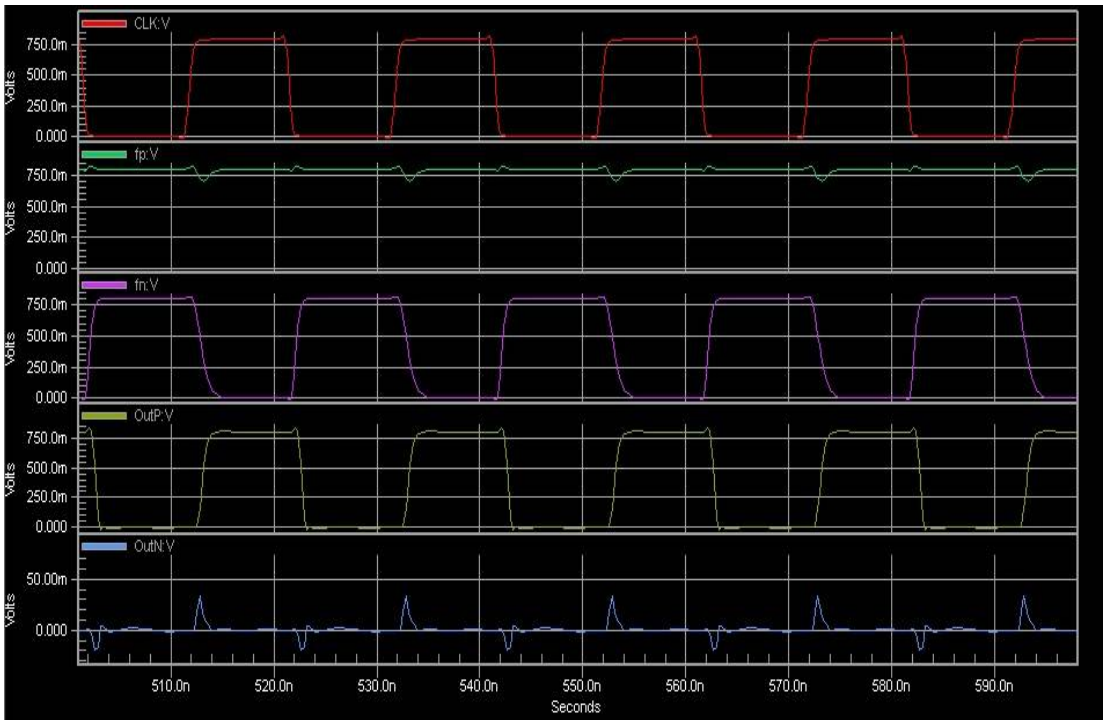

Fig. 4. Transient simulations of the modified clock gated double-tail dynamic comparator for V_{DD}=0.8V.

III. RESULTS

Tanner Tool V15.0 (Pre-layout simulation) is used for simulation. To compare the modified comparator with the double-tail and proposed double-tail comparators. All circuits have been simulated in a 0.18µm CMOS technology with V_{DD} = 0.8V. With decreased supply voltage, structures start to behave differently. It is important to perform corner analysis simulations, because if a design meets all requirements for all technology corners available in the kit during simulation stage, the likelihood that all requirements will be met during chip test increases.

Figure 5 and 6 shows the power variation along with different process variation at different supply voltages for the dynamic double-tail comparator and modified double-tail comparator circuit. The supply voltages of this comparator is varied from 0.8V to 1.2V. Input DC voltages are VInN=0.64V and VInP=0.8V with clock frequency of 45.45 MHz.

The validity of model at different corner processes is shown in table I and table II for dynamic double-tail comparator and for modified dynamic double-tail comparator where the model is valid at a different corner process if the power dissipation is within 10% of the typical corner.The simulations done above shows that the circuit may also suffer various types of process variation while fabrication or when subjected to various temperature and supply voltages. In such conditions the circuit must work properly, hence four corner analysis must be done before IC fabrication so that the device should not fail.

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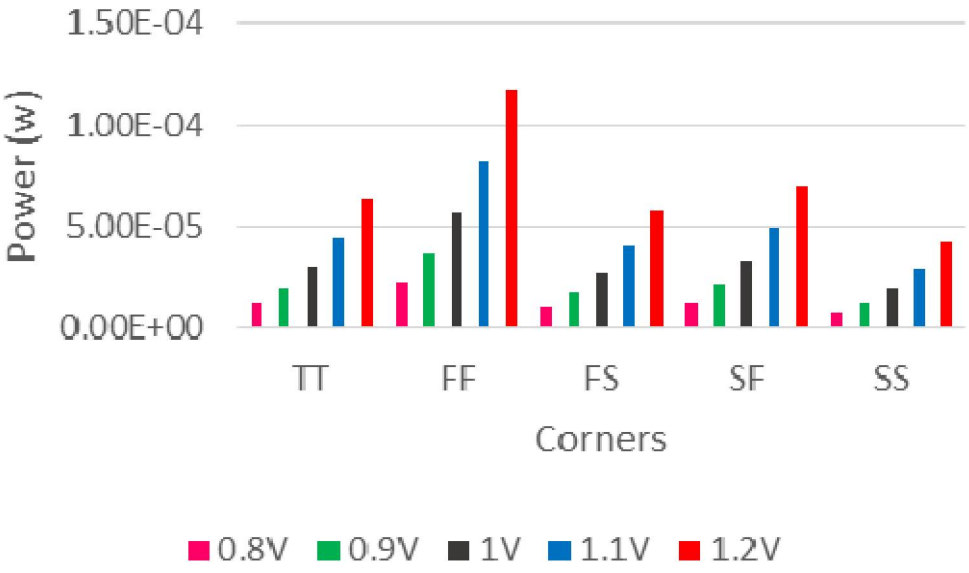

Fig.5.Power analysis at different process corners for proposed dynamic double-tail comparator

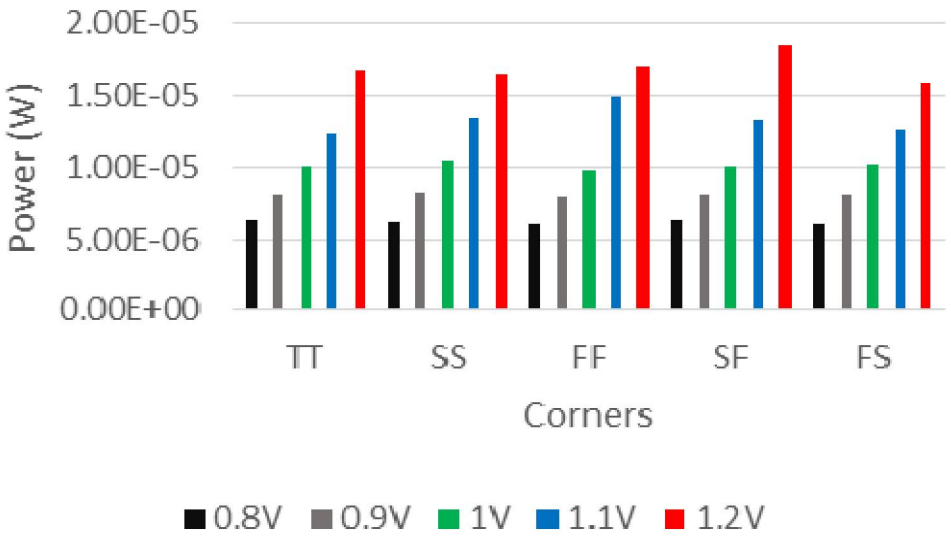

Fig.6. Power analysis at different process corners for Modified dynamic double-tail comparator

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Table I. Validity at different corners for Dynamic double-tail comparator

Corners	VDD				
	0.8V	0.9V	1V	1.1V	1.2V
TT	valid	valid	valid	valid	valid
FF	Invalid	Invalid	Invalid	Invalid	Invalid
FS	Valid	Valid	Valid	Valid	Valid
SF	Valid	Valid	Valid	Valid	Invalid
SS	Invalid	Invalid	Invalid	Invalid	Invalid

Table II. Validity at different corners for Modified Dynamic double-tail comparator

Corners	VDD				
	0.8V	0.9V	1V	1.1V	1.2V
TT	Valid	Valid	Valid	Valid	Valid
FF	Valid	Valid	Valid	Invalid	Valid
FS	Valid	Valid	Valid	Valid	Valid
SF	Valid	Valid	Valid	Valid	Invalid
SS	Valid	Valid	Valid	Valid	Valid

IV. CONCLUSION

The performance of the modified clock gated comparator and proposed double tail comparator comparators in terms of power have been compared. The pre-layout simulation using 0.18 µm technology shows that the modified clock gated comparator is valid at maximum process corners than the proposed dynamic double-tail comparator because of lower dynamic power dissipation.

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