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Design a High Speed 16x16 CMOS Vedic Multiplier, For Different Configuration

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ABSTRACT: we design a high speed 16x16 CMOS Vedic multiplier, for different configuration. All simulation is done on tanner EDA TOOL 13.00 software. Urdhva tiryakbhyam Sutra is most efficient Sutra (Algorithm) for high speed multiplication, and less number of transistor count. An adiabatic logic is used to design 16X16 CMOS Vedic multiplier. Multiplication is one of the basic operations for any high speed digital logic system design, digital signal processors or communication system. Primary issues in design of multiplier are area, delay, and power dissipation. There are many algorithms like booth multiplier, array multiplier, vedic multiplier, compressor based Vedic multiplier for overcoming this problems.

We analyze delay and power of proposed 16x16 CMOS vedic multiplier. It is clear that delay is reduced $\approx 71.85\%$ and power is also reduced $\approx 68.79\%$ as compared to existing vedic multiplier. 20479 transistors is used for the design of this vedic multiplier.

I. INTRODUCTION

The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications [2]. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications **.** This work presents different multiplier architectures. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier**.**

II. BASIC OF VEDIC MULTILPLIER AND ALGORITHM

The early Indian mathematicians of the Indus Valley Civilization used a variety of spontaneous tricks perform multiplication. Most calculations were performed on small slate hand tablets, using chalk tables. One technique was of lattice multiplication. Here a table was drawn up with the rows and columns labeled by the multiplicands. Each box of the table is divided diagonally into two, as a triangular lattice. The entries of the table held the partial products, written as decimal numbers. The product could then be formed by summing down the diagonals of the lattice. This is shown below:

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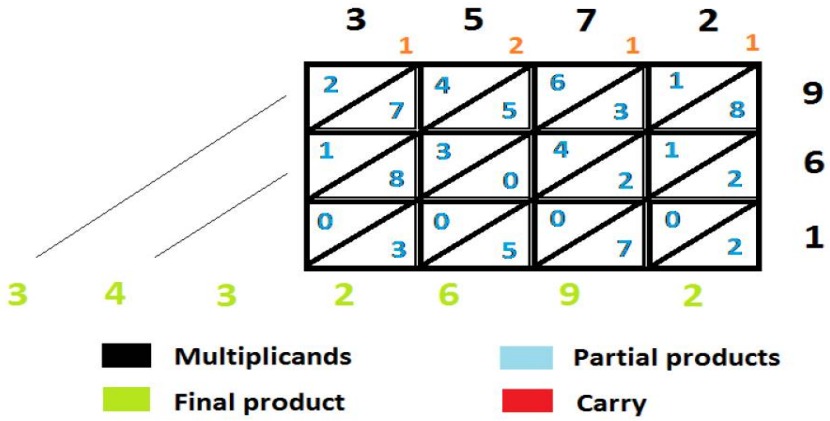

Figure : Example of Early Mathematician Technique

VEDIC MULTIPLICATION

The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutras). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. Vedic multiplication based on some algorithms, some are discussed below:

URDHVA TIRYAKBHYAM SUTRA

The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means “Vertically and crosswise”. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryakbhyam explained in fig 2.1. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. It is demonstrated that this architecture is quite efficient in terms of silicon area/speed [10, 4].

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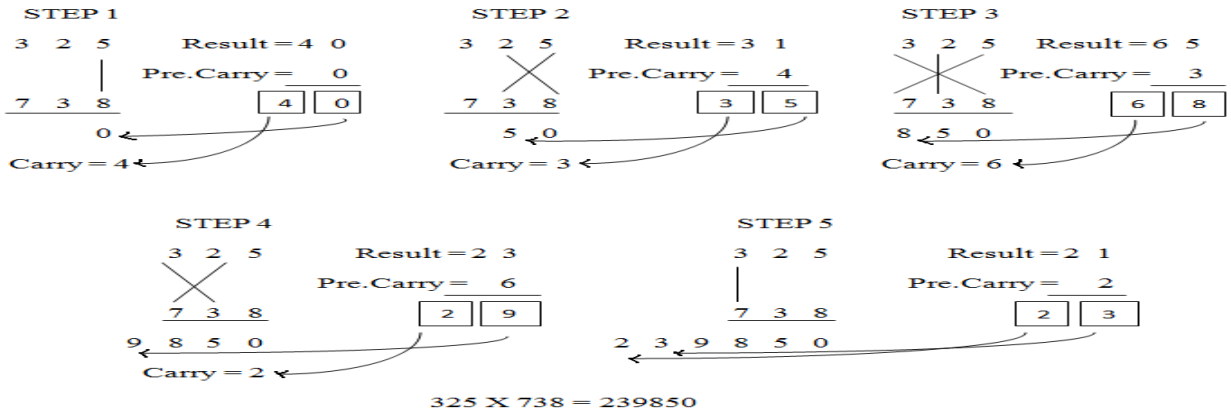

Figure 1.1: Multiplication of two decimal numbers by Urdhva Tiryakbhyam.

III. DESIGN AND IMPLEMENTATION OF VEDIC MULTIPLIER

BLOCK DESIGN OF 4X4 BITS VEDIC MULTIPLIER

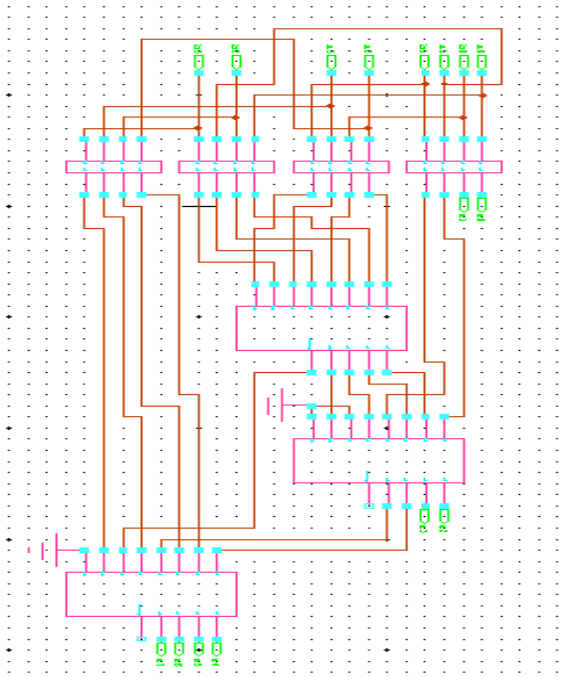

Figure 1.2: Circuit Diagram of 4x4 Bit Vedic Multiplier

Let's analyze 4x4 multiplications, say A3A2A1A0 and B3B2B1B0. Following are the output line for the multiplication result, Q7Q6Q5Q4Q3Q2Q1Q0. Block diagram of 4x4 Vedic Multiplier is given in fig 4.1.1.

IV. RESULTS AND ANALYSIS OF CIRCUIT

Simulation result and analysis of individual component used to design vedic multiplier is discussed below. Vedic multiplier is designed by means of 180nm CMOS technology.

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1.6 SIMULATION RESULTS OF 4X4 VEDIC MULTIPLIER

When the given input bit A=a3a2a1a0 & B=b3b2b1b0 then s = s7s6s5s4s3s2s1s0
A=15(1111)
B=15(1111)
Then output its S = 225 (11100001)
which is shown in given below:

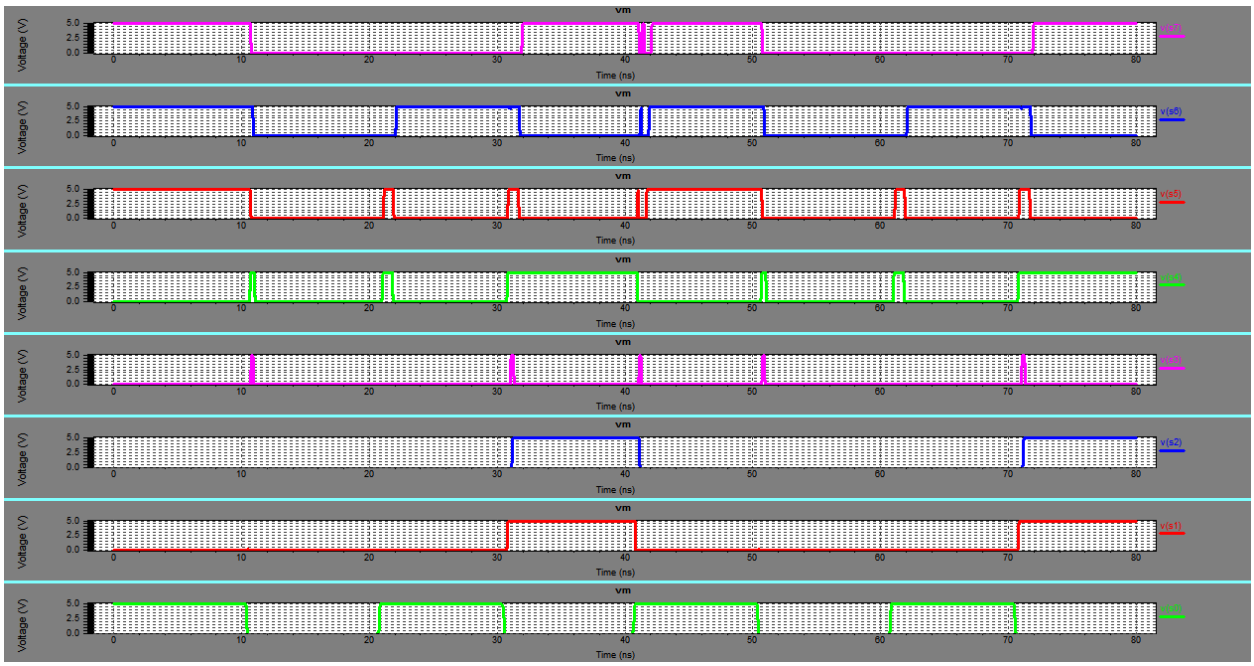

Fig 1.3: Output waveform of 4x4 vbedic multiplier

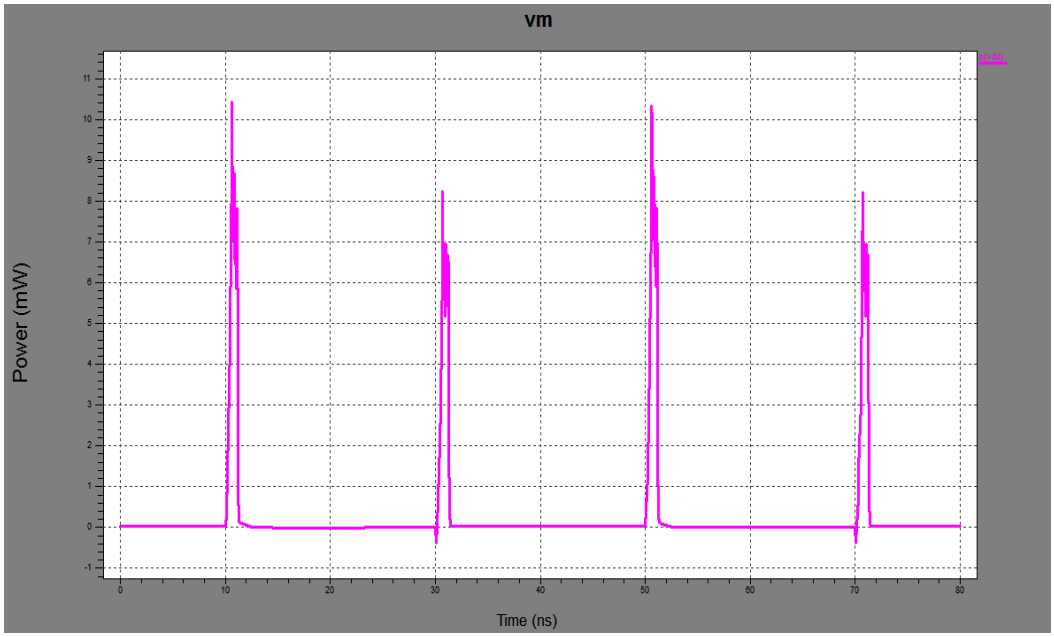

Fig 1.4 :Output Power of 4x4 vedic multiplier

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Table: Delay and power dissipation of 4x4 Vedic Multiplier

S. No.	V_{dd}(V)	Delay (ns)	Power (mW)
1.	1.8	1.19540	0.902
2.	2	0.10822	1.196
3.	3	0.16967	2.719
4.	4	0.12587	5.645
5.	5	0.12119	6.420

V. CONCLUSION AND FUTURE WORK

Conclusion

The design of 16x16 CMOS Vedic multiplier has been implemented on Tanner EDA tool 13.00v. The computation delay for 8x8 bits Vedic multiplier is 9.203 ns at 5V and for 16x16 CMOS Vedic multiplier is 20.856ns at 5V. Since power and delay of proposed Vedic multiplier is reduced as compared to existing multiplier. Thus, it is more efficient for fast multiplication.

Future Work

Vedic Mathematics, developed about 2500 years ago, gives us a clue of symmetric computation. Vedic mathematics deals with various topics of mathematics such as basic arithmetic, geometry, trigonometry, calculus etc. All these methods are very efficient as far as manual calculations are concerned. If all those methods effectively implement hardware, it will reduce the computational speed drastically. Therefore, it could be possible to implement a complete ALU using all these methods using Vedic mathematics methods. The future work is to designed 32x32 CMOS Vedic multiplier.

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