



International Journal of Innovative Research in Computer and Communication Engineering

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)





Standard Cell Design Using Cadence Virtuoso in GPDK 90nm CMOS Technology

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ABSTRACT: Standard cells are the fundamental building blocks of modern VLSI design, enabling efficient implementation of complex digital circuits. With continuous scaling of CMOS technology, designing optimized standard cells with reduced power consumption, improved speed, and minimal area has become essential. Here presents the design and implementation of standard cells using Cadence Virtuoso in GPDK 90nm CMOS technology. The proposed work includes schematic design, layout implementation, and verification using Design Rule Check (DRC) and Layout Versus Schematic (LVS). Various logic cells such as inverter, NAND, NOR, XOR, multiplexer, and sequential circuits are designed and analyzed. The performance of these cells is evaluated in terms of power, delay, and area. The results demonstrate that the designed standard cells meet design constraints and are suitable for scalable VLSI system design.

KEYWORDS: Standard Cells, CMOS, Cadence Virtuoso, GPDK 90nm, DRC, LVS, VLSI Design

I. INTRODUCTION

Integrated Circuits (ICs) are the basic building blocks of modern electronic systems and are widely used in devices such as smartphones, computers, and communication systems. With the advancement of technology, the number of transistors on a single chip has increased significantly, leading to the development of Very Large Scale Integration (VLSI). This allows designers to build complex and high-performance systems in a small area. However, as the complexity increases, designing circuits becomes more challenging and requires efficient design methods.

Complementary Metal Oxide Semiconductor (CMOS) technology is the most commonly used technology for digital circuit design because of its low power consumption, high speed, and reliability. CMOS circuits use both NMOS and PMOS transistors, which work together to reduce power loss. As technology scales down to smaller sizes like 90nm, designers face challenges such as increased power leakage, design complexity, and strict layout rules that must be followed to ensure proper circuit operation.

To simplify the design process, standard cells are used as basic building blocks for digital circuits. These include logic gates, multiplexers, and flip-flops, which are pre-designed and stored in a library. In this project, standard cells are designed using Cadence Virtuoso in GPDK 90nm technology. The design process includes schematic design, layout creation, and verification using Design Rule Check (DRC) and Layout Versus Schematic (LVS). The performance of the circuits is analyzed in terms of power and delay, and the developed cells can be used for building larger VLSI systems.

II. RELATED WORK

Previous research has focused on optimizing standard cell design for performance and area efficiency. Various techniques have been proposed for layout optimization and transistor sizing.

Traditional approaches involve manual layout design, which is time-consuming and prone to errors. Modern Electronic Design Automation (EDA) tools such as Cadence Virtuoso provide automated solutions for schematic design, simulation, and verification.



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Several works highlight the importance of DRC and LVS verification to ensure design correctness. The use of scalable design rules and advanced simulation tools improves the reliability of standard cell libraries.

III. METHODOLOGY

The methodology of this work focuses on the design and implementation of standard cells using Cadence Virtuoso in GPDK 90nm CMOS technology. The process begins with the schematic design of basic digital logic circuits such as inverter, NAND, NOR, XOR, multiplexer, and sequential elements. These circuits are designed using CMOS logic by properly connecting NMOS and PMOS transistors to achieve the required functionality. Proper transistor sizing is considered during this stage to balance power consumption and speed of operation.

After completing the schematic design, the next step is the layout design, where the physical representation of the circuit is created. The layout is designed by following lambda-based design rules and technology constraints to ensure manufacturability. Techniques such as stick diagrams and Euler paths are used to optimize the layout and reduce area. The layout includes proper placement of transistors, routing of interconnections, and alignment of different layers such as diffusion, polysilicon, and metal layers.

Once the layout is completed, verification is performed to ensure the correctness of the design. Design Rule Check (DRC) is used to verify that the layout follows all fabrication rules, while Layout Versus Schematic (LVS) ensures that the layout matches the original schematic design. After successful verification, simulation is carried out using the Spectre simulator to evaluate performance parameters such as propagation delay and power consumption. The results confirm that the designed standard cells are accurate, efficient, and suitable for use in larger VLSI system designs.

The “Cell-Aware” Design Flow

Our methodology deviates from standard student projects by adopting an **Industry-Standard Cell-Flow**:

1. **Netlist Architecture**: Define the logic function ($Y = \overline{A \cdot B}$).
2. **Transistor Sizing** (g_m/I_D): Use the constant current density method to size PMOS (W_p) vs NMOS (W_n) to achieve symmetric $V_m = 0.6V$ (for 1.2V supply).
3. **Euler Path Optimization**: Before drawing a single polygon, we graph the pull-up and pull-down networks.
 - *Step A*: Find a path that traverses every edge exactly once.
 - *Step B*: Ensure the order of inputs (e.g., A-B-C) is identical for both Logic Blocks to allow shared Poly gates.
4. **Layout Implementation**: Drawing N-Wells, Active regions, and Poly gates.
5. **Compaction**: Pushing rules to the DRC limit to minimize cell width.

90nm Process Specifics

- **Shallow Trench Isolation (STI)**: Unlike older LOCOS, 90nm uses STI. We calculate the “Stress Effect” of STI on the transistor mobility (μ).
- **Well Proximity Effect (WPE)**: Transistors placed closer to the N-Well edge have shifted thresholds. Our methodology mandates a $> 1\mu m$ buffer zone from the well edge

IV. EXPERIMENTAL RESULTS

The designed standard cells were successfully implemented and verified using Cadence tools.

- DRC results confirmed that all layouts are free from design rule violations.
- LVS results verified the correctness between schematic and layout.
- Simulation results showed acceptable propagation delay and power consumption.

Different logic cells such as inverter, NAND, NOR, XOR, multiplexer, full adder, and flip-flop were analyzed. The results indicate that the proposed design methodology produces efficient and reliable standard cells.



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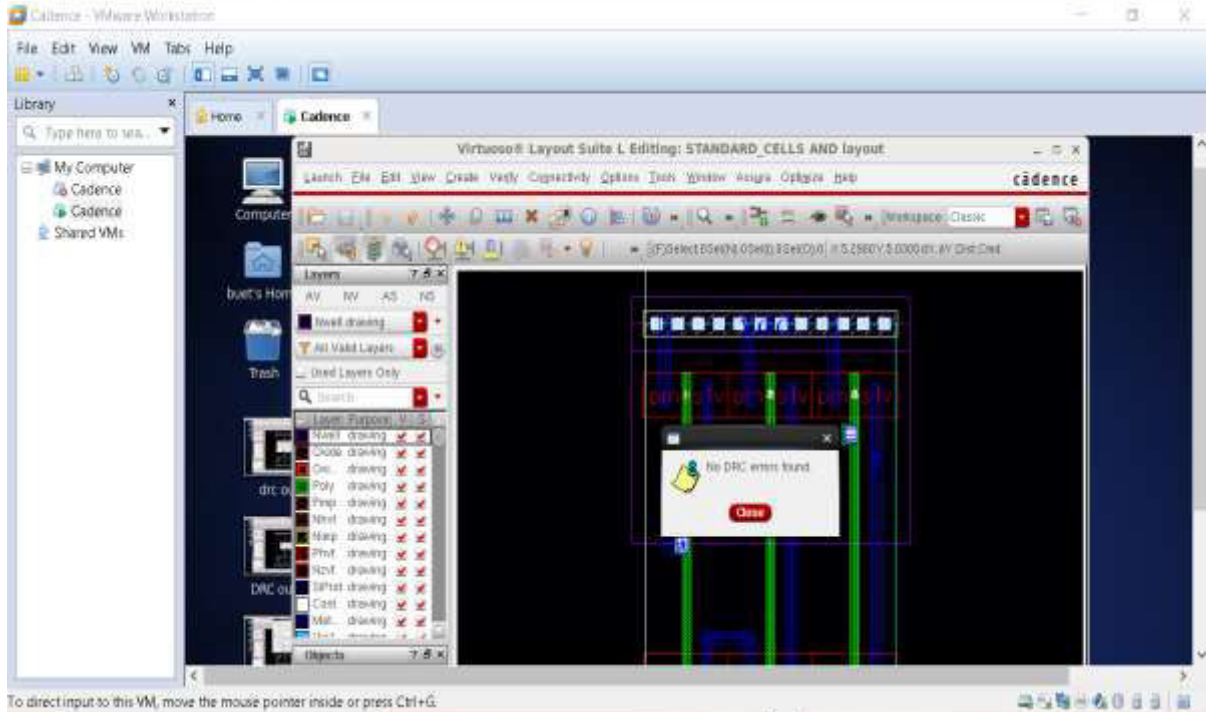


Fig 1 DRC Result

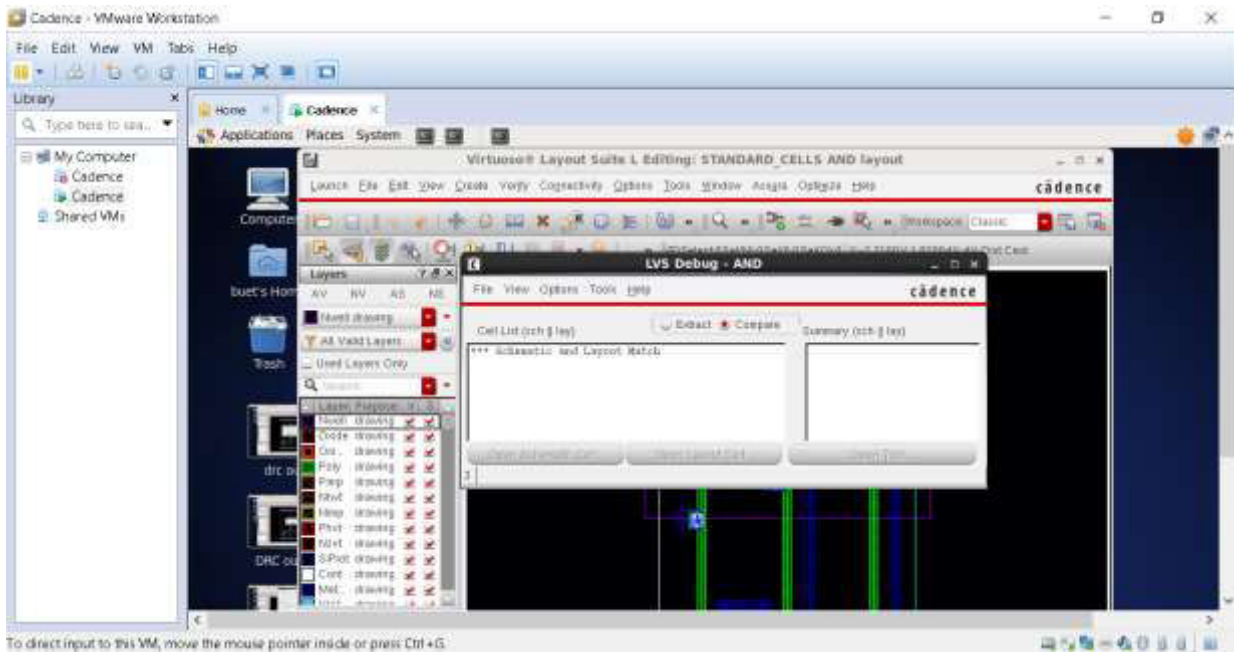


Fig 2 LVS AND



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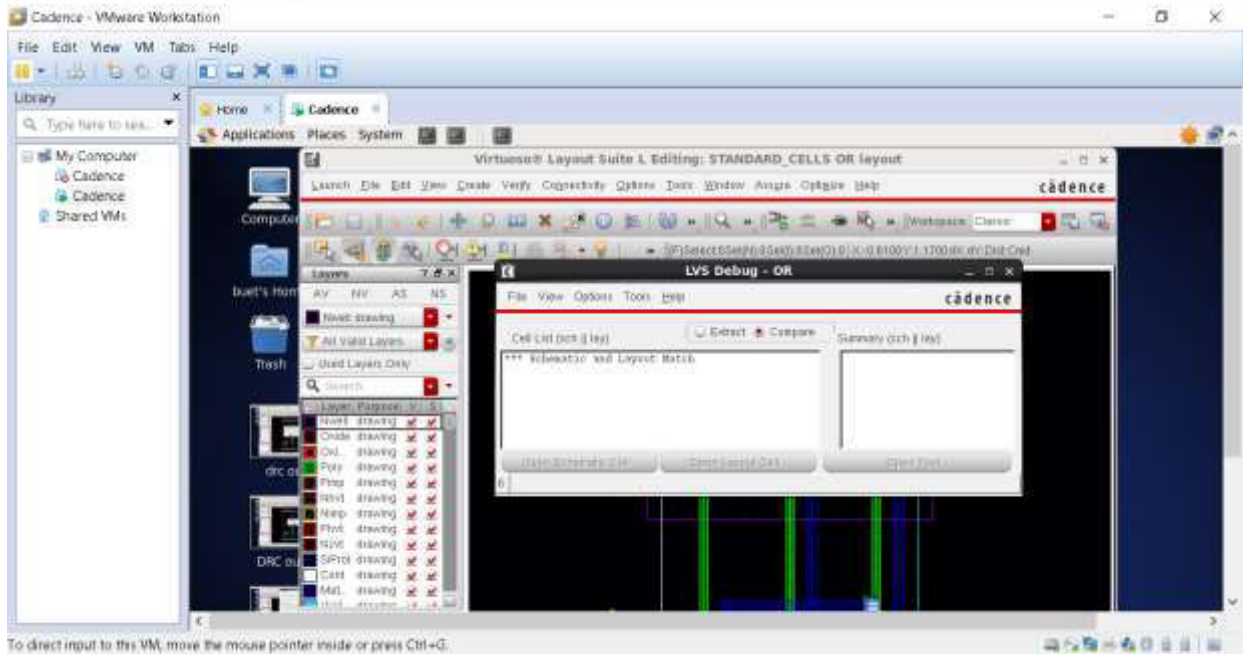


Fig 3 LVS OR



Fig 4 LVS NAND



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Fig 5 LVS NOR



Fig 6 LVS XNOR



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Fig 7 LVS XOR

V. CONCLUSION

In this paper, standard cells were successfully designed and implemented using Cadence Virtuoso in GPDK 90nm CMOS technology. Basic logic cells such as inverter, NAND, NOR, XOR, and other digital circuits were developed and verified. The layouts were checked using Design Rule Check (DRC) and validated through Layout Versus Schematic (LVS), ensuring correctness and reliability of the designs.

The performance analysis in terms of power consumption and propagation delay shows that the designed cells are efficient and suitable for VLSI applications. The developed standard cell library can be effectively used for building larger and more complex digital systems, making the design process faster and more reliable.

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