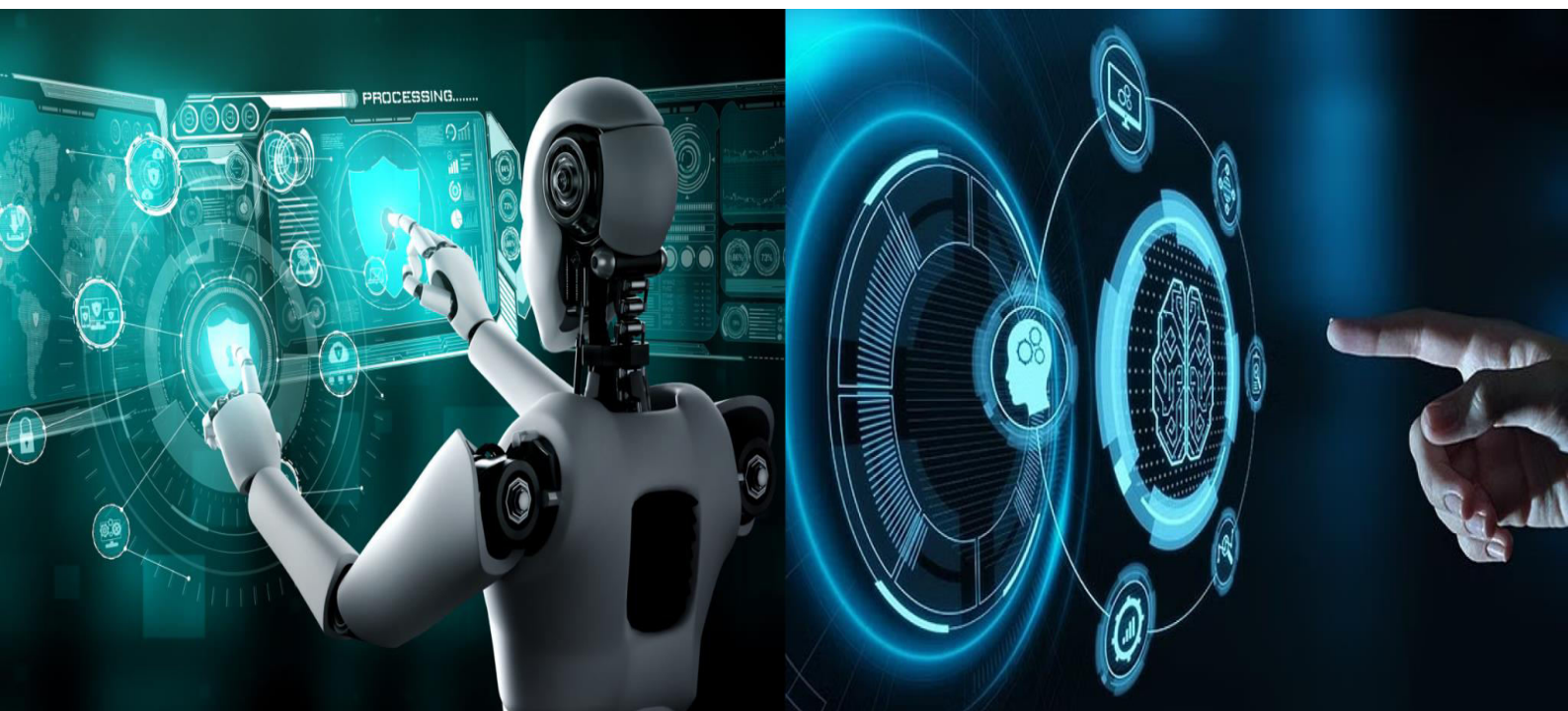


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Wide Load Range, High Current Accuracy Low Drop Out Regulator with Load Tracking Compensation and Dual Soft Start for Wireless Charging System

M. Sai Jyothi¹, K. Sai Rajesh², G. Srikanth³, B.T.S. Mani Deep⁴, N. Nagaraju⁵

U.G. Student, Department of ECE, SVIET Engineering College, Nandamuru, Pedana, Andhra Pradesh, India^{1,2,3,4}

Assistant Professor, Department of ECE, SVIET Engineering College, Nandamuru, Pedana, Andhra Pradesh, India⁵

ABSTRACT: This study introduces a High Voltage Low Dropout (LDO) regulator featuring a dual soft-start mechanism and load tracking compensation technique for Wireless Power Transfer (WPT) systems. The LDO design efficiently handles a broad input voltage spectrum from 5.15V to 20V and maintains stable performance under fluctuating load conditions ranging from 1mA to 1A. A notable advancement in this design is the dual soft-start mechanism, which enhances startup stability by separately regulating the pass transistor gate and the error amplifier input. Additionally, the load tracking compensation technique optimizes phase margin across diverse load currents, enhancing transient response and output stability. The regulator incorporates a current-sensing circuit for instantaneous overcurrent protection, accommodating load currents between 100mA and 1A. An integrated charge pump expands the error amplifier's operational range, allowing high-voltage compatibility while running on a 5V supply. Utilizing a BCD process, the proposed circuit delivers high power efficiency and robust performance within a compact layout measuring 0.8814 mm². These design features contribute to enhanced reliability and efficiency in WPT systems.

KEYWORDS: Low drop out regulator (LDO), load tracking compensation (LTC), dual soft-start, high accuracy current sensor, over current limit (OCL), WPT system.

I. INTRODUCTION

Wireless charging systems have emerged as a key enabling technology for modern portable electronics, electric vehicles, and biomedical devices, driving the need for highly efficient and robust power management circuits. Among these, low dropout (LDO) regulators play a critical role in providing clean, stable voltage supplies under varying load conditions.

This work focuses on the design of a wide load-range, high-current accuracy LDO regulator with load-tracking compensation and dual soft-start capability, implemented using 90 nm CMOS technology. The proposed regulator addresses the challenges of maintaining stability and fast transient response across a broad spectrum of load currents, which is essential in wireless power transfer environments where load conditions can change rapidly. The incorporation of load-tracking compensation enhances dynamic performance by adapting to varying output demands, while the dual soft-start mechanism effectively suppresses inrush current and minimizes voltage overshoot during startup and mode transitions. Leveraging the advantages of 90 nm technology, the design achieves improved integration, reduced power consumption, and enhanced performance, making it well-suited for compact and energy-efficient wireless charging applications.

II. RELATED WORK

Recent research on low-dropout (LDO) regulators has focused extensively on improving stability, transient response, and efficiency across wide load current ranges, which are critical requirements for wireless power transfer (WPT) systems. Conventional LDO designs rely on large off-chip capacitors and fixed compensation techniques, but these approaches suffer from limited adaptability under rapidly varying load conditions and increased area or cost. To



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overcome these issues, several works have introduced adaptive and dynamic compensation techniques, such as feedforward compensation, multi-zero pole tracking, and impedance-adaptive schemes, which enhance loop stability and transient response over a wide load range.

In particular, load tracking compensation has emerged as an effective method to dynamically adjust the frequency response of the regulator, thereby maintaining high loop gain and stability despite significant load variations, while also improving output accuracy and transient performance. Additionally, recent studies have explored capacitor-free and fast-response LDO architectures incorporating current tracking and class-AB error amplifiers to achieve high bandwidth and fast settling time without relying on bulky external components. For wireless charging applications, where input voltage and load current vary widely, advanced designs further integrate techniques such as dual soft-start mechanisms and current sensing to suppress inrush current, enhance startup reliability, and provide overcurrent protection. Despite these advancements, achieving high current accuracy, low dropout voltage, and stable operation simultaneously over a wide load range in scaled technologies like 90 nm CMOS remains a significant design challenge, motivating continued research in this area.

III. METHODOLOGY

The proposed MLDO itself is composed of several sub-blocks. The Error Amplifier (EA) with Load Tracking Compensation (LTC) forms the core of the control loop. The Dual Soft-Start Circuit manages the startup transient by separately controlling two voltage ramp paths. The Dual Path Charge Pump (CP) generates the elevated supply voltage required to drive the NMOS pass transistor gate. The Current Sensor with Overcurrent Limit (OCL) provides accurate current monitoring and protection. The Pass Transistor and Feedback Network complete the regulation loop.

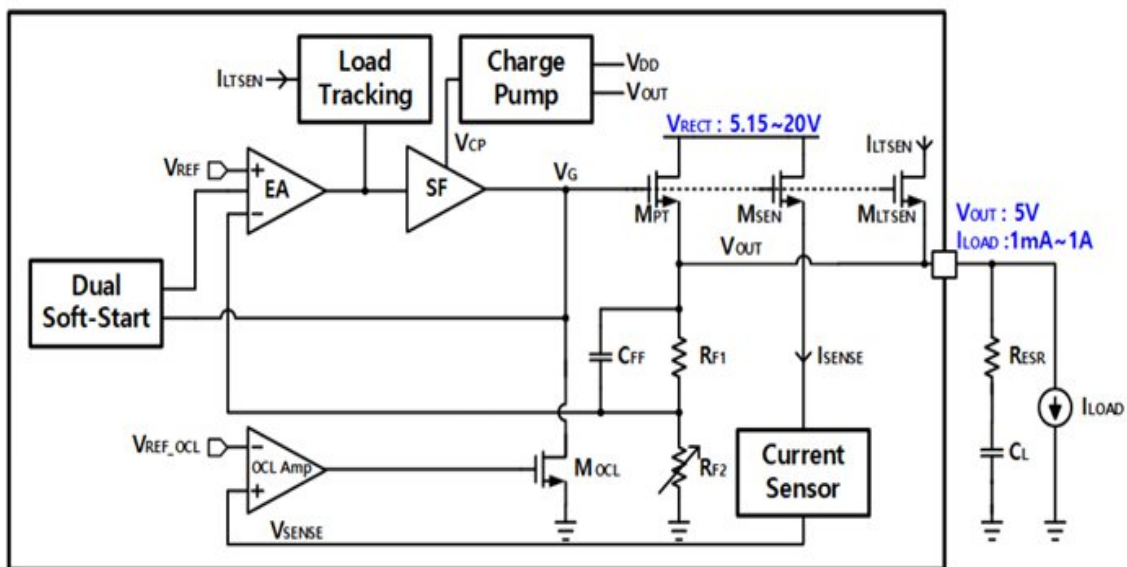


Fig.1 Block diagram of the LDO.

The proposed mldo system operates through a combination of control loops, sensing circuits, and power management blocks to ensure stable and efficient voltage regulation.

Nitially, a reference voltage (v_{ref}) is compared with the feedback output using an error amplifier (ea). The difference between these signals generates an error signal, which is used to control the system. A dual soft-start circuit is incorporated to gradually increase the output voltage during startup, reducing inrush current and preventing voltage overshoot.



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The error signal is then processed through load tracking and a charge pump. The charge pump generates a boosted voltage (v_{cp}) to properly drive the gate of the pass transistor (mp), ensuring efficient operation even at low input voltages. Load tracking dynamically adjusts the biasing based on load conditions to improve transient response.

The pass transistor (mp) acts as the main regulating element, controlling the output voltage (v_{out}). A current sensing circuit continuously monitors the load current (i_{load}) through a sense transistor ($msen$) and resistor network. This sensed current is fed back into the control loop to provide protection and maintain stability.

Additionally, a feedback network ($rf1$, $rf2$, and cff) is used to stabilize the system and improve transient response. The capacitor (cff) helps in compensating the loop and reducing voltage fluctuations.

The system also includes a current limit control loop, where the sensed current is compared with a reference (v_{ref_ocl}) using an operational amplifier. If the current exceeds safe limits, the system restricts the output to protect the circuit. Finally, the regulated output voltage ($v_{out} \approx 5v$) is supplied to the load, maintaining stability across a wide load range (1ma to 1a). The combination of charge pump, soft-start, current sensing, and feedback control ensures high efficiency, fast transient response, and reliable operation.

IV. EXPERIMENTAL RESULTS

With both DRC (No errors found) and LVS (Schematic and Layout Match) successfully passed, the physical design of the LDO Voltage Regulator is fully verified and ready for the next stage — parasitic extraction (PEX) and **post**-layout simulation.

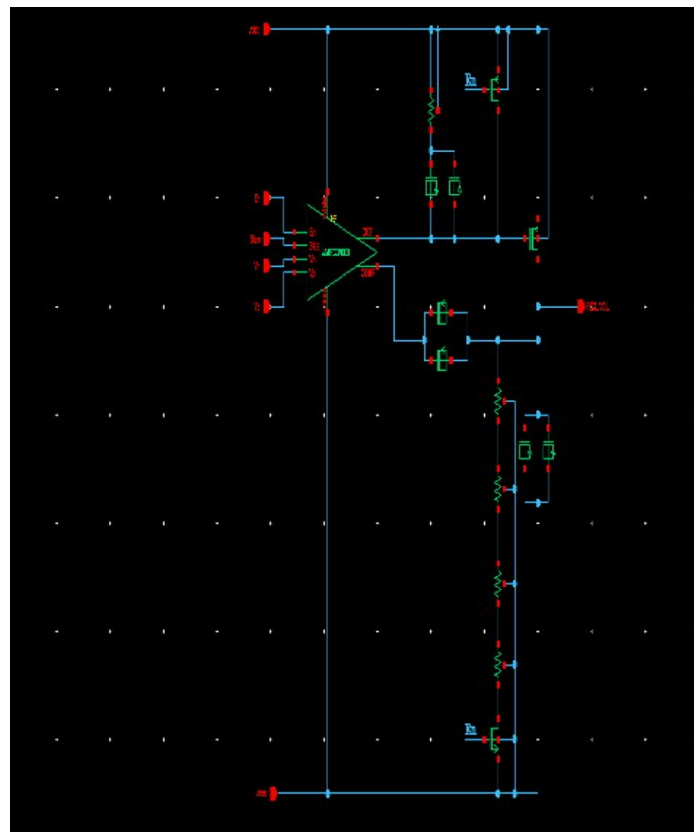


Fig 2 Schematic Design



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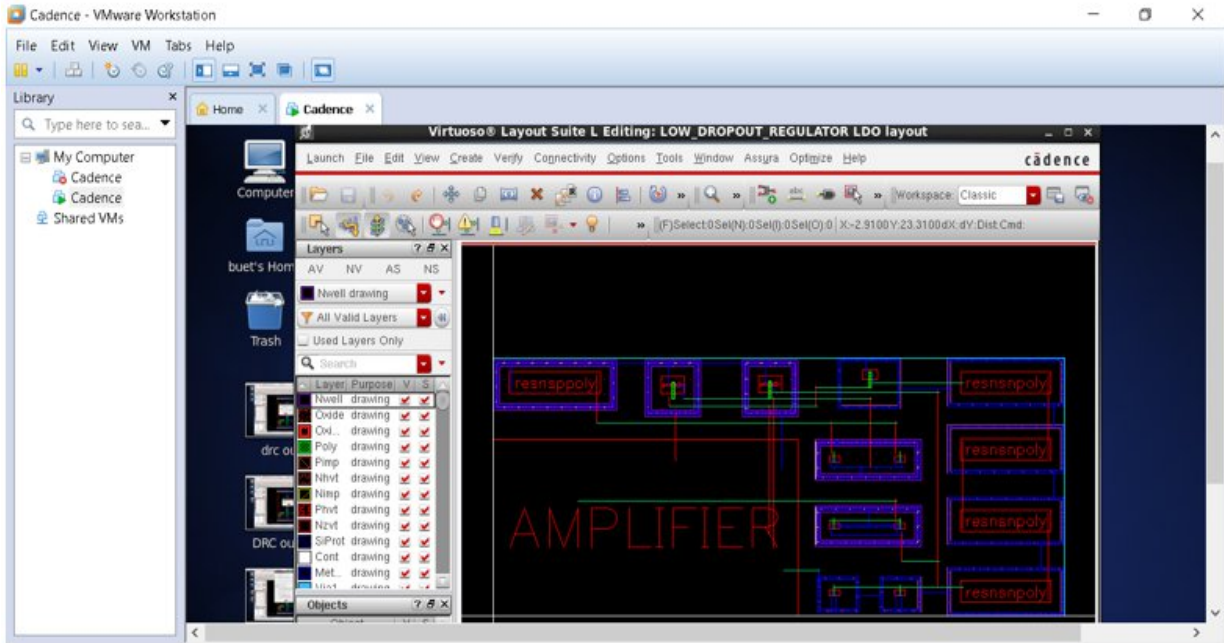


FIG3. LAYOUT OF LDO

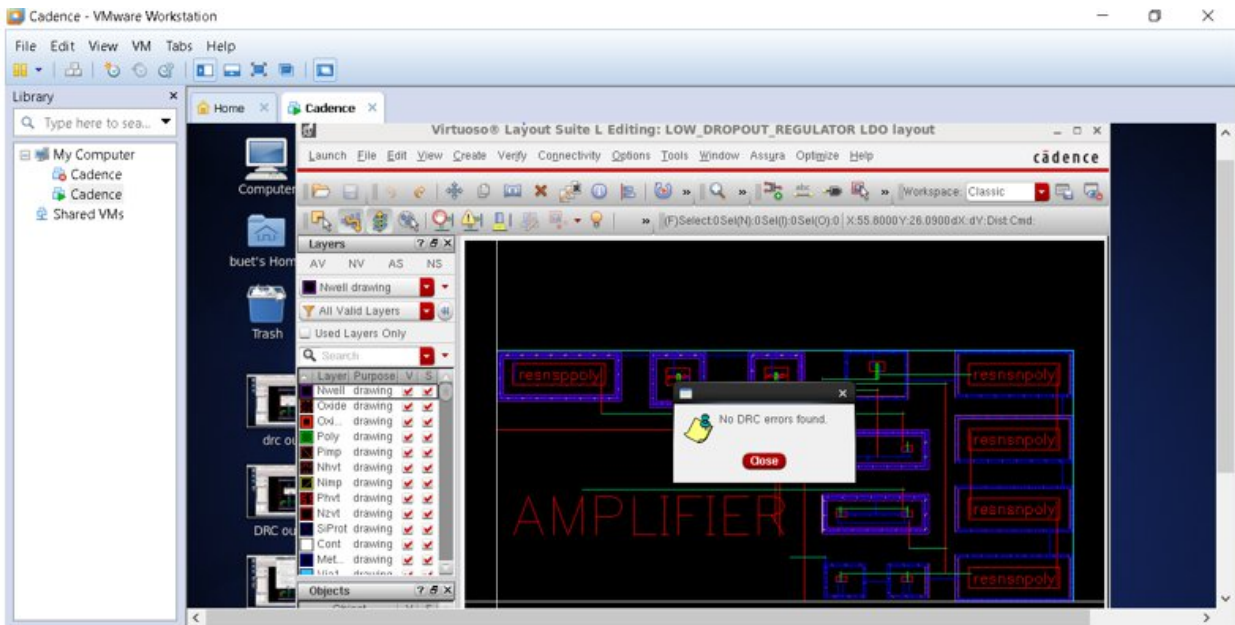


Fig 4.DRC output



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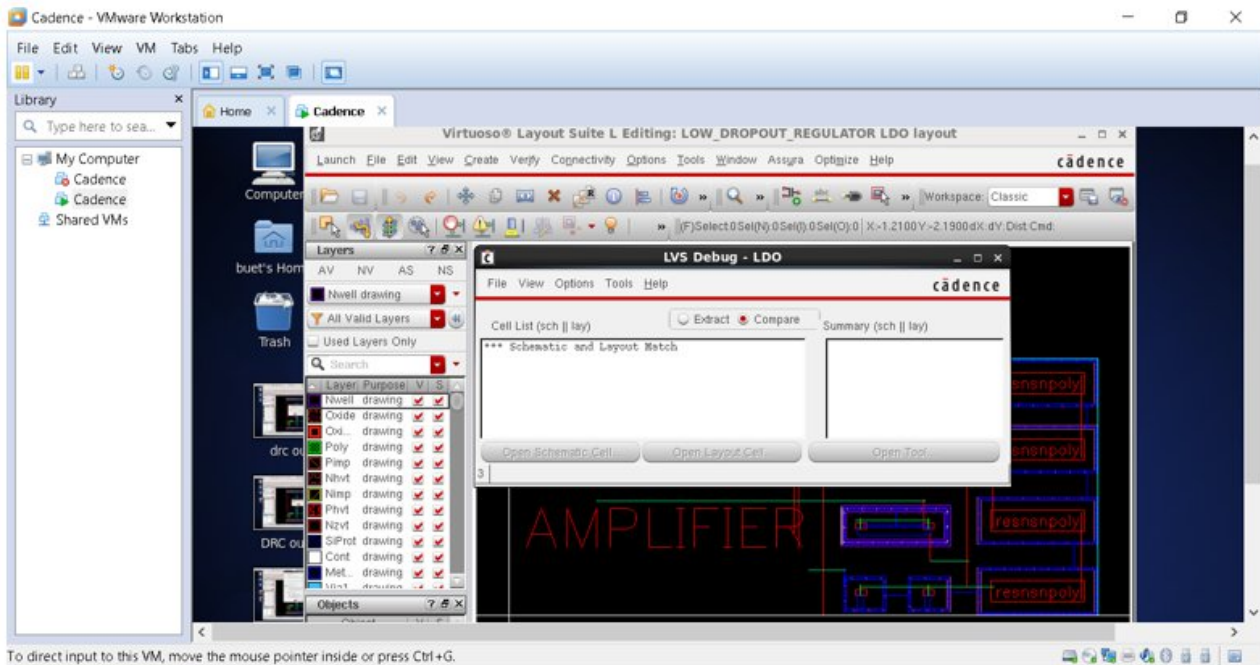


Fig5. LVS output

V. CONCLUSION

This project has presented a comprehensive design of a high-voltage low-dropout regulator tailored for wireless power transfer systems. The proposed LDO incorporates three key innovations that collectively address the limitations of existing designs.

Load Tracking Compensation (LTC) provides a dynamic zero that tracks load current variations, ensuring stable operation with a phase margin greater than 60° over a wide load range from 1mA to 1A, without requiring large on-chip capacitors. The dual soft-start mechanism, by separately controlling the gate voltage ramp and the error amplifier input ramp, reduces inrush current during startup by 74% (from 200mA to 27mA), protecting both the circuit and the load. The high-accuracy current sensor, using a replica MOSFET and a folded cascode amplifier, achieves greater than 90% accuracy across input voltages from 5.15V to 20V, enabling reliable overcurrent protection with programmable limits.

The LDO operates from a 5.15V to 20V input, delivers 5V at up to 1A, and occupies only 0.8814mm^2 in a $0.18\mu\text{m}$ BCD process implemented using GPDK 90nm technology in Cadence Virtuoso. Experimental results demonstrate excellent load regulation ($7.6\mu\text{V}/\text{mA}$), line regulation ($0.001\text{mV}/\text{V}$), and transient performance (undershoot 17mV, overshoot 15.8mV). The design achieves 99.99% current efficiency and compares favorably with prior works in terms of input range, area, and accuracy.

The proposed LDO is well-suited for integration into wireless charging receivers for IoT, medical, and portable devices, where wide input range, stability, and compact size are critical. Future work may extend the input range, reduce dropout, and explore digital control for enhanced adaptability. These research findings are expected to make significant contributions to various wireless power applications that require high-efficiency and high-reliability power management solutions.



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REFERENCES

1. B. Jang, A. Hejazi, R. E. Rad, Y. M. Qaragoez, I. Ali, Y. Pu, K. C. Hwang, Y. Yang, and K.-Y. Lee, "A 15-W triple-mode wireless power transmitting unit with high system efficiency using integrated power amplifier and DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9574–9585, Oct. 2021.
2. J. Tang, L. Zhao, and C. Huang, "A wireless hysteretic controlled wireless power transfer system with enhanced efficiency and dynamic response for bioimplants," *IEEE J. Solid-State Circuits*, vol. 58, no. 4, pp. 1160–1171, Apr. 2023.
3. T. Lu, K. A. A. Makinwa, and S. Du, "A single-stage dual-output regulating voltage doubler for wireless power transfer," *IEEE J. Solid-State Circuits*, vol. 59, no. 9, pp. 2922–2933, Sep. 2024.
4. F. U. Ahmed, Z. T. Sandhie, L. Ali, and M. H. Chowdhury, "A brief overview of on-chip voltage regulation in high-performance and high-density integrated circuits," *IEEE Access*, vol. 9, pp. 813–826, 2021.
5. D. Xu, Y. Zhang, X. Luo, Z. Li, and Q. Pan, "A 0.96–0.9-V fully integrated FVF LDO with two-stage cross-coupled error amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 10, pp. 3757–3761, Oct. 2023.
6. S.-W. Kwon, K.-I. Do, J.-M. Lee, U.-Y. Seo, and Y.-S. Koo, "Design of high-robustness LDO regulator with floating SCR based ESD protection circuit using high gain buffer," *IEEE Access*, vol. 12, pp. 33555–33568, 2024.
7. G. Li, H. Qian, J. Guo, B. Mo, Y. Lu, and D. Chen, "Dual active-feedback frequency compensation for output-capacitorless LDO with transient and stability enhancement in 65-nm CMOS," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 415–429, Jan. 2020.
8. X. Ming, J.-J. Kuang, X.-C. Gong, J. Zhang, Z. Wang, and B. Zhang, "An NMOS LDO with TM-MOS and dynamic clamp technique handling up to Sub-10- μ s short-period load transient," *IEEE J. Solid-State Circuits*, vol. 59, no. 2, pp. 583–594, Feb. 2024.
9. L. Huang, P. Luo, C. Wang, and X. Zhou, "A high speed on-chip soft-start technique with high start-up stability for current-mode DC-DC converter," *IEEE Access*, vol. 7, pp. 27579–27585, 2019.
10. M. Al-Shyoukh and H. Lee, "A compact ramp-based soft-start circuit for voltage regulators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 7, pp. 535–539, Jul. 2009.
11. J.-J. Chen, Y.-S. Hwang, J.-Y. Lin, and Y. Ku, "A dead-beat-controlled fast-transient-response buck converter with active pseudo-current-sensing techniques," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 8, pp. 1751–1759, Aug. 2019.
12. M. Doreyatim, M. Akbari, M. Nazari, and S. Mahani, "A low-voltage gain boosting-based current mirror with high input/output dynamic range," *Microelectron. J.*, vol. 90, pp. 88–95, Aug. 2019.
13. Y.-S. Hwang, J.-J. Chen, Y.-T. Ku, and J.-Y. Yang, "An improved optimum-damping current-mode buck converter with fast-transient response and small-transient voltage using new current sensing circuits," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9505–9514, Oct. 2021.
14. X. Lai, J. Zhao, and B. Wang, "A current-mode DC-DC buck converter with accurate current limit using multiplex PWM comparator," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12739–12749, Dec. 2022.
15. G. S. Kim, J. K. Park, G.-H. Ko, and D. Baek, "Capacitor-less low-dropout (LDO) regulator with 99.99% current efficiency using active feedforward and reverse nested Miller compensations," *IEEE Access*, vol. 7, pp. 98630–98638, 2019.
16. S.-K. Kao, J.-J. Chen, and C.-H. Liao, "A multipath output-capacitor-less LDO regulator," *IEEE Access*, vol. 10, pp. 27185–27196, 2022.
17. Y. Lu, T.-A. Yen, R. D. Nayak, S. Alevoor, B. Talele, S. Patil, K. Kunz, and B. Bakaloglu, "A novel parallel feed forward current ripple rejection (PFFCRR) technique for high load current high PSRR nMOS LDOs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 33, no. 3, pp. 651–661, Mar. 2025.



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