IJIRCCE

e-ISSN: 2320-9801 | p-ISSN: 2320-9798

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN COMPUTER & COMMUNICATION ENGINEERING

Volume 12, Issue 11, November 2024

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

Impact Factor: 8.625

© 2024 IJIRCCE | Volume 12, Issue 11, November 2024| DOI: 10.15680/IJIRCCE.2024.1211106

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.625| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

Comparative Analysis of 6T and 10T SRAM Cells using FINFET

[1]K. Phaneendra, [2]K. Chandhini, [3]K. Meghana, [4]M. Kishore, [5]Dr.Mohd Rizwan Uddin Shaikh

Students, Department of Electronics and Communication Engineering, GMR Institute of Technology, Rajam, A.P, India[1-4]

Assistant Professor, Department of Electronics and Communication Engineering, GMR Institute of Technology, Rajam, A.P, India[5]

ABSTARCT*:* SRAM technology is being gauged down to address challenges posed by advanced process variations and to enable ultra-low-power operation. presently, further than 80 percent of the face area in microdevices is devoted to memory factors. This trend isn't likely to drop, as the complexity of bias continues to increase over time. Traditional MOSFETs face several challenges, including high leakage current at lower process bumps. still, FinFET technology shows pledge as a good volition, offering bettered stability and reduced leakage at process bumps of 45nm and below. Memory cells represent the largest element of large- scale computing systems, with SRAM being the most generally used type of memory, enwrapping over 60 of chip area. A new design for SRAM cells at the 16nm knot, grounded on FinFET technology, has been proposed. This design demonstrates advancements in power consumption, leakage current, and detention, while also enhancing static noise periphery compared to conventional 6-transistor(6T) SRAM cells. The new 10- transistor(10T) SRAM design shows significant advancements in static noise periphery compared to contemporary models like 6T SRAM and earlier low- power SRAM designs. There are notable advancements in access time as well. When compared with MOSFET- grounded models, the power- detention product(PDP) during write mode is reduced by about 80.80, while in read mode, it's reduced by 50.65. also, the static noise periphery improves by 22.20, and leakage current reduction reaches a maximum value of 25.53(1). thus, this new design offers substantial earnings in both performance and energy effectiveness.

KEYWORDS*:* SRAM, FinFET, Power Consumption, Delay, Static Noise Margin (SNM), Sub-threshold Leakage Current (Ileakage)

I.INTRODUCTION

The operation of SRAM significantly influences the overall energy effectiveness of a device. In digital systems, the high- power consumption necessitates the optimization of power effectiveness, especially given the wide use of microelectronics in contemporary bias. The advanced characteristics of bias alongside reduced short- channel goods make FinFETs promising campaigners for low- power memory operations. These transistors are particularly well-suited for ultramodern memory designs(1).

This paper aims to design an SRAM cell using FinFET technology, fastening on low power consumption and functional effectiveness, especially in battery- operated bias. FinFETs offer lesser performance than conventional MOSFETs, and this paper addresses both power consumption and area effectiveness in being SRAM designs. It'll explore the design and development of a FinFET- grounded SRAM
cell, demonstrating the device armature and circuit design along with their simulation results. The ideal is to optimize design parameters for a largely effective low- power memory operation that makes effective use of area.
Although memory cells were firstly developed using CMOS technology, there are downsides associated with it, including subthreshold leakage current(I_leakage) and gate- convinced hedge lowering(GIBL). These issues complicate as knot sizes shrink. FinFETs present a feasible result to these challenges. While the short- channel range for CMOS bias reaches roughly 45 nm, FinFETs are completely functional at lower bumps, similar as 7 nm.

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.625| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

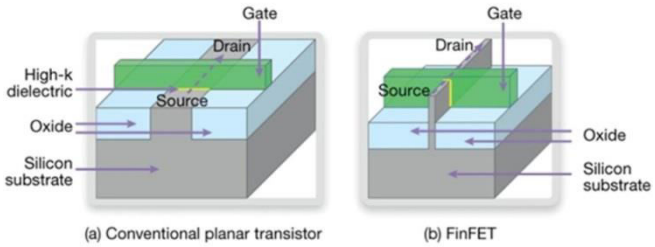
(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

As nano- scale technologies are decreasingly integrated into current device fabrication, customization is essential in memory device design. By replacing MOSFETs with FinFETs in the proposed memory cell, numerous conventional design issues can be resolved. also, the read- out path, threshold voltage, and mounding schemes of FinFET- grounded designs will further reduce leakage current, minimizing the threat of incorrect read operations(2).

II.METHODOLOGY

FINFET:

The FinFET is a 3D shape of the transistor wherein fins are protruding vertically that will be used as the source and the drain. That does not apply to planar MOSFETs for transistors larger than 45 nm. Instead, FinFETs will be applied on smaller transistors smaller than 45 nm because it has better controls over short-channel effects, off-state leakage current, power dissipation, and propagation delay. In this paper, a design of an SRAM cell with the aid of dual-gate FinFET transistors will be carried out. FinFET is based on the assertion of the research and possesses a better speed than the planar CMOS transistors, in spite of retaining improved current density. Thus, the device is at a relatively higher energy efficiency.



The existence of the second gate at the opposite end of the conventional gate enhances control in FinFET technology specifically in low-voltage operating modes. In order for a FinFET to operate, both gates must be driven simultaneously. In such an arrangement of a FinFET in which the gates are driven to the same voltage we refer to this as mode of operation called shorted gate (SG). If the gates of a FinFET are driven shorted we call it an SG FinFET. An independent-gate or IG FinFET is known to be a 4-terminal device in which the two gates are separated physically. IG FinFET is comparatively more versatile than the counterpart SG FinFET.

IG FinFET. This device operates on the principle that the two applied voltages of the gates differ. It is in this way how one creates a third control voltage for the amplitude of the transistor's threshold voltage and behaves like a switching element that may either be activated or inactivated. It can rather easily be visualized as the structure of the FinFET is of a 2D nature. The height of the fin is characterized by two major parameters that consist of the width of the fin (W) and the height (Hfin) of the fin. The quantization width for SG and also for IG FinFETs can be calculated by using the following expressions For SG FinFET, the width W is provided as

$$W_{SG} = 2 \times H_{fin} + T_{si},$$

Where Tsi is the silicon thickness.

The width for IG FinFET has been given as

$$W_{IG} = 2 \times H_{fin}.$$

Since the gate configuration of FinFETs is flexible, it suits the reduced process nodes and thus enhances electronic devices.

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.625| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

III.WORKING PRINCIPLE OF FINFET

Voltage Control: FinFETs are essentially identical to traditional MOSFETs. This is because the applied voltage at the gate determines what it will do, thus it will do similarly to that of a voltage-controlled device. In this manner, the conductivity of the channel implemented by the fins depends on the applied voltage. Therefore, the flow of currents can be controlled through variations in voltage.

Control: FinFET has a three-dimensional gate structure and thus it can control the channel from all the three sides, and with that very good electrostatic control over the channel can be achieved. This has significantly reduced leakage current and short-channel effects both of which were major problems identified with conventional planar MOSFETs[3].

Short-Channel Effects: If the channel length is reduced as much as possible in a standard MOSFET, then DIBL and leakage currents are significant problems. In the case of FinFETs, such degrading effects are suppressed due to the provision of longer effective gate area compared to channel length**.**
Improved Short-Channel Effects: The 3D structure improves the control offered by the gate, thus minimizing DIBL and current leakage issues. Lower Leakage Current: Electrostatic control is better, which in turn decreases leakage and hence efficiency of power consumption. Scalability: FinFETs are quite efficient even at very low nodes, i.e., greater than 45nm, with higher performance along with lesser power consumption than planar MOSFETs. Higher Current Drive: Current density in FinFETs is better; hence, the performance of high-speed applications boosts. Lesser Power Dissipation: Channel control is much better; thus, power dissipation is less. Choose Lower Voltages: Much better at lower voltages. This can be aptly useful for the power-sensitive circuits. Better Switching: The switching speed is much better in FinFETs and therefore, the overall performance of the device may be optimized.

SCEs in MOSFETs, for example, FinFETs SCEs, should also be taken into consideration at any scale of the channel length. Among the effects that include are: Gate-Induced Drain Leakage (GIDL): Because of the voltage field at the gate-source edge and across the drain, which makes it power-hungry, slow, and lower reliability. Drain-Induced Barrier Lowering (DIBL): The drain voltage field reduces the barrier between channel and source, thereby causing additional increase in leakage current and threshold voltage. This degrades performance.

SRAM

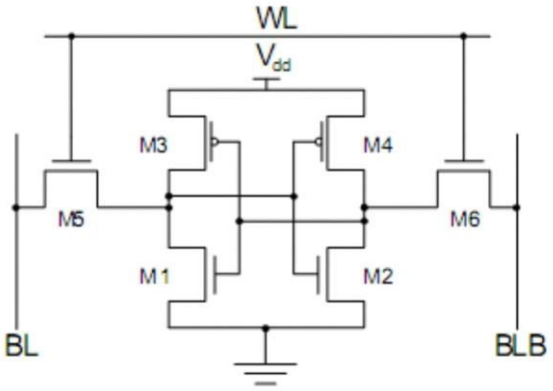
SRAM, or Static Random- Access Memory, is a type of changeable RAM. This means that the information stored in SRAM is lost when power is cut off. Compared to DRAM(Dynamic Random- Access Memory), SRAM is hastily but tends to be more precious due to its larger silicon area, which presently occupies about 94 of System on Chip(SoC) circuit area in modern designs. In moment's VLSI(truly Large- Scale Integration) systems, memory is constantly partitioned, with semiconductor remembrances serving as fundamental structure blocks for the architecture.
One key difference between SRAM and DRAM is that SRAM doesn't bear frequent stimulating; it maintains stored charge naturally over time. In distinction, DRAM must be refreshed continuously, leading to lower frequent operation of DRAM in certain operations(2).

Recent advancements in SRAM cell designs aim to enhance stability and reduce power consumption. Despite these inventions, the standard 6T SRAM cell remains current due to its conciseness and simplicity, although it faces limitations with stability during read and write operations, especially at ultra-low voltage situations.
Down from issues related to speed and power consumption, necessary configurations of SRAM, analogous as 7T, 8T, and 9T cells, have been proposed, fastening on advancements to the stationary Noise fringe(SNM) to achieve further low- power performance(3). 6T CONVENTIONAL SRAM

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.625| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)



The most commonly used memory cell structure in digital designs is the 6T Conventional SRAM cell. It is called "6T" because it consists of six transistors that store one bit of data. A general model of a 6T SRAM can be viewed as a latch made up of two cross-coupled inverters and two access transistors, which control the read and write operations[2].

Cross-Coupled Inverters:
A latch comprises two PMOS (positive-channel metal-oxide-semiconductor) transistors and two NMOS (negative-channel metal-oxide-semiconductor) transistors to store the bit of data. When the value of the bit continuously feeds back, maintaining either a 0 or a 1, the two inverters create a stable feedback loop.

Access Transistors:
The two additional NMOS transistors connect to the bit lines, labeled BL and BL-bar. These transistors enable data to be read from or written into the cell. The access transistors are controlled by the word line (WL). When the word line is set high, the access transistors turn on, allowing the data stored in the cell to be read or modified.

Read Operation:
In the read operation of an SRAM, the word line (WL) is set to Vdd, and the memory retains Q = 1 and Qb = 0. The bit lines are pre charged to the potential Vdd. Initially, there is no need for a potential drop since Qb is at 0 while the bit line BLB has a potential. As a result, there will be a discharge and current flow in the circuit. The sensing amplifier is connected to the bit lines and is tasked with detecting the voltage difference. In this scenario, since the potential on BLB will be lower, the amplifier will output a value of 1. Conversely, if Q = 0 and Qb = 1, the specified potential difference will cause a discharge in the bit line, leading to a change at the Q node. The memory cell ratios must ensure that Q falls within the "P2 zone," or read limit, for the operation to be successful. If Q = 0, the output will be 0, confirming that the read operation is successful in either case.

Write Operation
For the write operation, Vdd is applied, and BL is discharged to ground while writing a '0'. The word line is set high at this time to facilitate the writing process into the SRAM cell. In memory bits with Q = 0 and Qb = 1, two input lines are utilized for the write operation at bit-lines BL and BLB. The process begins by pulling BLB to ground, creating a significant potential difference between Qb and BLB. We ensure that the device ratios are set such that the pass transistors are stronger than the PMOS transistors, allowing Q to be set to 1, which is our goal when writing a '1' into the SRAM cell. Once this is accomplished, Q becomes 1, indicating that the write operation was successful.

Hold Operation
In the hold state, the word line is connected to the ground, which forces the access transistors M5 and M6 to turn off. This isolation keeps nodes Q and Qb disconnected from the bit lines BL and BLB. The state of the SRAM cell is maintained thanks to the cross-coupled inverters M1, M2, M3, and M4. This negative feedback between the two

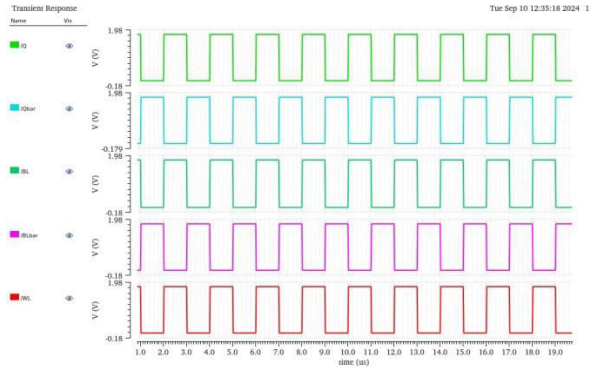
www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.625| ESTD Year: 2013|

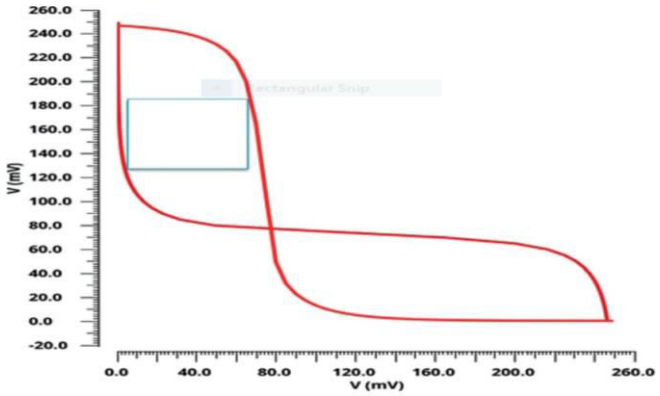
International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

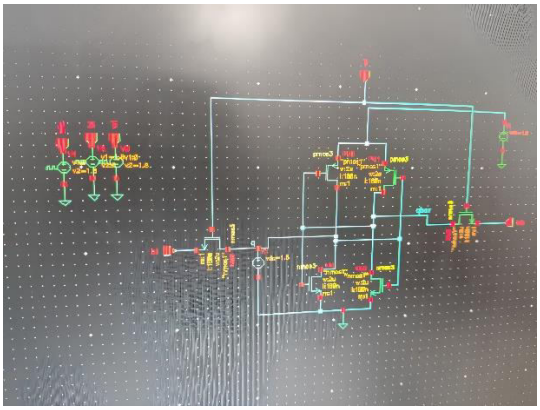
inverters ensures that Q remains high (1) while Qb is low (0), or vice versa, thus keeping the data stable. Although this SRAM cell can retain its state while powered by Vdd, it loses data once the power is cut off, as it is volatile.

Simulations:





SNM



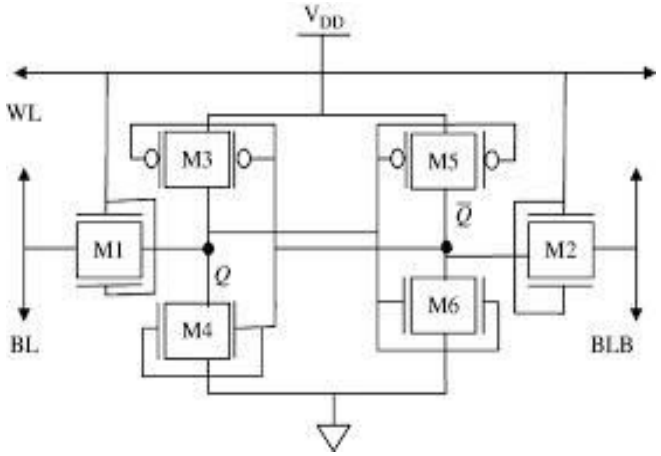
www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.625| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

10T SRAM CELL

Designed to be one of the most advanced SRAM cells, the 10T SRAM cell offers greater performance compared to that of the 6T SRAM cell. In addition to allowing increased stability, the device supports greater data retention for low power high-speed applications that require stronger read stability. The 10T SRAM cell has two cross-coupled inverters that comprise M1, M2 and M3, M4, as shown in Figure 1, in order to create a bistable latch for the data storage.[3] The cell has four access transistors-M5, M6, M7, and M8-designed into it for more effective control over read and write operations, leading to better isolation and stability during reads. It provides such benefits like reduced read disturbances, quicker access time, and superior control within the write margins. The SRAM 10T works very efficiently at lower supply voltages so that the leakage currents are reduced, with a reduction in power consumption, thus becoming the best energy-aware application[4]. The proper utilization of the additional transistors maximizes the access times by the individual control signals both for reading as well as writing. They generate less noise and are scaled more effectively at higher technology nodes[5]. They natively support newer technologies, including FinFET and SOI. Their architectures can be flexible enough to meet the specific requirements for speed, power, and area. In summary, 10T SRAM cells are far more advanced than 6T cells with better performance and reliability for today's high-performance applications.



It is the basic performance metrics in terms of an SRAM cell that can be used for high-speed memory systems and applications like cache memory. The access time is the time elapsed between reading or writing the data after the activation of the word line, and shorter times are critical for fast applications. Data integrity must be read and write stable. A read stability would mean that the value being stored is preserved whenever that value is read out. Write stability is thus the overhead of a write cycle, and it says how much the voltage can change without failing the write cycle. Another prime parameter of this memory is power consumption. This needs to be static, leakage current during a sleep or idle cycle, and dynamic, the power that is consumed by the circuit during the time of the read/write cycle.[6] Both static and dynamic power consumptions have to be minimized for energy efficient designs. Noise margin measures SRAM cell performance with noise tolerance for data not corrupted and a higher margin results in greater reliability. Area is the physical size of a cell. As the areas shrink, so there comes a possibility of greater memory density, which is yet another significant enabler for state-of-the-art circuits. Scalability will thus denote that with downscaled technology nodes, the cell should be able to sustain performance; thus it's crucial for future advancements in the semiconductor industry. The time the SRAM can retain data with no power supply applied is considered as retention time in the low-power operating modes. This refers to margins of write and read, voltage differences required for a surety of reliable write and read cycles so that the circuit sustains operational states even for a variety of conditions. Lastly, processor cache memory must be fast enough to work so that it can impose speed, including access time and operation.

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.625| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

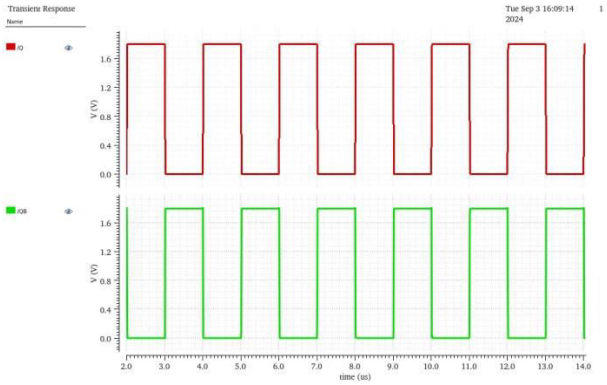


Figure 3- simulation result for 10T SRAM cell.

IV.RESULTS AND ANALYSIS

Performance Comparison Of 6T And 10T SRAM CELL in WRITE Mode.

SRAM(T)	Transistor	Power(nW)	Delay(ns)	PDP(nJ)	Percentage improvement
6	MOSFET	78.92	60.02	4736	68.58
	FINFET	24.53	60.69	1488	
10	MOSFET	70.46	44.69	3148	80.80
	FINFET	18.82	32.02	602	

SRAM Cell Level Performance Comparison: With the two types of transistors, MOSFET and FINFET comparing the two types of bit-cells in SRAM memory, 6T and 10T read mode. P Key performance metrics are the FINFET-based SRAM shows a reduction in power consumption that is 28.321 nW and delay that is drastically reduced to an extent of 0.16 ns vs. 0.27 ns, which subsequently saves much on PDP: power-delay product being a measure for energy efficiency. Overall PDP is improved by 40.01%. That means FINFET SRAM is quite much efficient compared with MOSFET-based SRAM. As the MOSFET-based SRAM is in consideration, then it decreases even further in the power as well as delay factors namely 12.52 nW whereas as against 16.7 nW and 0.12 ns whereas also 0.1825 ns respectively. On the other hand again the PDP increases drastically by reducing the factors 3.04 nJ to 1.50 nJ and it reflects that actually a better design is in question. Again, the percent improvement at PDP is very high at 50.65% compared to that in the 6T SRAM case which is representing much more significant advantages of FINFET transistors in the context of a high bit-cell configuration.

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.625| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

Performance Comparison Of 6T And 10T SRAM CELL in Read Mode

SRAM(T)	Transistor	Power(nW)	Delay(ns)	PDP(nJ)	Percentage improvement
6	MOSFET	31.234	0.27	8.43	40.01
	FINFET	28.321	0.16	4.53	
10	MOSFET	16.7	0.1825	3.04	50.65
	FINFET	12.52	0.12	1.50	

In the case of FINFET transistors, a few key parameters improved compared to MOSFETs in read mode for 6T and 10T SRAM cells. Actually, about 9.4% power consumption was saved with a FINFET-based 6T SRAM compared to that of MOSFET configuration (28.321 nW vs. 31.234 nW). Delay is also lesser for FINFET- (0.16 ns vs. 0.27 ns for MOSFET) and hence reads faster. The Power-Delay Product, PDP shows a better energy reuse. PDP rises from 8.43 nJ of MOSFET to 4.53 nJ of FINFET. The power for the layout around 10T decreased nearly by about 25% relative to its MOSFET counterpart-12.52 nW, whereas relative to 16.7 nW, and the delay comes down to 0.12 ns from 0.1825 ns. The PDP for FINFET 10T SRAM comes out to be very low at 1.50 nJ and significantly smaller compared to MOSFET because of 3.04 nJ values, thus improving 50.65 % in the regard of energy efficiency. Thus, these results prove that FINFET-based SRAM excels in the two performances of speed as well as energy efficiency also.

$I_{LEAKAGE}$ Comparison of SRAM CELLS

SRAM(T)	Transistor	$I_{leakage(nA)}$	Percentage improvement
6	MOSFET	44.608	50.22
	FINFET	22.204	
10	MOSFET	39.169	25.53
	FINFET	29.439	

The Leakage for the MOSFET-based SRAM is 39.169 nA whereas, for FINFET-based SRAM it has been reduced to 29.439 nA, thus leakage reduction of 25.53% has been noticed. Although this reduction is spectacular, it is not as high as the 50% improvement proven by the 6T SRAM configuration. This could be due to the reason that 10T SRAM has a larger bit-cell, which most probably provides more leakage paths; hence the leakage reduction efficiency of FINFET cannot be as remarkable as that of 6T design. In greater details, leakage currents in 6T SRAM with FINFET were reduced to 50.22%, whereas leakage currents in 10T SRAM with FINFET were reduced by 25.53%.

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.625| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

Comparison of SNM

SRAM(T)	SNM(Mv)	MOSFET	FINFET	*1)* Improvement(%) FINFET
6	HSNM	190	220	13.63
	RSNM	110	130	15.38
10	HSNM	210	270	22.20
	RSNM	210	270	22.20

The above results are taken from efficient sram based on finfet technology for low memory applications.[1]
FINFET transistors have been shown to improve SNM significantly for both 6T and 10T SRAM cells. In simple words, the cells will be more stable along with noise-resistant. For 10T SRAM, FINFETs offer more impressive enhancements regarding HSNM and RSNM by 22.20%, and in the case of 6T SRAM, HSNM is enhanced by 13.63% and RSNM by 15.38%. That means, the benefits to FINFET are much bigger at larger bit-cell designs wherein noise and stability become really more critical. FINFET improves noise margins, which leads to more reliable SRAM cells, especially at advanced technology nodes, because leakage and noise become more dominant. Therefore, the developed FINFET-based SRAM would present better overall performance by using noise margins that would give quality memory operations in the future.

V.CONCLUSION

Results showed that the 10T FinFET-based SRAM cell provides rich benefits over the conventional SRAM designs and thus can be considered an ideal candidate for the future requirements of low-power and high-performance memory. PDP, SNM, and leakage current with dramatic improvements indicate the benefits the adoption of FinFET in SRAM offers and surpass limitations at advanced CMOS technology nodes. The 10T SRAM cell with FinFET has a lower PDP and leakage current compared to the 6T and is well stable for reading and writing. Due to this structure having a high drain current (ID) and stable in the subthreshold region, this architecture can work at very high frequencies[7]. The SRAM cell 10T demonstrates very good scalability with SCE impacts shown not to result in effects down to 32nm for memory elements. PDP has been reduced to 80.80% in case of write operation and reduced to 50.65% during the read operation for MOSFET-based designs. Parameters SNM and leakage current also improved by 22.20% and 25.53%, respectively. This FinFET-based 10T SRAM technology may see wide proliferation towards ultra-low power applications in the future with the area efficiency much higher than the conventional 6T SRAM and other low-power SRAM cells.

REFERENCES

1.MV Nageswara Rao, "Design and development of efficient SRAM cell based on FinFET for low power memory applications." Journal of Electrical and Computer Engineering 2023.1 (2023): 7069746.
2.Panchal, Jigyasa, and Vishal Ramola, "Design and implementation of 6T SRAM using FinFET with low power application," International Research Journal of Engineering and Technology (IRJET), Vol.4.07 2017.
3. Sachdeva, A. and V. K. Tomar. "10T SRAM cell design with improved read performance and enlarged write margin." IET Circuits, Devices & Systems, vol. 15, no. 1, 2021, pp. 42-64.
4. Lakshmi, T. Venkata, and Madduraju Kamaraju. "Review on SRAM memory design using FinFET technology." International Journal of System Dynamics Applications (IJSDA) 11.6 (2021): 1-21.

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.625| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

5. Geethumol et al., "Power and area efficient 10T SRAM with improved read stability," ICTACT Journal on Microelectronics, vol. 3, no. 1, pp. 337-344, 2017.

6.Kaur, Navneet et al., "Low power FinFET based 10T SRAM cell," Proc. 2016 2nd International Innovative Applications of Computational Intelligence on Power, Energy and Controls with their Impact on Humanity (CIPECH), IEEE, 2016.

7. Rahaman, Mirwaiz, and Rajat Mahapatra. "Design of a 32nm independent gate FinFET based SRAM cell with improved noise margin for low power application."2014 International Conference on Electronics and Communication Systems (ICECS). IEEE, 2014.

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

INNO SPACE SJIF Scientific Journal Impact Factor

doi crossref

निस्केयर NISCAIR

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN COMPUTER & COMMUNICATION ENGINEERING

9940 572 462 6381 907 438 ijircce@gmail.com

www.ijircce.com

Scan to save the contact details