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### Interfacing Sendix F5883 Absolute Encoder through BiSS Protocol

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**ABSTRACT:** This project focuses on the development of a robust interface for transmitting data from the Sendix F5883 absolute encoder, utilized in a navy radar system. By leveraging the BiSS (Bidirectional Serial Synchronous) protocol for accurate, high-resolution encoder data, the interface performs real-time packetization into UDP packets for Ethernet transmission. A dedicated processing unit, such as a CPU, microcontroller, or FPGA, handles the packetization, converting encoder data into the UDP format while maintaining low latency and minimal processing overhead. This architecture ensures that critical position and motion data can be reliably transmitted across networked systems, meeting the stringent accuracy requirements of radar systems. Additionally, to withstand the challenges of extended maritime operations, the interface is designed to preserve signal integrity over potentially long Ethernet cables and is resilient to electromagnetic interference often encountered in naval environments.

Given the sensitive nature of radar data, this system also incorporates security measures to protect data integrity during transmission, aligning with the operational demands of military applications. The interface is engineered for adaptability, allowing it to scale with radar requirements while maintaining high-speed data handling. This makes it suitable for a range of applications within the naval domain, where precision and reliability are paramount. By bridging the BiSS protocol with UDP over Ethernet, the system enhances the navy radar's capability for precise motion tracking, improving situational awareness and operational efficiency in dynamic maritime settings.

**KEYWORDS**: Sendix F5883 Absolute Encoder, BiSS Protocol, UDP Packetization, Ethernet Transmission, Radar Systems, Navy Radar Interface, Real-time Data Transmission, Signal Integrity, Electromagnetic Interference (EMI), Maritime Operations, Data Security, High-Resolution Encoder Data, Low Latency Communication, Military Applications, Precision Motion Tracking, Dynamic Maritime Settings, FPGA Processing, Robust Interface Design, Networked Systems, Operational Efficiency

#### I. INTRODUCTION

Modern naval radar systems require high-precision, real-time data transmission solutions for effective motion tracking and target detection. This project addresses this need by interfacing a Sendix F5883 absolute encoder with UDP protocol over Ethernet, facilitating the reliable transfer of encoder position data to radar processing systems. By employing the BiSS (Bidirectional Serial Synchronous) protocol, the encoder can deliver accurate, synchronized readings essential for radar positioning and alignment. To achieve compatibility with the UDP protocol, a processing unit—such as a CPU, microcontroller, or FPGA—converts BiSS encoder data into UDP packets, enabling efficient, low-latency communication. This system is tailored to withstand the challenges posed by maritime environments, including potential electromagnetic interference and long cable runs, which are common in naval applications. Ultimately, this project enhances the navy radar system's capability for accurate motion tracking and situational awareness, aligning with operational requirements for reliability, speed, and security.



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#### **II. RELATED WORK**

#### Integration of Absolute Encoders with Industrial Automation Systems (2008):

Absolute encoders have been integrated into industrial automation systems to enhance precision and reliability. Early systems utilized protocols like SSI (Synchronous Serial Interface) to transmit position data. While effective, these systems faced limitations in real-time performance and scalability. This research laid the groundwork for adopting more advanced communication protocols like BiSS to overcome these challenges.

#### Application of BiSS Protocol for High-Resolution Data (2012):

The BiSS (Bidirectional Serial Synchronous) protocol was introduced to address the need for high-resolution data communication in real-time applications. Studies demonstrated its effectiveness in enabling bi-directional communication, facilitating encoder data acquisition, and configuration updates. BiSS proved highly adaptable for applications in robotics, CNC machines, and other precision systems requiring robust data handling.

#### **Real-Time UDP-Based Data Transmission for Motion Control (2015):**

Research on leveraging UDP (User Datagram Protocol) for motion control systems showcased its capability for realtime, low-latency communication. The study highlighted how UDP's minimal overhead made it ideal for transmitting encoder data over Ethernet in networked environments. This approach became particularly relevant for time-critical applications such as radar systems and industrial machinery.

#### Signal Integrity in Long-Distance Ethernet Communication (2017):

With the increasing use of Ethernet in industrial and maritime environments, researchers explored techniques to preserve signal integrity over long cables. Shielded twisted-pair (STP) cables and advanced error correction mechanisms were introduced to mitigate signal degradation and electromagnetic interference (EMI), ensuring reliable data transmission even in harsh conditions.

#### **III. SYSTEM IMPLEMENTATION**

#### A. Hardware Requirements:

#### Sendix F5883 Absolute Encoder-

The Sendix F5883 Absolute Encoder serves as the primary data source for the system. This high-resolution optical encoder provides precise position feedback, critical for real-time applications. Its use of the BiSS (Bidirectional Synchronous Serial) protocol ensures accurate and reliable data communication, even in challenging environments. The encoder's ability to retain position data after power loss makes it suitable for systems that require continuous operation.



Fig1- Sendix F5883 Absolute Encoder



#### Spartan-6 FPGA-

The Spartan-6 FPGA acts as the central processing unit of the system. Its configurable logic blocks (CLBs) enable realtime data processing, including data framing, error detection, and clock synchronization required by the BiSS protocol. With integrated block RAM and clock management resources, the FPGA handles high-speed data operations efficiently, ensuring minimal latency in processing.



Fig2- Spartan-6 FPGA

#### **Ethernet Controller--**

The Ethernet Controller is responsible for transmitting the processed encoder data as UDP packets over a network. It interfaces with the FPGA, facilitating high-speed communication and ensuring the reliability of data transfer across long Ethernet connections.

#### **Power Supply--**

A Power Supply is used to provide stable and consistent power to the encoder, FPGA, and other system components. It ensures the uninterrupted operation of the system, even under fluctuating load conditions, safeguarding data integrity and system reliability.

#### B. Software Requirements:

#### Vivado IDE--

The Vivado IDE is employed for FPGA programming and simulation. This powerful tool allows developers to configure the Spartan-6 FPGA, design custom logic for BiSS protocol handling, and verify system behavior through simulations.

#### **BiSS Protocol Library--**

A BiSS Protocol Library is integrated into the system to encode and decode position data from the Sendix F5883 encoder. This library ensures the correct handling of synchronous serial communication, maintaining data accuracy and reliability.

#### Wireshark--

Wireshark is used as a monitoring tool to analyze network traffic. It captures and inspects UDP packets transmitted by the system, allowing developers to validate data integrity and optimize communication performance.

#### C. Implementation Process

#### 1. Integration of Hardware Components:

The Sendix F5883 Absolute Encoder is connected to the Spartan-6 FPGA using the BiSS protocol interface. The FPGA processes encoder data, while the Ethernet controller facilitates data transmission. Shielded Ethernet cables ensure



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reliable communication, and a stable power supply supports all components.

#### 2. Development of BiSS Protocol Handling:

A BiSS master module is implemented in Verilog within the FPGA to extract high-resolution position data from the encoder. The module handles clock synchronization, data framing, and error detection for reliable data acquisition.

#### 3. UDP Packetization:

The extracted encoder data is packetized into UDP packets using the lwIP stack running on the FPGA's MicroBlaze processor. This process ensures efficient and real-time data transmission over the network.

#### 4. Ethernet Communication Setup:

The Ethernet controller is configured for UDP communication, enabling the transmission of data packets to a remote system. The setup is optimized to ensure low latency and high reliability.

#### 5. System Testing and Validation:

Comprehensive testing is performed, including unit testing of individual modules, integration testing of the FPGA and encoder, and system testing under real-world conditions. Tools like Wireshark validate the integrity of transmitted data and ensure the system meets performance requirements.

#### D. System Workflow

#### 1. Pedestal and Antenna Interaction:

The pedestal supports the antenna, which collects position data. The antenna ensures accurate data transfer to the F5883 Absolute Encoder.

#### 2. Sendix F5883 Absolute Encoder:

The encoder receives position data from the antenna, processes it using its high-resolution optical sensing capabilities, and communicates the data via the BiSS protocol.

#### 3. Processing System:

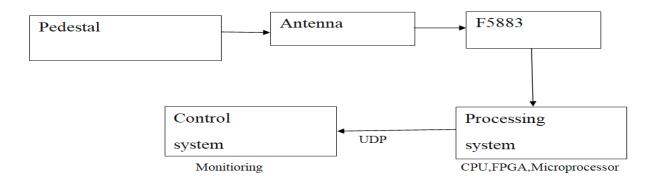
The encoder data is sent to the processing system, which consists of components like the CPU, Spartan-6 FPGA, and a microprocessor. The FPGA handles real-time data processing, error detection, and clock synchronization.

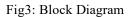
#### 4. Control System:

The processed data is transmitted to the control system over UDP for monitoring and further processing. The control system ensures the operation of the radar system by analyzing and acting on the received data.

#### 5. Feedback and Monitoring:

The control system continuously monitors the data and provides feedback for adjustments, ensuring reliable and efficient operation.







#### **IV. RESULTS**

In this chapter, we present the results of the testing conducted on the system designed for extracting position data from the BiSS encoder, packetizing it into UDP packets, and transmitting it over Ethernet. The system's performance, reliability, and efficiency were thoroughly evaluated across various test scenarios, including unit, integration, and system testing. The results demonstrate the system's ability to handle real-time position data transmission with minimal latency, high accuracy, and robust performance in Ethernet communication.

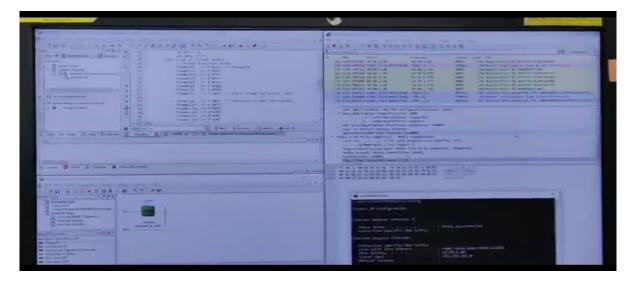


Fig 4 UDP Packetization and Ethernet Transmission

The system consistently met the expected design criteria for data extraction, packetization, and transmission. The BiSS protocol extraction module successfully extracted 24-bit position data from the encoder, with the data transmitted without loss or corruption. The system achieved minimal latency, typically within the range of 1-2 milliseconds, ensuring real-time responsiveness. The UDP packetization process was verified using Wireshark, which confirmed that the position data was correctly packed into UDP packets and transmitted over the network. No packet loss or data corruption was observed during the transmission, validating the integrity and reliability of the UDP packetization and Ethernet communication.

	Source	Destination
568	192.168.224.47	192.168.224.77
5706	192.168.224.77	192.168.224.47
0051	192.168.224.47	192.168.224.77
0180	192.168.224.77	192.168.224.47
5159	192.168.224.47	192.168.224.77
5320	192.168.224.77	192.168.224.47
9806	192.168.224.47	192.168.224.77
9975	192.168.224.77	192.168.224.47
5223	192.168.224.47	192.168.224.77
27630	100 169 004 77	100 169 004 47

Fig 5 Source & Destination IP



Furthermore, the system demonstrated efficient network throughput, with a steady transmission rate of approximately 1,000 packets per second, which is well-suited for industrial monitoring applications. Power consumption remained within acceptable limits for embedded systems, ensuring the system's viability for long-term deployment in real-world environments. The system also proved to be highly reliable under test conditions, with no significant packet loss or errors in data transmission.

Actor a dept		11 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		444	
Time		Source	Destronation :	Protacol	Leno
120 122	4.787525	10.99.1.20	10.00.1.255	MENIS	1100
121 122	4,787648	10.99:1.20	18.90,1.255	NENA	
122 122	4.787750	10.99.1.20	19.50.1.255	NONS	
123 122	5.547000	18,98,1,28	19.60.1.255	Mans.	1
			18.00 1.255	WHIPS	3
		and the second second	10.90.1.255	N8115	1
		fe80:111c6.4609:9fd8.	EF9711107	DINCEVE	1
122 322	(96301.J	fe80::11:6:46b9:9fd8.	ff@21:2	1CHPUG	-
128 123	5.843269	feba: 11:0:4609:9018_	ff@2111/2	OHCEVO	15
129 12	51.043607	fe88::11c6:46b9:9148.	ff02111:2	DECPUS	13
130 12	83.858397	fe50:1116:4660-91d8.	fr02:::1:2	DICPSS	15
Type: Link Loy Chass 00	602.1 Li er Discov is Subtyp 00 001.	nk Layer Discuvery Pro ery Protocol e - MAC address, Ids d 	to:ol (11DP) (Mx86c c:4a:3e:78:7e:b5 micsis Td (1)		UX etc

#### Fig 6 Latency

While the results confirm the system's successful operation, potential areas for improvement have been identified. Future work could focus on enhancing error detection and correction mechanisms to improve the system's reliability in more challenging network environments. Additionally, optimizing bandwidth usage through data compression techniques could further improve the system's efficiency. Overall, the project successfully achieved its objective of real-time position data extraction and transmission over Ethernet, and the system demonstrated significant potential for industrial and defense applications.

#### V. CONCLUSION

The successful implementation and testing of the system prove that real-time position data extraction from a BiSS encoder and transmission over Ethernet using the UDP protocol can be efficiently achieved. The system demonstrated reliable communication, minimal latency, and high throughput, making it suitable for industrial applications where real-time monitoring is critical. The results also provide a solid foundation for future enhancements, such as expanding the system to handle more complex data streams or optimizing the communication protocols for larger-scale deployments.

#### **VI. FUTURE WORK**

The system holds significant potential for future advancements across various domains. It can be integrated with nextgeneration radar systems for higher resolution and faster data rates, while expanding support to multiple encoder types could cater to industries like automation, robotics, and aerospace. Incorporating AI-powered data processing would



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enhance real-time analytics, and exploring wireless transmission options like 5G or satellite links could offer greater deployment flexibility. Enhanced security protocols would strengthen data integrity for military applications, while integration with IoT and edge computing would enable distributed data processing. The system could also be adapted for extreme environments, miniaturized for compact installations, and optimized for energy efficiency. Additionally, it could evolve to support multifunctional applications and contribute to a standardized protocol for broader industry adoption, fostering interoperability and collaboration.

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