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Prospects for Analog Circuits in Deep Networks

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ABSTRACT: Operations commonly used in machine learning algorithms, such as additions and softmax, can be effectively implemented using compact analog circuits. Analog Application-Specific Integrated Circuit (ASIC) designs leverage techniques like charge-sharing circuits and subthreshold transistors to achieve high power efficiency. With recent advances in deep learning algorithms, there has been a shift towards digital hardware accelerator designs that focus on matrix-vector multiplication operations. In these designs, power consumption is primarily dominated by the memory access power required for off-chip DRAM used to store network weights and activations. Emerging dense non- volatile memory technologies offer the potential for on- chip memory, and analog circuits are well-suited to perform the necessary multiplication-vector operations in conjunction with in-memory computing approaches. This paper provides a brief review of analog designs that implement various machine learning algorithms and offers an outlook on the use of analog circuits in low- power deep network accelerators suitable for edge or tiny machine learning applications.

I. INTRODUCTION

Machine-learning systems produce state-of-art results for many applications including data mining and machine vision. They extract features from the incoming data on which de- cisions are made, for example, in a visual classification task. Current deep neural network approaches in machine learning (ML) [1] produce state-of-art results in many application domains including visual processing (object detection [2], face recognition [3] etc), audio processing (speech recognition [4], keyword spotting etc), and natural language processing [5], to name a few. This improvement in algorithms and software stack has eventually led to a drive for better hardware that can run such ML workloads efficiently.

In recent times, edge computing has become a big research topic and edge devices that first process the local input sensor data are being developed within different sensor domains. Many current deep network hardware accelerators designed for edge devices are implemented through digital circuits. Less explored are analog/mixed-signal designs that can provide high energy-efficient implementations of deep network architec- tures. Custom analog circuits can exploit the physics of the transistors in implementing computational primitives needed in deep network architectures. For example, operations such as summing can be implemented by simpler analog transistor circuits rather than digital circuits. These designs can provide better area and energy efficiencies than their digital coun- terparts in particular for edge inference applications which require only small networks. With the increasing availability of dense new non-volatile memory (NVM) technology, the com- putation can be co-localized with memory, therefore further savings in power can be obtained by the reduction of off-chip memory access.

This article reviews analog and mixed-signal hardware chips that implement ML algorithms including the deep neural network architectures. We discuss the advantages of analog circuits and also the challenges of using such circuits. While other reviews have focused on analog circuits for on-chip learning [6], we focus more on implementations of generic building blocks that can be used in both training and inference phases.

The paper organization is as follows: First, Sec. II provides a brief review on analog circuits used for neuromorphic comput- ing and how these circuits can implement computational prim- itives useful for neural processor designs and ML algorithms. It is followed by Sec. III that describes basic operations (such as vector-matrix multiplications) being accelerated by analog building blocks, and Sec. IV that reviews the field of non- volatile memory technologies for deep network accelerators. Section V reviews recent Application-Specific Integrated Cir- cuits (ASICs) that implement certain ML algorithms. Finally, we end the paper with a discussion about future prospects of analog-based ML circuits (e.g. in-memory computing).

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II. REVIEW OF CIRCUITS FOR ANALOG COMPUTING

With great advances made in digital circuit design through the availability of both software and hardware design tools, analog circuits have taken a back seat in mainstream circuits and are now primarily used in high speed analog domains such as RF, power regulation, PLLs, and interface of sensors and actuators (e.g. in the analog-digital converter (ADC) readout circuits of analog microphone or biochemical sensors).

When it was proposed that the exponential properties of run- ning the transistors in subthreshold can be useful for emulating the structure of nervous system in the field of neuromorphic engineering [7], analog circuits became popular for emulating biological structures like the retina [8], implementing gen- eralized smoothing networks [9], [10], and both simplified and complex biophysical models of biological neurons. The exponential properties of a subthreshold transistor also make it easier to design analog VLSI circuits for implementing basic functions used in many mixed-signal neuromorphic systems such as the sigmoid, similarity [11], charge-based vector- matrix calculations [12], and highly distributed operations such as the winner-take-all [13].

Analog ML designs using these basic functions included a low-power analog radial basis function programmable sys- tem [14]; a sub-microWatt Support Vector Machine classifier design [15] with a computational efficiency of ~ 1 TOp/s/W; and the analog deep learning feature extractor system [16] that processes over 8K input vectors per second and achieves 1 TOp/s/W. The power efficiency of [16] is achieved by running the transistors in subthreshold and using floating-gate non-volatile technology for both storage, compensation and reconfiguration.

Even though analog neural processor circuits were already reported in the 1990s [17], they had taken a back seat partially because of the ease of doing digital designs; and the care needed for good matching in analog circuits. Although mismatch is usually reduced by using larger transistors, there are circuit strategies to minimize the mismatch effect, for example, by techniques to simplify the circuit complexity (Sec. III), floating-gate techniques to compensate for the mismatch, and training methods for deep networks to account for this mismatch as will be discussed in Sec. V.

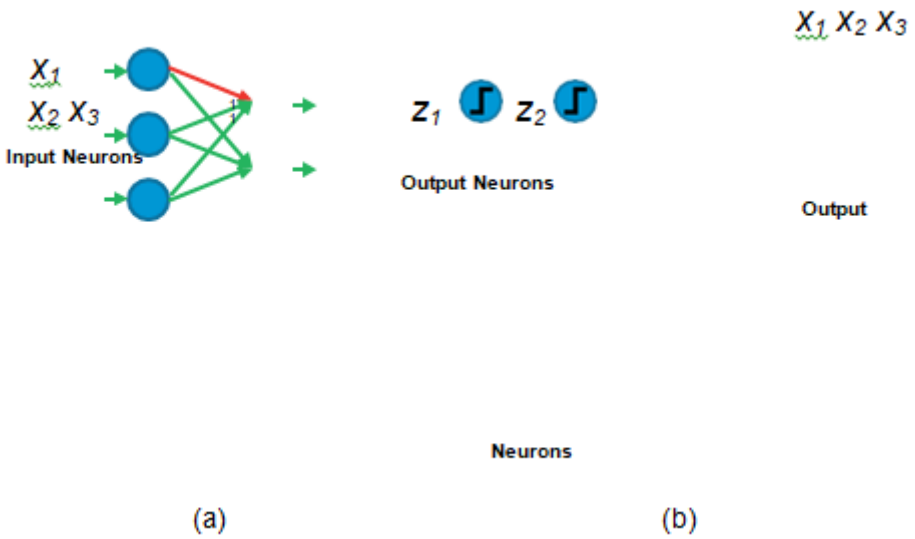

Fig. 1. Simple two-layer Artificial Neural Network (ANN) using a non-linear transfer function (a) and an implementation using a resistive crossbar array with differential weights: two non-negative resistors are used to represent a bipolar weight (b).

III. ANALOG CIRCUITS FOR MATRIX-VECTOR MULTIPLICATION

In a multi-layered neural network, the output of a neuron I in layer l is given by $y^l = g(z^l) = g(\sum w_{ij}x^l)$, where $g()$ is a nonlinear function and the j-th input to the l-th layer x^l is the j-th output from the previous layer (Fig. 1 (a)). The basic operations: summation, multiplication by scalars, and simple nonlinear transformations such as sigmoids can be imple- mented in analog VLSI circuits very efficiently. Dropping the index 1 denoting layer, we can write the most

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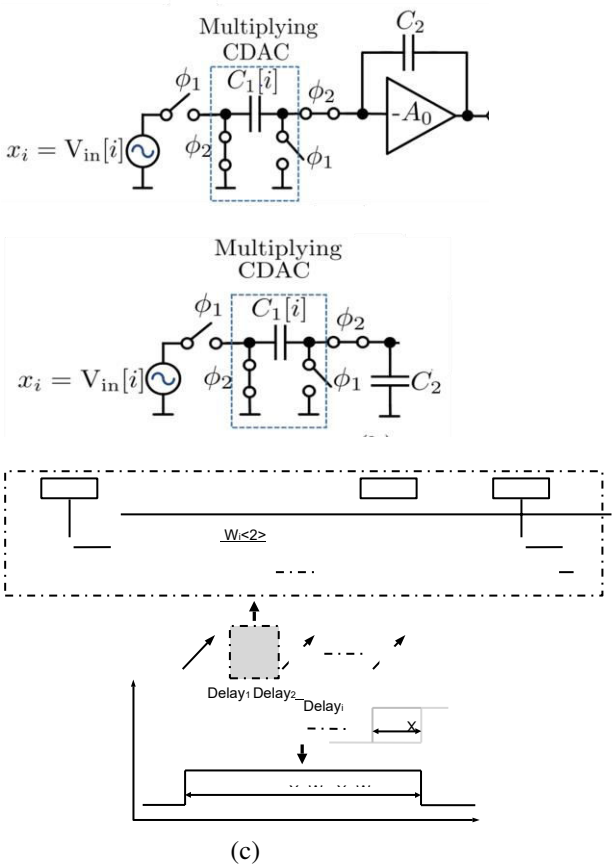
computationally intensive part as a matrix-vector multiplication (MVM) as follows:

$$z = \mathbf{W}x \quad (1)$$

where x is the vector of inputs to a layer, **W** denote the matrix of weights for the layer and z denotes the vector of linear outputs which is then passed through a nonlinear function g() to produce the final neuronal output. Figure 2 illustrates how the key core computation of weighted summation can be



(c)

Fig. 2. Three modes of matrix-vector multipliers using analog circuits: (a) Charge (b) Time and (c) Current. Figures adapted from [18], [19] and [20].

performed in three modes: (a) Charge, (b) time and (c) current. Further storage of weight coefficients can be performed in a volatile or non-volatile manner. More details about these different possibilities are described next.

a. Charge: Figure 2(a) depicts a capacitive digital analog converter (CDAC) based charge mode MVM circuit. In this circuit, the weight is stored in the form of binary weighted capacitor sizes (shown as C1[i] in the figure) and hence weighting of input happens naturally by charging the desired capacitor value with the input voltage. Summation happens through the process of charge redistribution among capacitors via switched capacitor circuit principles. The charge redistri- bution can be more accurate if done by using an amplifier in a negative feedback configuration (as shown on top of Fig. 2(a))–this is referred to as an active configuration [18], [21]. On the other hand, the passive configuration without an amplifier (shown below the active one) has the benefit of high speed operation due to the absence of settling time limitations from the amplifier. However, it was shown in [18] that the errors in the passive multiplication amount to a change in the coefficients of the weighting matrix **W** and can be accounted for. A disadvantage of this approach is that it requires N clock cycles to perform a dot product on two N dimensional vectors. Static random access memory (SRAM) is used to store the weights–hence, it suffers from volatile storage issues. A 6-b input, 3-b weight implementation of this approach achieved ≈ 7.7 − 8.7 TOp/s/W energy efficiency at clock frequencies of 1 − 2.5 GHz clock frequency [18]. Other recent implementations using this approach are reported in [22] and [23].

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b. Time: Another way of implementing addition in the analog domain is by using time delays. Figure 2(b) shows how addition can be implemented through the accumulation of delays in cascaded digital buffer stages [19]. By modifying the delay of each stage according to the weight, a weighted summation can be achieved. Figure 2(b) shows one example of a delay line based implementation of this approach. Here, the weight storage is in volatile SRAM cells. The authors used a thermometer encoded delay line as an unit delay cell to avoid nonlinearity at the expense of area. A 1-b input, 3-bit weight architecture achieved very high energy efficiency of ≈ 105 TOp/s/W at 0.7 V power supply [19].

c. Current: By far, the most popular approach for analog VMM implementation is the current mode approach. This architecture offers flexibility in choosing the way input is applied (encoding magnitude in current [24], voltage [25] or as pulse-width of a fixed amplitude pulse [26]) and non- volatile weight storage (Flash [27], PCM [28], RRAM [25], MRAM [29], Ferroelectric FETs [30], ionic floating-gate [31], transistor mismatch [32], etc). An example implementation using standard CMOS compatible Flash transistors shown in Fig. 2(c) was presented as early as 2004 [20].

In these approaches, a crossbar array of NVM devices are used to store the weights **W**. In the case of Flash, the inputs xj can be encoded in current magnitude ($I^{+} - I^{-}$) and presented j j along the columns (word-lines) while current summation occurs along the rows (bit-lines) by virtue of Kirchhoff's Current Law (KCL) to produce the output zj. Here, the weighting happens through a sub-threshold current mirror operation of the input diode-connected Flash transistor and the NVM device in the crossbar with weight being encoded as charge difference between the two devices. Since then, several variants of these Flash-based VMM architectures have been published using amplifier based active current mirrors [33] for higher speed, source coupled VMM for higher accuracy [34] and special Flash process based VMM [27] with promise of scaling down to 28nm. These approaches generally achieve energy
efficiencies in the range of 5 − 10 TOp/s/W.

An interesting alternative is to use the threshold voltage mismatch in-built in transistors as a weight quantity. This leads to ultra-compact arrays for VMM operation [24]. However, since these weights are random, they may only be used to implement a class of randomized neural networks such as reservoir computing, neural engineering framework, extreme learning machines etc. While these networks are typically only two layers deep, they have advantages of good generalization and quick retraining. Such approaches have been used for brain-machine interfaces [35], tactile sensing [36] and image classification [37].

The recent trend in this architecture is to use resistive memory elements, sometimes dubbed memristors, as the NVM device in the crossbar. They are less mature but offer ad- vantages of longer retention, higher endurance, low write energy, and promise of scaling to sizes smaller than Flash transistors. They have also been shown to support back- propagation based weight updates with small modifications to the architecture. Due to their increasing popularity in deep network implementations, we will discuss them further in the next section.

IV. NON-VOLATILE RESISTIVE CROSSBARS

A popular approach for performing the matrix-vector multi- plications in ML - and especially in the deep neural networks of today - is to leverage emerging non-volatile memory technologies such as phase change (PCM), oxide-based re- sistive RAM (RRAM or memristors), and spin-torque mag- netic technologies (STT-MRAM). The equivalent of an ANN implemented in a resistive memory array is shown in Fig. 1 (b). As further illustrated in Fig. 3, a dense crossbar circuit is constructed with these resistive elements or memristors at every junction. Each resistor is analog tunable to encode mul- tiple bits of information (from binary to over seven bits [38], [39]). Most importantly, the devices retain this analog resistive programming in a non-volatile manner. This is appropriate for encoding the heavily reused weights in deep neural networks, such as convolution kernels or fully connected layers. And, as noted earlier, this allows for the dominant vector-matrix computations to be performed in-memory without the costly fetching of neural network (synaptic) weights.

To take full advantage of analog non-volatile crossbars in deep neural networks, it is necessary to devise a larger architecture that supplements the vector-matrix computations performed in-memory, with a range of additional data orches- tration and processing performed by traditional digital circuits. These include operations such as data routing, sigmoidal or other nonlinear activation functions, max-pooling, and nor- malization. Several prior works have explored this design- space [40], [41] for resistive crossbars, with the inclusion of schemes to encode arbitrarily high precision weights across multiple resistive elements ("bit-slicing") and the overhead in constantly converting all intermediate calculations performed within analog resistive crossbars back into the digital domain

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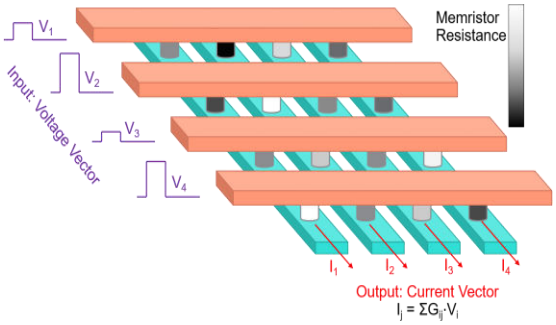
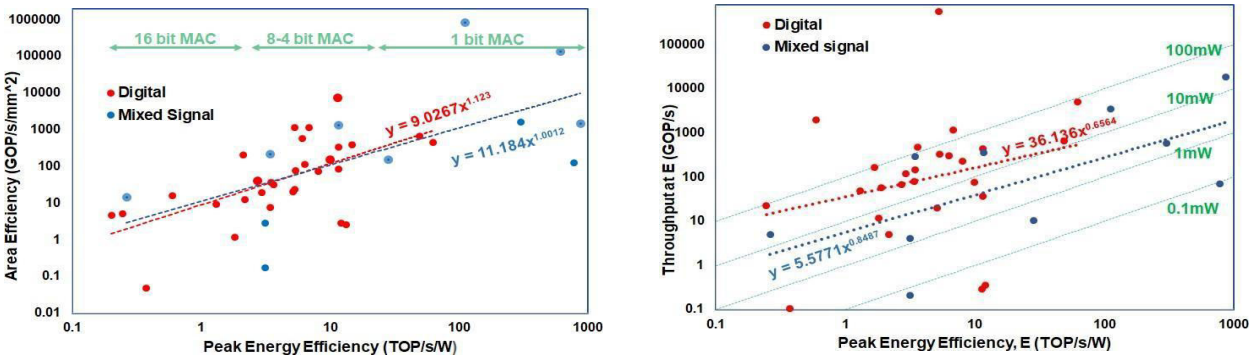


(a)

Fig. 3. Performing vector-matrix multiplication in non-volatile resistive (memristive) crossbar arrays.

The input can be encoded in voltage amplitude with fixed pulse width, as shown here, or other approaches such as fixed amplitude and variable pulse width. At each crossbar junction, a variable resistor is present representing a matrix weight element, modulating the amount of current injected into the column wires through Ohm's law. On each column, the currents from each row are summed through Kirchhoff's current law, yielding the desired output vector representing the vector-matrix product. Pairs of differential weights can be utilized as in Fig. 1(b) to allow bipolar representations. to avoid error accumulation in deep networks of potentially tens of layers. An architecture and performance analysis was first done for CNNs [40], and then extended to nearly all modern deep neural networks including flexible compiler support [42].

To date, non-volatile resistive crossbars have been explored for both the inference and training modes of deep neural networks. In the case of inference, the main advantage from NVM comes from reduced data-fetching and movement, while reprogramming of the crossbars is infrequent, requiring lower endurance from the resistive technology (PCM or RRAM), but potentially higher retention and programming yield ac- curacy [43]. To handle device faults, programming errors, or noise, novel techniques for performing error-detection and cor- rection for the computations performed within these crossbar arrays have been devised recently [44], [45] and experimen- tally demonstrated [46]. On the other hand, implementation of training in NVM crossbars [47], [48], [49] can take advantage of efficient update schemes for tuning each of the resistive weights in parallel (e.g., "outer product" updates such as in [50]). In turn, the implementation of neural network training puts a larger burden on the underlying NVM technology from an endurance perspective, and requirements for a symmetric and linear change in the device resistance when programmed up or down. While the technology remains highly promis- ing, the current state of resistive NVM suffers from large programming asymmetries and uniformity challenges. As the technology continues to mature, some current approaches are able to mitigate these setbacks by complementing the resistive technology with short term storage in capacitors [51], or oper- ating in a more binary mode [52], but with cost of either area or prediction accuracy. Nonetheless, practical demonstrations using resistive crossbar networks have already included, to name just a few, image filtering and signal processing [53], fully connected and convolutional networks [48], [39], [51], LSTM recurrent neural networks [25], and reinforcement learning [54].



(a) (b)

Fig. 4. Machine learning hardware trends: Peak energy efficiency vs throughput (a) and area efficiency (b) for recent ASIC implementations reported in ISSCC, SOVC, and JSSC (see main text).

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V. FUTURE OF ANALOG DEEP NEURAL NETWORK ARCHITECTURES

Analog circuits can be more compact than digital circuits, especially for certain low-precision operations like the add operation needed in neural network architectures or the in- memory computing circuits for summing up weighted currents [55]. While mismatch variations could be a feature for certain network architectures like the Extreme Learning Net- works, they need to be addressed in analog implementations of deep networks by using design techniques such as the schemes described in Sec. III or through training methods that account for the statistics of the fabricated devices.
The work of [56] shows that it is possible to use neural net- work training methods as an effective optimization framework to automatically compensate for the device mismatch effects of analog VLSI circuits. The response characteristics of the individual VLSI neurons are added as constraints in an off- line training process, thereby compensating for the inherent variability of chip fabrication and also taking into account the particular analog neuron's transfer function achievable in a technology process. The measured inference results from the fabricated analog ASIC neural network chip [56] matches that from the simulations, while offering lower power consumption over a digital counterpart. A similar retraining scheme was used to correct for memristor defects in a memristor-based synaptic network trained on a classification task [57].

A. Trends in machine learning ASICs

To understand the energy and area efficiency trends in recent ASIC designs of ML systems, we present a survey [58] of papers published in IEEE ISSCC and IEEE SOVC conferences from 2017-2020 (similar to the ADC survey in [59]), and in the IEEE Journal of Solid-state Circuits (JSSC).

Using the data from [60], we show two plots. The first plot shows the throughput vs. peak energy efficiency tradeoff for digital and mixed-signal designs (Fig. 4(a)). It can be seen that while throughput is comparable for analog and digital approaches, the energy efficiency for mixed-signal designs is superior to their digital counterparts. Figure 4(b) plots the area efficiency vs peak energy efficiency for these designs and further classifies the digital designs according to the bit-width of the multiply-accumulate (MAC) unit. It can again be seen that the mixed-signal designs have better tradeoff than the digital counterparts. Furthermore, as expected, lower bit widths lead to higher efficiencies in terms of both area and energy. Lastly, the efficiency of mixed-signal designs seem significantly better than digital designs only for these with very low-precision 1-bit MACs.

VI. CONCLUSION

While deep network accelerator designs are implemented primarily using digital circuits, in-memory computing systems can benefit from analog and mixed-signal circuits for niche ultra low-power edge or biomedical applications. The peak energy efficiency trends in Fig. 4 show that mixed-signal designs can be competitive at lower-bit precision parameters for network accelerators. Some of the analog machine learning circuit blocks such as the sigmoid and the winner-take-all de- signs can implement directly the sigmoid transfer function of the neuron, and the soft-max function of the final classification layers of a deep network. It will be interesting to see how these circuits will be incorporated further into in-memory computing systems in the future.

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